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Approximate Reverse Carry Propagate Adder for Energy-Efficiency

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Abstract: ***The hypothesis of estimated measure is to design computation quality for computation efforts. The Approximate full adders (AFA's) are the lead objective to reduce the length of carry propagation which is put through to the slightest error rate. Approximate adder comes up with important enhancement in delay, area and power. The developing attribute is carry doesn't propagate in it. So in this we mainly use the hybrid adders where it utilizes the RCPFA. The approximate adder generates the input carry from higher bit to lower bit to produce carry output, , the weight of the carry reduces when it generates. In Reverse Carry Propagate Adder there are accomplishments to be completed those are the power, delay and energy. So, compared to the conventional ones the Approximate Mirror Adders (AMA's) has less transistors compared to it. This is to establish on the internal structure of the mirror adder which consumes less area and power consumption as well as higher speed. The representation performed by the RCPFA and hybrid adders is observed and compared using Mentor Graphics. As a result, it consists of higher accuracies and specifies that, by working on the RCPFA in the hybrid adders can consists of improved consumption of area by 14%, consumption of power by 19.2%, consumption of delay by 27%.***

Keywords: ***RCPFA, Approximate Adder, Approximate Mirror Adder, Mentor Graphics, Hybrid Adder, Conventional Adder, Accuracy, Delay.***

I. INTRODUCTION

Adder: Adders are combinations of logic gates that unite binary values to obtain a sum. They are classified according to their capacity to accept and combine the digits.

Hybrid Adders: Hybrid adders combine various additional plans to achieve implementation delay or area constraints. Hybrid adders use carry-look ahead and carry-select schemes. Hybrid adders are also relevant when the operand bits to the final adder in tree multipliers do not approach simultaneously. In such a condition, a hybrid adder gives an efficient implementation.

FULL ADDER: The full adder becomes mandatory when a carry input must be added to the two binary digits to attain the correct sum.

Literature Survey: An adder is a digital circuit that accomplishes addition of numbers. In other types of processors, adders are used in the arithmetic logic units (ALU). A full adder adds three one-bit binary numbers, two operands and a carry bit.

Table1: Truth Table of Full - Adder

INPUTS			OUTPUTS	
X	Y	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The adder represents two numbers a sum and a carry bit. Energy efficiency directly means that using less energy to achieve the same task that is, removing energy waste. Energy efficiency brings a variety of benefits: reduction of greenhouse gas emissions, reduction of demand for energy imports, and minimizing our costs on a household and economy-wide level. While sustainable energy technologies also help perform these objectives, enhancing energy efficiency is the cheapest and frequently the most instant way to reduce the use of fossil fuels.There are vast chances for efficiency improvements in every part of the economy, whether it is exponents.

Existing System: There are Five Approximate Mirror Adders (AMA's) having less number of transistors compared to that of the conventional adder have been suggested. These designs are based on simplifying the internal structure of the approximate mirror adders which removes the transistors of the tables of AMA-I, AMA-II, AMA-III and AMA-IV are represented and in AMA-V.

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Author [citation]	Adopted methodology	Features	Challenges
T.Jagannadha Swamy, / Meera G	complexity of a conventional MA cell by reducing the number of transistors.	transistors help in reducing the effective switched capacitance	number of transistors compared to convention al ones.
Vaibhav Gupta	to simplify the complexity of a conventional mirror adder cell by reducing the number of transistors and also the load capacitances	utilize them to design approximate multi-bit adders.	The errors introduced by these approximations are reflected at a high level
P. Divakara Varma, R.Ramana Reddy	require ment of no. of transistors had been reduced remarkably.	average power dissipation and delay using a set of input vectors for equal time periods.	But dynamic power dissipation is Increased.
Ihsen Alouani, Hamzeh Ahangari, Ozcan Ozturk, and Smail Niar	It leads to lower error rates compared to the classical homogeneous designs	To limit the overall deviation from the exact results	It results in an approximate multiplier with higher accuracy and better tradeoffs

Existing Drawbacks:

1. The Area and Power was high compared to the suggested method.

2. Its Accuracy is very low.

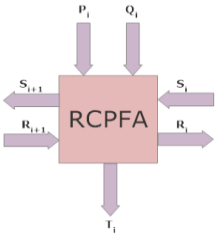
System Technique:

Reverse Carry Propagate Adder (RCPA**).**

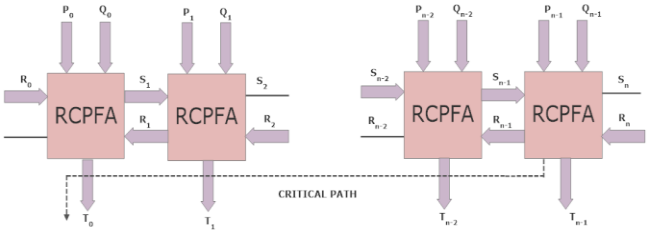
Advantages:

- It consumes less power.
- Increase in the Speed.
- Accuracy is high.

Block Diagram:



(A)



(B)

Fig.1. (A) Schematic outline of RCPFA. (B) Proposed n-bit RCPA

A New RCFA:

Each exact full adder creates its convey yield and whole flag using

$$2R_{i+1} + T_i = P_i + Q_i + R_i \qquad \text{——— (1)}$$

$$T_i - R_i = P_i + Q_i - 2R_{i+1} \qquad \text{——— (2)}$$

Error Analysis:

$$M = 1/2^{2n} \sum_{i+1}^{2^{2n}} |D_i/T_i|$$

The proposed RCPFA is obtained as follows

RCPFA1:

$$R_i = \overline{S_i}(\overline{R_{i+1}}(P_i+Q_i)) + \overline{(R_{i+1}+ (P_iQ_i))}$$

$$K(R_{i+1}=0|P_i=1 \cap Q_i=1)) = 1/3 - 4^i/3*4^{n-1}$$

$$K(R_{i+1}=1|(P_i=0 \cap Q_i=0)) = 1/3 - 4^i/3*4^{n-1} \quad \text{i.e.,}\{0,1,....,n-2\}$$

Truth Table:

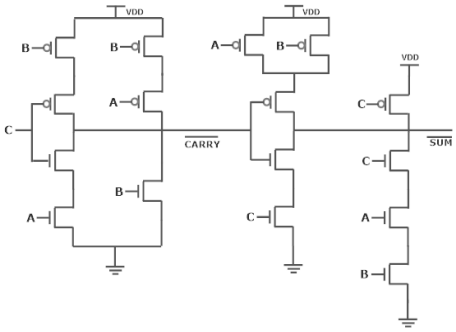
For Traditional FA, AMA-I TO AMA-IV

INPUT	CONV.FULL ADDER	AMA 1	AMA 2	AMA3	AMA 4

A	B	C	SUM	CARRY	SUM	CARRY	SUM	CARRY	SUM	CARRY	SUM	CARRY
0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	1	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	0	1	1	0	0	1	0	0
0	1	1	0	1	0	1	0	1	0	1	1	0
1	0	0	1	0	0	0	1	0	1	0	0	1
1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	1	0	1	0	1	0	1
1	1	1	1	1	1	1	0	1	0	1	1	1

STRUCTURES:

AMA-I:



It exhibits the approximation Mirror Adder-I. In order to get approximate mirror adder (AMA-I) with fewer transistors, we start to detach transistors from the conventional schematic one after the other. Though, we should not do this in an random manner. We have to make sure that any input combination of A, B and Carry will not result in short circuits or open circuits in the simplified schematic. Another main rule is that the resulting simplification should establish less errors in the Full It Adder.

AMA-II:

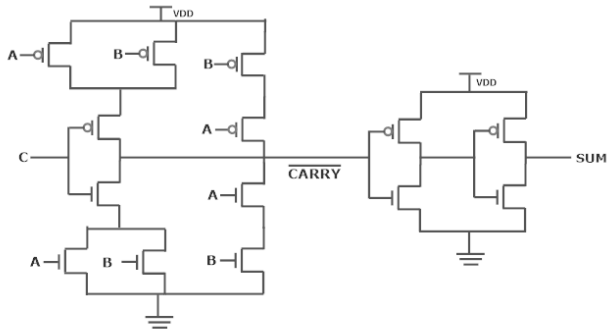


Fig.3: Approximate Mirror Adder 2

In Full Adder the truth table indicates that the Sum = carry' for six out of eight cases, excluding the two input combinations A = 0, B = 0, C = 0 and A = 1, B = 1, C= 1. At present, in the conventional mirror adder, carry is calculated in the first step. Therefore, an simple way to get a simplified schematic is to set Sum=carry . Though, we establish a buffer stage after carry to generate the same functionality.

AMA-III:

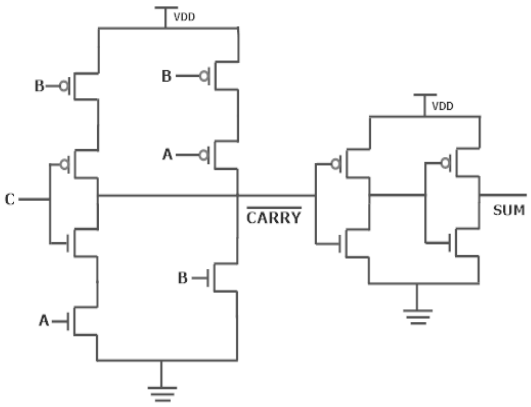


Fig.4: Approximate Mirror Adder 3

Approximation Mirror Adder- III is a combination of AMA-I and AMA-II. This introduces three faults in Sum and one fault in Carry.

AMA-IV:

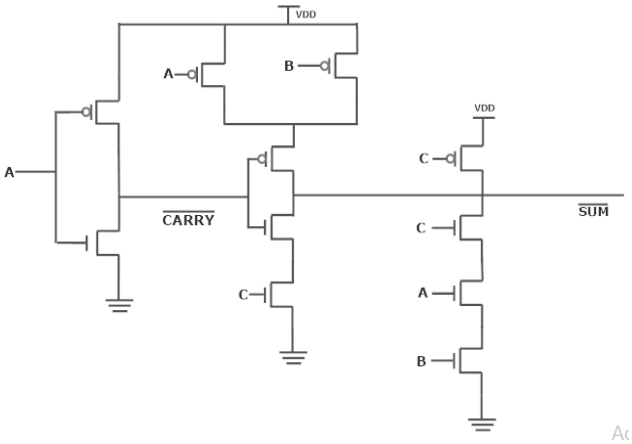


Fig.5: Approximate Mirror Adder 4

It exhibits the fourth Approximation Mirror Adder (AMA-IV). From the truth table we can observe that carry = A for six out of eight cases. Similarly carry = B for six out of eight cases. So, we consider carry = A. We use inverter in this type with input A to calculate carry' and Sum is calculated similar to approximation mirror adder-I. So in this there are two faults in Carry and three faults in the Sum.

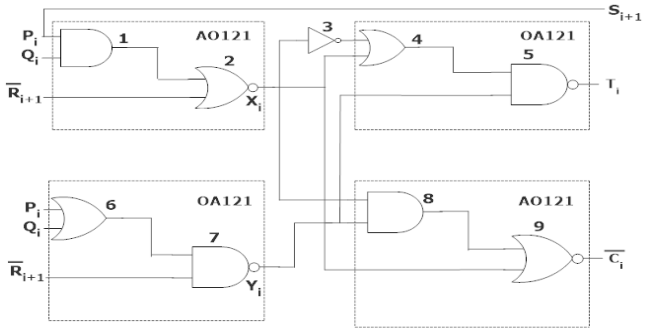
Truth Table:

ITEM	P_i	Q_i	R_{i+1}	S_i	T_i	C_i	S_{i+1}	X_i	Y_i
1	0	0	0	0	0	0	0	0	1
2	0	0	0	1	1	1	0	0	1
3	0	0	1	X	0	1	0	1	1
4	0	1	0	X	1	0	0	0	0
5	0	1	1	X	0	1	0	1	1
6	1	0	0	X	1	0	1	0	0
7	1	0	1	X	0	1	1	1	1
8	1	1	0	X	1	0	1	0	0
9	1	1	1	0	0	0	1	0	1
10	1	1	1	1	1	1	1	0	1

(a)

Fig.6: (a) Truth Table of RCPFA-I

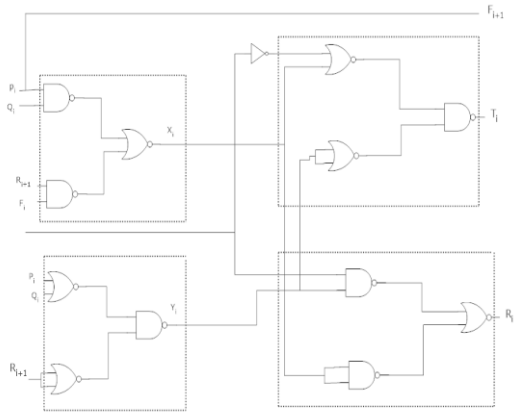
Internal structure:



(a)

Fig.7: (a) RCPFA I

Modified Circuit:



(b)

Fig.7: (b) RCPFA 1 Modified Circuit

Results:

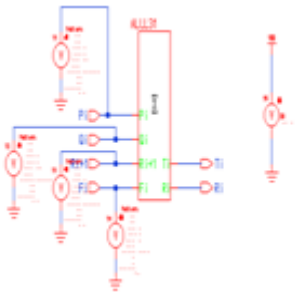


Fig.7: (A)

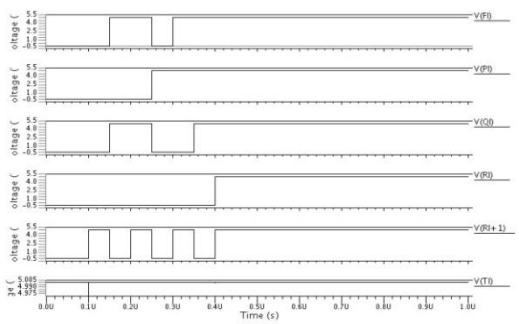


Fig.7: (B) Inputs

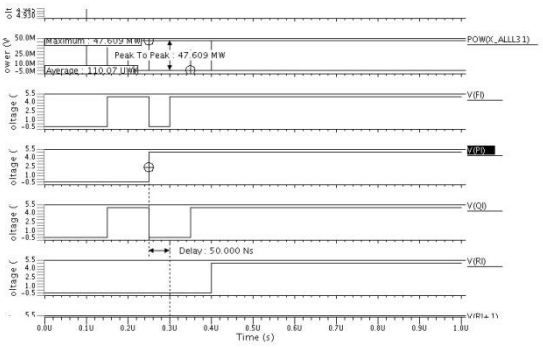


Fig.7: (C) Power and Delay

Conclusion:

In the proposed article rough RCPFAs, spread convey noteworthy to LSBs. The turnarounds convey spread gave higher dependability in delay variation. The adequacy of the proposed estimated FAs and the half and half adders which acknowledged them has been examined in mentor graphics the outcomes show that we proposed RCPFA's area by 14%, consumption of power by 19.2%, consumption of delay by 27%.

REFERENCES:

1. Z. Yang, A. Jain, J. Liang, J. Han, and F. Lombardi, "Approximate XOR/XNOR-based adders for inexact computing," in Proc. 13th IEEE Int. Conf. Nano technol. (NANO), Aug. 2013, pp. 690–693.
2. Z. Yang, J. Han, and F. Lombardi, "Transmission gate-based approximate adders for inexact computing," in Proc. IEEE/ACM Int. Symp. Nanosc. Archit. (NANOARCH), Jul. 2015, pp. 145–150.
3. J. Liang, J. Han, and F. Lombardi, "New metrics for the reliability of approximate and probabilistic adders," IEEE Trans. Comput., vol. 62, no. 9, pp. 1760–1771, Sep. 2013.
4. H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 49, no. 1, pp. 25–30, Jan. 2002.
5. Prasad G.R.K., Babu P.S.S., Khan H., Niak K.K., Generation of radiation characteristics from waveguide slot arrays for satellite tracking radar system,2017 INCEMIC 2015 - 13th International Conference on Electromagnetic Interference and Compatibility, Proceedings, pp:276-278, DOI: 10.1109/INCEMIC.2015.8055894, ISBN: 9.78151E+12
6. Murali A., Hari Kishore K., Rama Krishna C.P., Kumar S., Trinadha Rao A., Integrating the reconfigurable devices using slow-changing key technique to achieve high performance,2017 Proceedings - 7th IEEE International Advanced Computing Conference, IACC 2017, pp: 530-534, DOI: 10.1109/IACC.2017.0115, ISBN: 9.78151E+12
7. Suresh Kumar N., Pavan Kumar K.V.K.V.L., Preetham Reddy C.S., Tirumalasetty V.R., Suman M., A novel region wise random valued impulse noise detection and filtering,2017 Journal of Advanced Research in Dynamical and Control Systems, Vol:9, pp: 1983-1991, ISSN: 1943023X.
8. Prasad G.R.K., Srinivas Babu P.S., Siddaiah N., Srinivasa Rao K.,Design and simulation of MEMS based sensor for early detection of PD,2017 2016 International Conference on Electrical, Electronics, Communication, Computer and Optimization Techniques, ICEECCOT 2016,Vol:, issue:,pp: 366-371,DOI: 10.1109/ICEECCOT.2016.7955247,ISBN: 9.78151E+12
9. Siva D., Sunithamani S., Bojja P., An automated damage assessment index to quantify damage for disaster management using satellite images,2017 Journal of Advanced Research in Dynamical and Control Systems, Vol:9, issue:1, pp: 407-420, ISSN: 1943023X
10. Vasudha M., Pravallika B.S., Kiran C.S., Subhani P., Rakesh Chowdary G., Prakash M.D., Kishore K.H., Ramakrishna T.V., Design and performance analysis of a nonvolatile memory cell,2017 Journal of Advanced Research in Dynamical and Control Systems, Vol:9, issue: Special Issue 14, pp: 2320-2327, ISSN: 1943023X.

11. Prasad K.V., Prasad G.R.K., Kranthiveer D., Sowmya D., Nikesh M., Sailesh T.V., ECG signal acquisition and analysis for portable heart monitoring devices,2017 Journal of Advanced Research in Dynamical and Control Systems, Vol:9, issue: Special Issue 14, pp: 1685-1693, ISSN: 1943023X
12. Murali Krishna B., Khan H., Madhumati G.L., Praveen Kumar K., Tejaswini G., Srikanth M., Ravali P., FPGA implementation of des algorithm using DNA cryptography,2017 Journal of Theoretical and Applied Information Technology, Vol:95, issue:10, pp: 2147-2158, ISSN: 19928645
13. Kumar P.K., Rao P.P., Kakarla H.K., Optimal design of reversible parity preserving new Full adder / Full subtractor,2017 Proceedings of 2017 11th International Conference on Intelligent Systems and Control, ISCO 2017, pp: 368-373, DOI: 10.1109/ISCO.2017.7856019, ISBN: 9.78151E+12
14. Noorbasha F., Manasa M., Gouthami R.T., Sruthi S., Priya D.H., Prashanth N., Rahman M.Z.U., FPGA implementation of cryptographic systems for symmetric encryption,2017 Journal of Theoretical and Applied Information Technology, Vol:95, issue:9, pp: 2038-2045, ISSN: 19928645
15. Narasimhanayak V., Lokesh V., Chaitanya V., Feroz M., Soundarya D., Sai Krishna V., Design of bandgap reference circuits,2017 Journal of Advanced Research in Dynamical and Control Systems, Vol:9, issue: Special Issue 6, pp: 840-846, ISSN: 1943023X
16. Tulasi S.K., Prasad G.R.K., Siva Kumar M., Bharath Kumar Reddy A., Giridhar Y., Ajay Reddy C.V., Supriya P.,Design and analysis of T-shaped mendor structure for CPW MEMS switches,2017 Journal of Advanced Research in Dynamical and Control Systems,Vol:9, issue: Special Issue 17,pp: 1987-1994, ISSN: 1943023X
17. Ganesh G.V., Srinivasa Rao K., Pavansai Prasad N., Goutham Krishna K., Sravani T., Hemeema K., RF mems based tunable cpw band pass filter integrating periodic circular slot cells,2017 Journal of Advanced Research in Dynamical and Control Systems, Vol:2017, issue:17 Special Issue, pp: 2053-2065, ISSN: 1943023X
18. Bharadwaj M., Kishore H.,Enhanced launch-off-capture testing using BIST design,2017 Journal of Engineering and Applied Sciences,Vol:12, issue:3,pp: 636-643,DOI: 10.3923/jeasci.2017.636.643,ISSN: 1816949X
19. Murali Krishna B., Madhumati G.L., Khan H., Stochastic key generation mechanism in cryptography applications through partial reconfiguration,2017 Journal of Advanced Research in Dynamical and Control Systems, Vol:9, issue: Special Issue 12, pp: 1566-1586, ISSN: 1943023X
20. Prasad G.R.K., Vivek T., Phani Rohith B., Yashwanth Y.,Verilog implementation on cryptography encryption and decryption of 8 bit data using ECC algorithm,2017 Journal of Advanced Research in Dynamical and Control Systems,Vol:9, issue: Special Issue 14,pp: 2711-2719, ISSN: 1943023X
21. Tulasi S.K., Siva Kumar M., Amruthalakshmi P., Akhila M., Teja M., Mohan Shankar G., Performance analysis of through silicon via's (TSV's),2017 Journal of Theoretical and Applied Information Technology, Vol:95, issue:10, pp: 2125-2131, ISSN: 19928645
22. Lakshmi Narayana T., Girija Sravani K., Srinivasa Rao K., A micro level electrostatically actuated cantilever and metal contact based series RF MEMS switch for multi-band applications,2017 Cogent Engineering, Vol:4, issue:1, DOI: 10.1080/23311916.2017.1323367, ISSN: 23311916
23. Manasa M., Noorbasha F., Sudheshna C.L., Santhosh M., Naresh V., Rahman M.Z.U., Comparative analysis of cordic algorithm and taylor series expansion,2017 Journal of Theoretical and Applied Information Technology, Vol:95, issue:9, pp: 2015-2022, ISSN: 19928645
24. Prasad G.R.K., Siddaiah N., Preeti M., Rao K.S., Bhavitha E., Babu P.S.S., Comparative analysis of mems capacitive pressure sensor for detection of tremors in parkinson's disease,2017 Journal of Theoretical and Applied Information Technology, Vol:95, issue:9, pp: 2023-2030, ISSN: 19928645

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