

A Multilayer High-Speed Magnetic-Tunnel-Junction Magneto-resistive RAM Structure with Read-Disturb-Detection Circuit by Using Nano-Electronics Quantum Dot Cellular Method

Rupsa Roy, Swarup Sarkar, Sudipta Das



Abstract: In this nano technical world the “Complementary MOS technology” can be replaced by using “Quantum Dot Cellular Automata” with reversible logical phenomenon to achieve a fault tolerant, low-cost nano electronics formation by feature size, latency and power consumption minimization. The memory is one of the most interesting part of research in this digital world. This paper represents an optimizing high-frequency (in THz) reversible design of a “Random Access Memory” which is simulated by using nano electronics ‘QCA’ simulator to get a better performance than “Complementary MOS technology” with high frequency (in THz), less occupied area and dissipated power. This paper also shows a highly-flexible magnetic quantum cell logic-design and MTJ logical representation which is used for non-volatile MRAM which is widely used in digital electronics world and as a part of aerospace and military device. A reversible nano electronics formation of the control logic to select the word-line and input-line of the MRAM also presented here. The reversible-logic can avoid the information-loss in memory device by zero-heating technique. Non-reversible formations dissipate ‘ $KT \ln 2$ ’ energy per bit which can be ignored in reversible formation. But, read disturb at low write current is a major issue of MTJ MRAM due to the same path of read/write current path. In this paper a three dimension reversible “Read Disturb Detection Circuit” is formed by nano electronics ‘QCA’ technology which bit-wise follows the control logic of read-disturb-detection technique and the same figure also simulated by ‘VHDL’ coding in Xilinx software to prove the advantages of ‘QCA’ technology contrast to Xilinx. This paper also focuses on the correspondence between change of temperature and supply power.

Keywords : Magnetic Tunnel Junction, Quantum cell, Reversible Logic, Read Disturb Detection.

I. INTRODUCTION

QCA or Quantum Dot cellular Automata are used to replace the CMOS technology in a proper alternative method because of its faster switching possibility,

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less area, higher clock-frequency (in THz) and low power-consumption and we can access more bits in a single time by applying QCA technology compare to CMOS technology [1]. A portable high speed reversible memory formation with less heat dissipation and occupied area is introduced in this paper. Reversible Devices should be logically and physically reversible by making the input and outputs uniquely recoverable from each other and can be properly run in backward direction respectively [2]. We can realize arbitrary functions (non-symmetric) using repeated variables. Due to the high leakage problem and also the scalability problem the SRAM, DRAM are replaced by nonvolatile Magneto resistive RAM with spin transfer torque technique to get more flexibility, low power dissipation, more endurance, more speed and less occupied area. MRAM stores data (using electric charge) in magnetic region with uniform magnetization. In the Spintronic technique a torque is applied to the chargeable-layer by the spin of electron flow and this phenomena takes place in a magnetic tunnel junction (‘MTJ’) which mainly works for electron-tunneling and this is a quantum-phenomena. In this magnetic process the memory uses a pair of ‘ferromagnetic metal plates’ and a thin layer of an insulating-material separates them and the orientation of the plates (parallel or not) is determined by ‘1’ and ‘0’ binary bits. MTJ MRAM faces some challenges. Mainly it faces problems due to read disturb at low current [3]. This paper presents a multiple layer or 3-D reversible MTJ or magnetic tunnel junction structure by ‘QCA’ technology which bit-wise follows the control logic of Spintronic process with the application of the “read disturb detection technique”.

II. BACKGROUND

This paper presents the applied cell-design of QCA (fig.1), the different cell designs (fig.2) and the different wiring process of QCA (fig.3 and fig.4). This paper also presents the simulator-parameters in table.1.

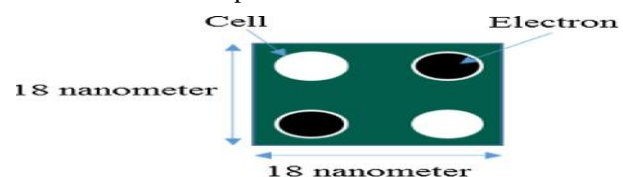


Fig.1. A cell-design of QCA

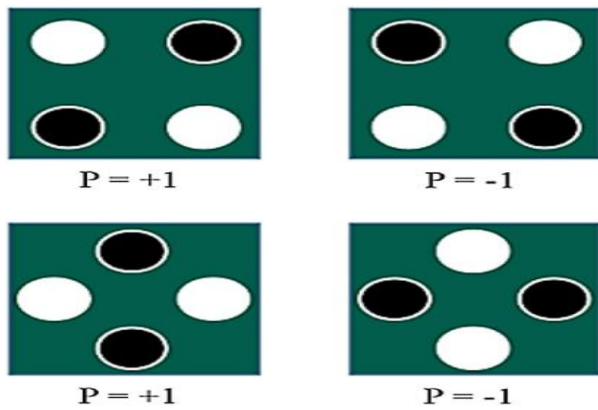


Fig.2. 90-degree wire structure (upper part) and 45-degree wire structure (lower part) of a QCA-cell.

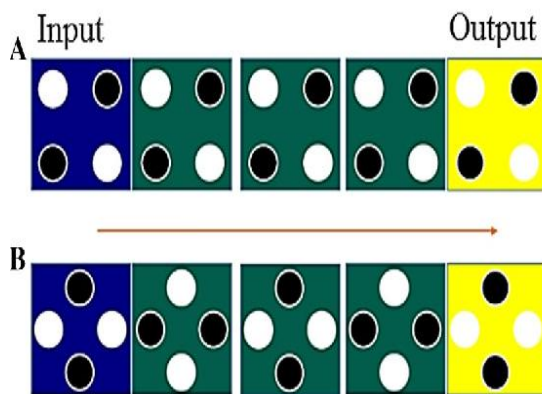


Fig.3. Wiring process of 90-degree (upper part) and 45-degree (lower part) quantum cell.

Basic reversible gates [4] (Reversible-NOT and F-Gate) and ‘five input’ majority gates are used in this paper to design reversible RAM and MRAM formation. The equation of applied ‘five input’ majority gate is:

$$M(A, 1, B, C, D) = A(B+C+D) + BC + BD + CD$$

Table- I: Table of simulation-parameters [2019]

Parameters are used	Values of the parameters
Cell-Size	324 nm ²
Distance between layers	11.5 nm
Dot-Diameter	5 nm
Clock-Area (lower)	3.800000e ⁻⁰²³
Clock-Area (Upper)	9.800000e ⁻⁰²²
Area of clock-shift	0
Clock-Amplitude-Factor	2
Permittivity (relative)	12.90
Sample-Numbers	50,000
Convergence-tolerance	0.001
Maximum interaction of one sample	100

III. RELATED WORKS

Some related works in 2018-19 are summarized in this part. In paper [5] an SOC feature was presented using 180 nm CMOS/200 nm MTJ MRAM and required area, time and energy of this design was 23 mm², 4.15 ns and 98.7 no respectively. In the paper [6] “1 Mb pe STT-MRAM” was

designed using “28 nm FD-SOI-CMOS” technology and here the write latency was 10 ns and required energy 3pJ. Paper [7] has given a brief discussion about the “MgO-based MTJ” materials and in paper [8] a “1T1R STT MRAM” was designed using “28 nm” technology with 0.214 mm² area, 20 ns writing speed and 3.6 mW power consumption. The operation of MTJ was represented through Boolean function in the paper [9] using “HieIM” with 21.8 μm² area and 3.2 no energy. Here 1620 cycles (delay) required to access the data. Three different designs of MRAM such as “STT MRAM”, “SOT MRAM” and “VC MRAM” have been compared in paper [10] and presented that the “STT MRAM” gives best solution to reduce the area (70-100 F² cell-size), delay and power consumption. Paper [11] presented a “512 KB STT MRAM” cache memory using 20 nm technology node. The ‘SNR’ value of “STT MRAM” (6 dB - 16 dB) was given in paper [12] and paper [13] presented the stiffness constant of “MRAM” (26.6 pJ/m for 425°C temperature) using “MgO / Fecal based MTJ”. Paper [14] calculated the size of heat-effect of Spintronic-device which was 300 n J/ Vm and the stability-factor was above 60 of the same technology [15]. The paper [16] accorded the same stability of “STT MRAM” for 4 nm diameter and 300 K temperature using “10 nm” node. The “pMTJ MRAM” design was formed in [17] where 66% TMR was changed. “MRAM” using “22 FFL FinFET Technology” was designed in paper [18] for high quality performance and it can work -40°C to 125°C temperature range with 0.048 μm² area and the required time (8ns for 0.6 V) was given in paper [19]. A “Quad Interface MTJ” was designed in [20] using “1-X” technology by applying an extra MgO layer (90 nm diameter) for getting low power-consumption. In the paper [21] the MTJs were integrated with CMOS for high-density (over 100 Mb) Spintronic (“STT”) memory-design. A “6T-STT MRAM” with 400 mW powers and 45 ns delay was formed in the paper [22] using “500 x” performance for 1 GB density and [23] presented an “MRAM” with 50 nm diameter. [24] applied a fast “gem 5” simulation on “MRAM” and “DRAM” and manifested that we can replace the other memories using magnetic-RAM to reduce power consumption up to ‘8%’ and ‘27%’ at the cost of ‘2x’ the area with 10.4 ns time-delay.

IV. THE PROPOSED METHOD

In the paper [25] the Schematic circuit of memory cell and the irreversible QCA design of ‘RAM’ cell are presented which are manifested here in fig.4 and 5 respectively. This paper presents the same circuit using reversible logic (“reversible NAND” gate)[26] to reduce the cell number from 88 to 41, occupied-area from 0.08 μm² to 0.036 μm², required clock-zones from 4 to 2 and delay from 1.5 clocks to 1 clock-cycle, which is presented in fig.6.

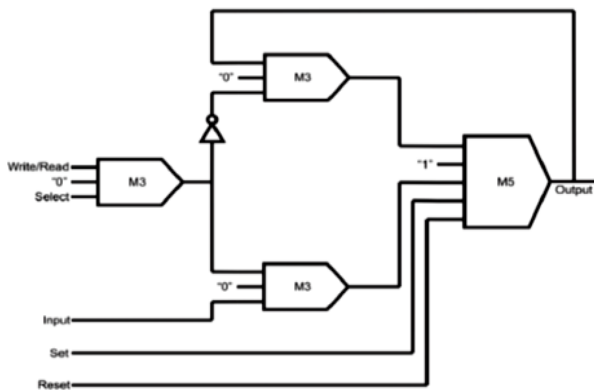


Fig. 4. Schematic Diagram of Memory Cell [25].

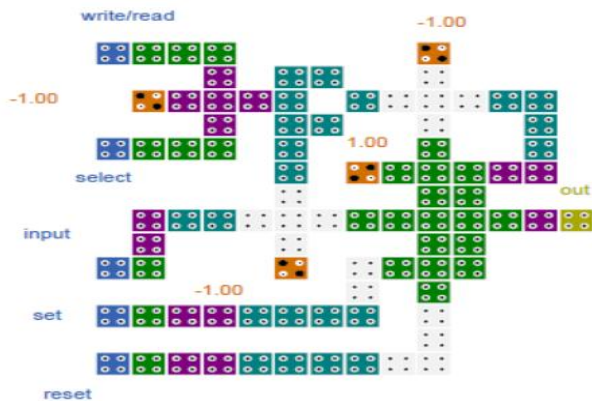


Fig.5. Irreversible QCA Design of RAM [25].

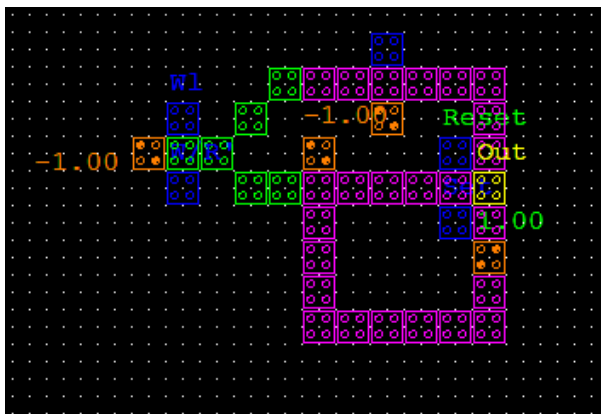


Fig.6. Proposed Reversible Random Access Memory.

The same logic-design is simulated through 'VHDL' code in 'Xilinx' and the compared outcomes are enlisted in table-II. Today's world is widely using 'MTJ MRAM' technology which is a modern replacement of other RAM-cells. The logical representation of magnetic cells can be formed by using a three-input majority gate and an inverter gate one after another [27] and if the three input majority gate is replaced by a five input majority, the previous structure works as a "XOR / XNOR" MTJ logic circuit. This paper suggests a reversible control circuit of word-line and input-line selection of magneto resistive RAM structure, which is formed by QCA technology (fig. 7). In fig. 7 the three inputs A, B and C presents the word-line, select-line and input-line respectively. If the A is one and Bit zero then output Q read the same bit pattern of C and if A is one and Bit also one then the Q presents inverting output of C. In this figure the

Q' gives the 'XOR' output of B and C and Q'' is the representation of input A.

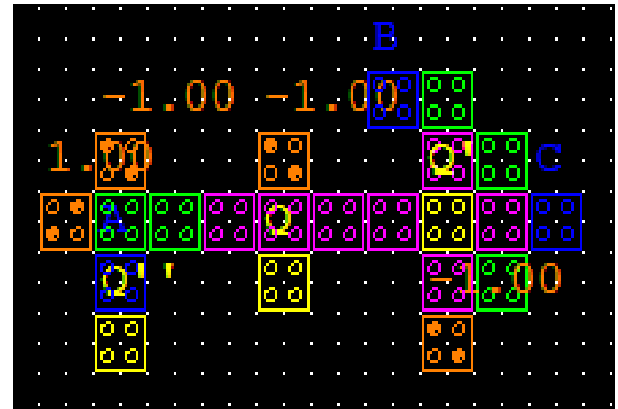


Fig.7. Reversible control circuit of MRAM.

The write-current of "STT MRAM" is 5 to 10 times higher than the read-current. So, at the time of read to write (when a flip of 'bit' cell is required) the magnetic disturbances in 'MTJ' take place. This is the main reason of read-disturb in 'MRAM'. This paper presents a three dimension reversible read disturb detection control circuit by using quantum-cells and the same figure also deigned through 'VHDL' coding in 'Xilinx' and the advancement of 'QCA' technology contrast to 'Xilinx'.

Table- II: Compared outcomes between 'Xilinx' and 'QCA Designer'.

Outcomes	In 'Xilinx'	In 'QCA Designer'
Area	25 IOB	0.036 μm^2
Latency	8.752 ns	1 clock-cycle
Power	0.204 W	0.03 W for 0.7 E_k

This paper shows the block-representation of F-Gate which is applied as a reversible gate in this design in fig. 8, where

$$P = W/l$$

$$Q = \text{in}$$

$$\text{Out} = W/l. (\sim \text{in}). \text{rl}$$

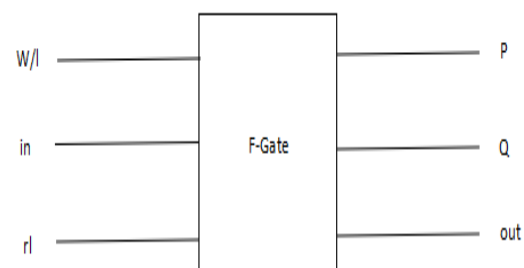


Fig.8. Reversible F-Gate.

The circuit-design of control-logic of MTJ with read-disturb-detection process and the truth-table [3] are presented here in fig. 9 and table- III respectively.

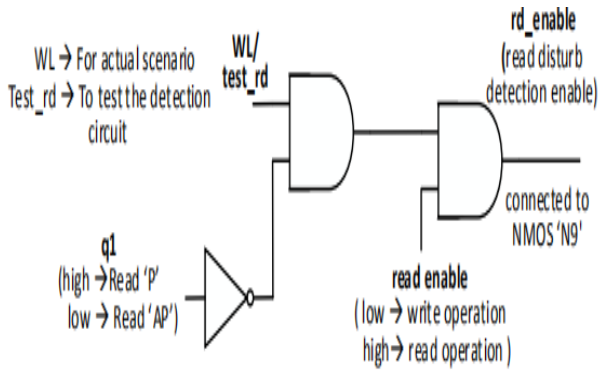


Fig.9. Circuit-Diagram of control logic of read-disturb-detection [3].

Table- III: Truth-table of control logic of MTJ with read-disturb-detection [3].

read enable	q1	WL/test_rd	rd_enable
0	X	X	0
1	1	X	0
1	0	0	0
1	0	1	1

The normal reversible formation (required 2 clock-zones) and multilayer or 3-D formation (required 1 clock-zone) of the above circuit and also the inverting-outcomes are proposed in this paper which are presented in fig. 10, 11, 12 and 13 respectively and the 'RTL' and 'Technology' schematic of the above figure (synthesized in 'Xilinx') are presented in fig.14 and 15 respectively. The schematic figures properly shows the logical representation of the proposed 'MTJ' design and the logic-diagrams, truth-tables and k-map of different circuits which are used in this proposed 'MTJ' circuit can be obtained by the technology schematic.

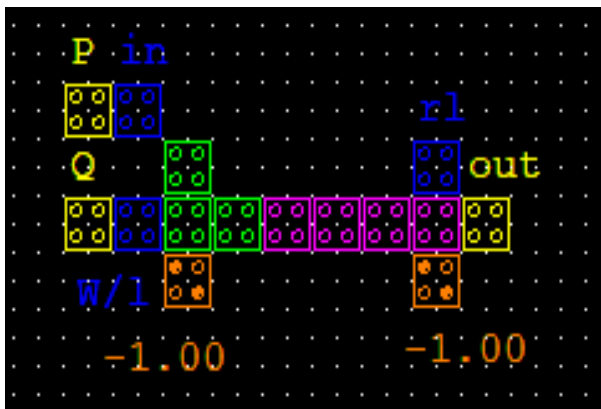


Fig.10. Reversible formation of MTJ control logic with read-disturb-detection using 'QCA'.

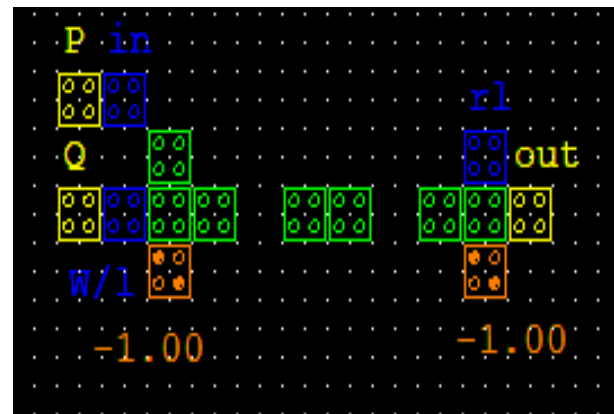


Fig.11. 3-D Reversible formation of MTJ control logic with read-disturb-detection using 'QCA'.

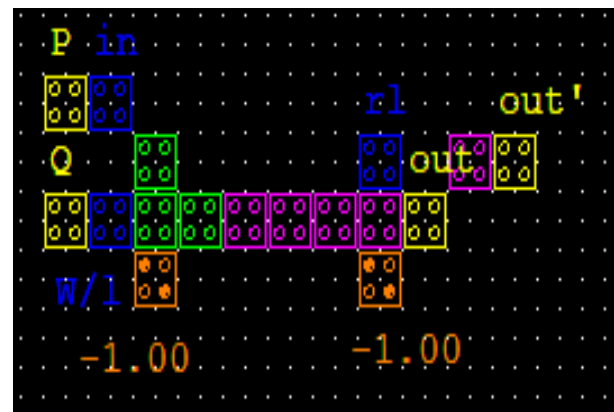


Fig.12. Reversible formation of control logic of MTJ with read-disturb-detection and inverting output using 'QCA'.

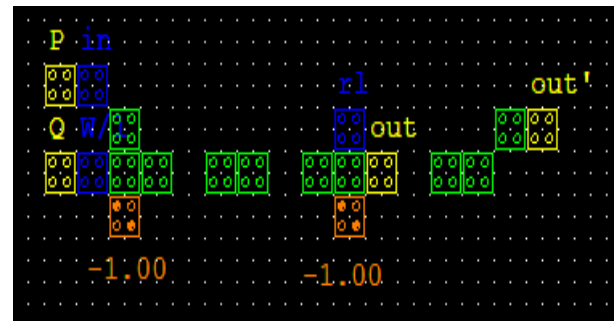


Fig.13. 3-D Reversible formation of control logic of MTJ with read-disturb-detection and inverting output using 'QCA'.

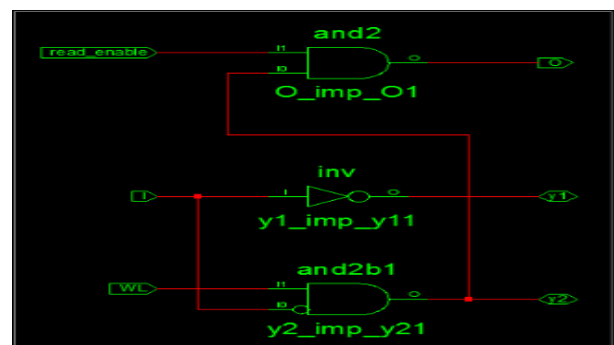


Fig.14. 'RTL' Schematic of MTJ control logic with read-disturb-detection using 'Xilinx'.

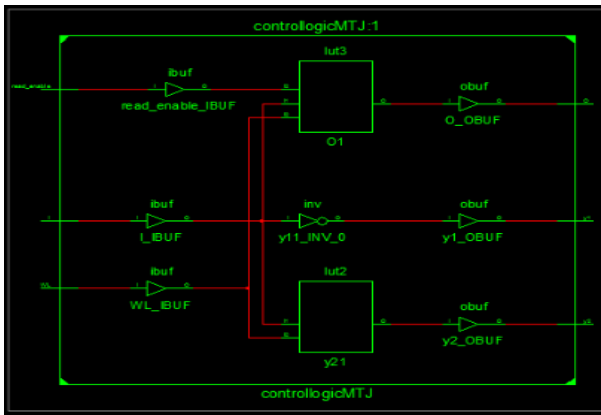


Fig.15. 'Technology' Schematic of MTJ control logic with read-disturb-detection using 'Xilinx'.

V. SIMULATION RESULTS AND COMPARISON

The simulated result of reversible 'RAM' and the reversible control circuit of word line and input line selection of magneto resistive random access memory are presented in fig. 16 and fig. 17 respectively. The outcomes of fig. 17 follows table IV. This research work also shows the outcome of simulated 3-D reversible read-disturb-detection circuit of 'STT MRAM' formed by 'QCA' technology with and without changing the clock-zone in fig. 18 and 19 respectively.

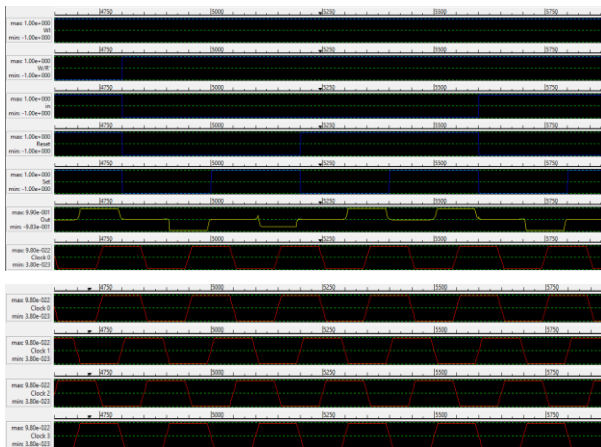


Fig.16. Simulated result of Reversible 'RAM' using 'QCA'.

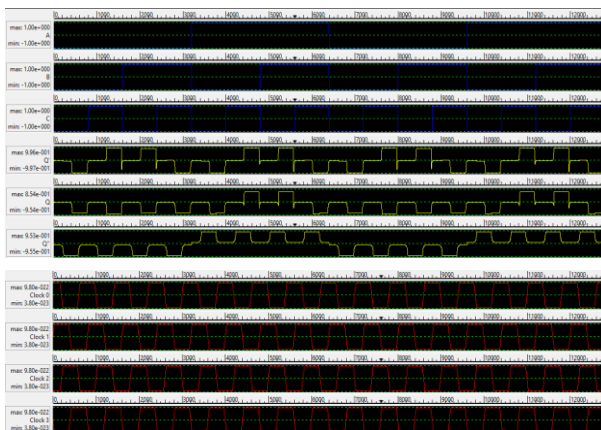


Fig.17. Simulated result of Reversible control circuit of word-line and input-line selection of 'MRAM' using 'QCA'.



Fig.18. Simulated Result of 3-D Reversible control logic of MTJ with read-disturb-detection using 'QCA'.

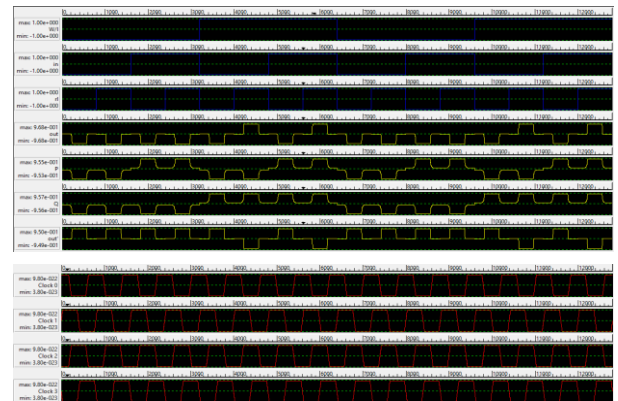


Fig.19. Simulated Result of Reversible control logic of MTJ with read-disturb-detection using 'QCA' without changing the clock-zone.

Table- V represents the compared outcomes of different proposed structures formed in different technology such as, "45 nm CMOS Technology"(2018), "28 nm FDSOI"(2019), "QCA Designer Technology with 3-D reversible logic" and "Xilinx Software". The correspondence between ambient temperature and power consumption and also the junction temperature and supply power are presented in this paper through the fig. 20 and 21.

Table- IV: The bit-wise representation of proposed reversible control circuit of MRAM

Designs	Area	Delay	Leakage Power
"45 nm CMOS" (2018)	5.871 mm ²	1.93 ns	730 mW
"28 nm FDSOI" (2019)	0.036 μm ²	10 ns (100 MHz max)	352 μW
"Xilinx"	6 IOB	6.236 ns	203 mW
"QCA Designer"	0.01 μm ²	0.5 clock-cycles (Frequency in THz)	0.008μW for 0.7 E _k

Table-V: Table of compared outcomes of different proposed structures formed in different technology

Word line	Select line	Input line	Q'' = Word line	Q' = XOR (Select line and Input line)	Q = Q' AND Word line
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	0	0

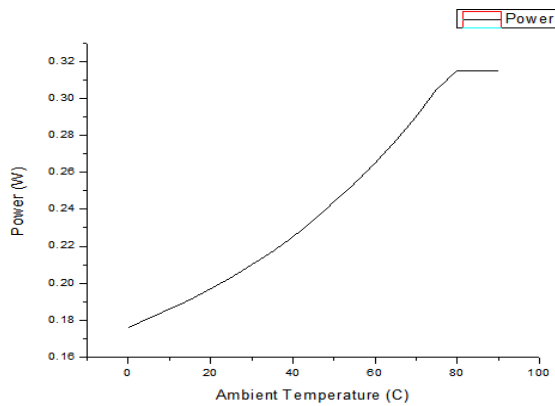


Fig.20. Graph of ambient temperature vs. power consumption.

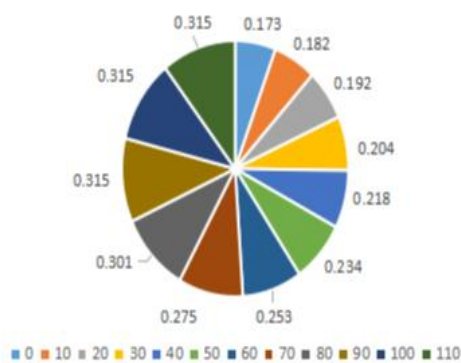


Fig.21. Pie-Chart of junction temperature (0°C - 110°C) vs. supply power.

VI. CONCLUSION

The new designs of reversible ‘RAM’ and multilayer reversible control logic of ‘MTJ’ (in ‘STT MRAM’) with ‘read-disturb-detection’ process is presented in our paper by using ‘QCA-designer’. These proposed formations give better response to reduce the number of required cells, area ($0.01 \mu\text{m}^2$), delay (0.5 clock cycles) and power ($0.008 \mu\text{W}$) than other previously suggested designs and also this paper presents a comparison of area, delay, power with reversibility process between the circuits formed by ‘QCA-designer’ and the same circuits implemented through ‘Xilinx’ software (using ‘VHDL’ code). This paper also shows the relation between ambient temperature and power consumption and between junction temperature and supply power through graph and pie-chart. The exponential

increment of the total power of the suggested device with the room-temperature increment are clearly represented here through a graphical representation and it is also shows that after “80 degree C” the increment of power with the increment of room-temperature is stopped. In future we can try to reduce the area, energy and number of the garbage-outputs by reducing the cell-size, dot-diameter and by applying new reversible-gates of the proposed figures and also we can try to improve the fault tolerance and reversibility of the formations. This proposed design is required to fabricate for hardware implementation which is required for proper real-world application.

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