International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-2, December 2019

# Modified Cascaded Inverter using ANFIS Controller with Reduced Number of Switches

**Kola Muralikumar, Ponnambalam. P**

***Abstract*: In this paper, an Adaptive Neuro Fuzzy Inference System (ANFIS) is proposed to the multilevel inverter to eliminate the Total Harmonic Distortions (THD) with a modified cascaded inverter. This method prohibits the variations presents in the output voltage of the modified cascaded inverter. The work is directed to prove that the importance of ANFIS is integrated learning for alteration of learning content affording to learners desires. The concert of the ANFIS model was calculated by means of standard error quantities which shows the ideal setting needed for better certainty. The MATLAB Simulink performance point out that it is affordable and easy to implement the performance of the ANFIS process. The study of different modified cascaded inverter consisting of five-level, seven-level, and nine- level is carried out for evaluating the THD with ANFIS controller and without ANFIS controller is implemented. The learning outcomes are based on the study of various system settings; it demonstrates the usability of the m-learning application. However, it must be noted that the number of inputs increased being considered by the model increases the system response time of the system.***

***Keywords : Multilevel Inverters, Cascaded Multilevel Inverter, Adaptive Neuro Fuzzy Inference System, Total Harmonic Distortion, Root Mean Square Value.***

## I. INTRODUCTION

Multilevel inverter plays an important role in high power and medium voltage applications. The concept behind the multilevel inverter can harvest more than two levels at its output and provides more benefits like improved output voltage spectrum [1]. Particularly these multilevel inverter includes its ability to synthesize at higher DC voltages using series-connected semiconductor device. Various multilevel inverter topologies are introduced in 1980 such as neutral point-clamped (NPC) or diode- clamped technology [2], in the 1990s the new topologies were introduced. Some of the important topologies are NPC multilevel inverter, flying-capacitor multilevel inverter, and cascaded H-bridge multilevel inverter. However, due to simple construction features and other advantages, the NPC topology is widely used [3].

**Revised Manuscript Received on December 30, 2019.**
***** Correspondence Author
**Kola Muralikumar**, School of Electrical Engineering, Vellore Institute of Technology, Vellore, Tamilnadu, India, 632014. Email: kolamuralikumar@gamail.com
**Ponnambalam.P***, School of Electrical Engineering, Vellore Institute of Technology, Vellore, Tamilnadu, India, 632014. Email: p.ponnambalam@gamail.com

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC-BY-NC-ND license http://creativecommons.org/licenses/by-nc-nd/4.0/

In multilevel inverters, as the switching has a number of smaller voltages, the wild deviation in voltage is slighter. In additional, fundamental switching frequency will also result in the decreasing these voltage changes that arise per fundamental cycle [4]. However, harmonic elimination is the main concern for multilevel inverters. The use of multilevel inverters results in a better approximation to a sinusoidal waveform because of the increased number of dc voltages. These increased the number of dc voltages allows more harmonic contents to be eliminated [5].

The Total Harmonic Distortion is relatively high for a conventional two-level inverter which generates synchronization problem with the voltage and reduces the life time of the electrical machine [6]. By using the filter circuit the problem can be solved on the inverter output which complicates the implementation and increases the cost. In the multilevel inverter, the modified cascaded inverter can mitigate this problem to produce a better performance of the output voltage with less THD without using any bulk filter. By using suitable topology, the THD can be reduced significantly [7]-[12].

The modified cascaded inverter for five-level, seven-level and nine-level with switching pattern for different level and corresponding results are detailed in section 2. The ANFIS controller analysis for the different modified cascaded inverter and corresponding results are illustrated in section 3. Analysis of step response for different levels of the cascaded inverter is calculated for each parameter in section 4. THD comparison for different levels of the cascaded inverter with ANFIS controller and without ANFIS controller is differentiated in section 5. The inference is presented in section 6.

## II. MODIFIED CASCADED INVERTER

In this section, the modified cascaded inverter for five-level, seven-level, and nine-level is simulated using MATLAB Simulink. In this configurations Multi carrier based Pulse Width Modulation (PWM) technique is used to produce the converter circuit for triggering pulses. The hybridization of phase shifted and level shifted PWM is a multi-carrier based PWM technique. This PWM technique gives the multi-level inverter self-balancing property [7]-[12].

### A. Five-Level modified Cascaded Inverter

The five-level modified cascaded inverter topology is demonstrated in Fig.1. This configuration of the modified cascaded inverter has a positive

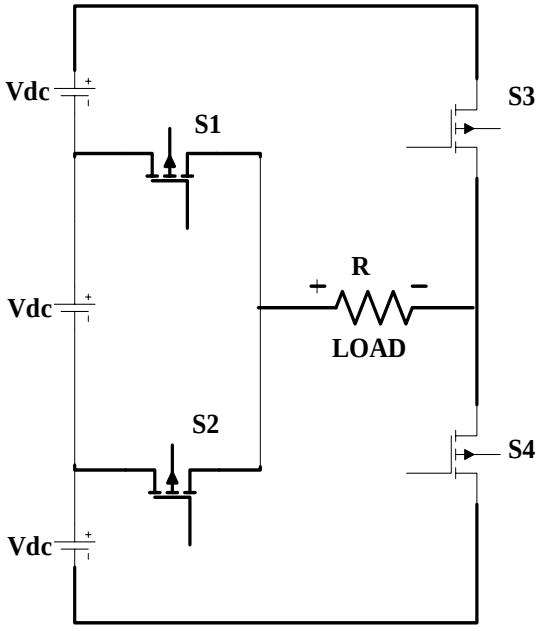


**Fig. 1.Circuit configuration for Five-level modified cascaded inverter.**

**Table- I: Switching pattern for five-level inverter**

| Switching Pattern | | | | Output Voltage |
|---|---|---|---|---|
| *S1* | *S2* | *S3* | *S4* | |
| OFF | ON | OFF | ON | +Vdc |
| ON | OFF | OFF | ON | +2Vdc |
| OFF | OFF | OFF | OFF | 0 |
| ON | OFF | ON | OFF | -Vdc |
| OFF | ON | ON | OFF | -2Vdc |

cluster and negative cluster. The positive cluster is conducting for giving positive waveform through the load and the sum of voltage level Vdc increases with increase in the switches. In the circuit configuration, when the switches (S2, S4) is in switched on condition and (S1, S3) is switched off, the output voltage +Vdc is generated. When the switches (S1, S4) is in switched on condition and (S2, S3) is switched off, the output voltage +2Vdc is generated. When all of the switches (S1, S2, S3, and S4) is switched off, the output voltage +0Vdc is generated. When the switches (S1, S3) is in switched on condition and (S2, S4) is switched off, the output voltage -Vdc is generated. When the switches (S2, S3) is in switched on condition and (S1, S4) is switched off, the output voltage -2Vdc is generated. The switching pattern of five-level modified cascaded inverter is as shown in Table. I. In this circuit configuration, the input voltage for each source is 100 V. Then the output voltage across the load is 200 V. The output voltage through the load is illustrated in Fig.2. The fast Fourier transform (FFT) analysis of five- level modified cascaded inverter is illustrated in below fig .3. From the FFT, the THD value is 17.55%.

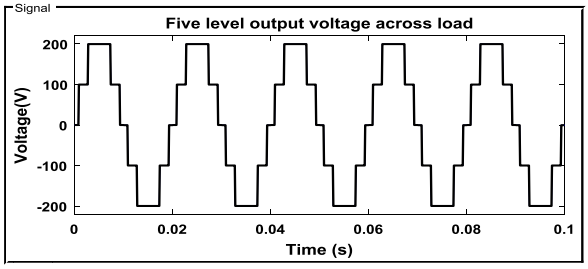


**Fig. 2.Output voltage through the load for Five-level Cascaded inverter**

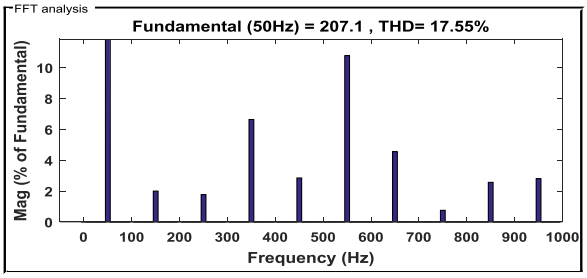


**Fig. 3.FFT analysis for Five-level Cascaded inverter**

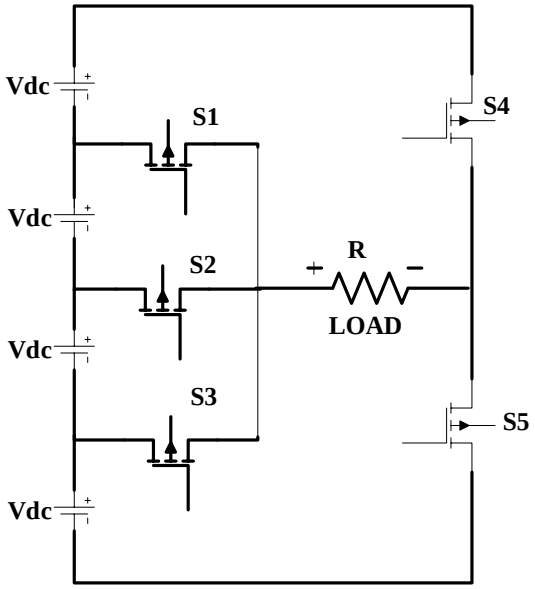


**Fig. 4.Circuit configuration for Seven-level modified cascaded inverter.**

### B. Seven-Level modified Cascaded Inverter

The Seven-level modified cascaded inverter topology is demonstrated in Fig.4. This configuration of the modified cascaded inverter has a positive cluster and negative cluster. The positive cluster is conducting for giving positive waveform across the load and the number of voltage level Vdc increases with increase in the switches. In the circuit configuration, the output voltage +Vdc is produced when the switches (S3, S5) is in turn on and (S1, S2, S4) is switched off. When the switches (S2, S5) is in turn on condition and (S1, S3, S4) is switched off, the output voltage +2Vdc is generated. When the switches (S1, S5) is in turn on condition and (S2, S3, S4) is switched off, the output voltage +3Vdc is generated. When all the switches

**Table- II: Switching pattern for Seven-level inverter**

| Switching Pattern | | | | | Output Voltage |
|---|---|---|---|---|---|
| *S1* | *S2* | *S3* | *S4* | *S5* | |
| OFF | OFF | ON | OFF | ON | +Vdc |
| OFF | ON | OFF | OFF | ON | +2Vdc |
| ON | OFF | OFF | OFF | ON | +3Vdc |
| OFF | OFF | OFF | OFF | OFF | 0 |
| ON | OFF | OFF | ON | OFF | -Vdc |
| OFF | ON | OFF | ON | OFF | -2Vdc |
| OFF | OFF | ON | ON | OFF | -3Vdc |

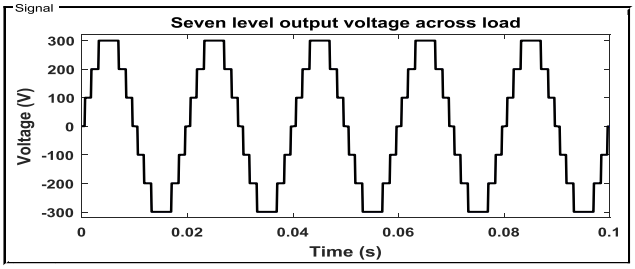


**Fig. 5.Output voltage across the load for Seven-level Cascaded inverter**

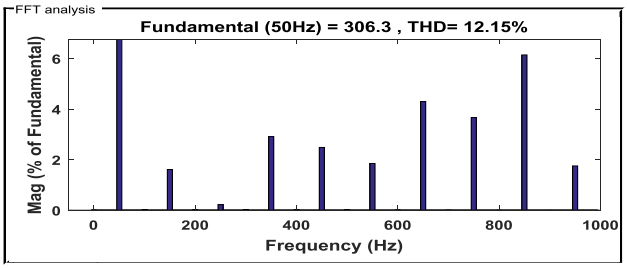


**Fig. 6.FFT analysis for Seven-level Cascaded inverter**

(S1, S2, S3, S4, and S5) is switched off, the output voltage +0Vdc is generated. The output voltage –Vdc is generated when the switches (S1, S4) are switched on and (S2, S3, S5) is switched off. The output voltage -2Vdc is generated when the switches (S3, S4) are switched on condition and (S1, S2, S5) are switched off. The output voltage -3Vdc is generated. The switching pattern of seven-level modified cascaded inverter is as shown in Table.II. In this circuit configuration, the input voltage for each source is 100V. Then the output voltage through the load is 300V. The output voltage across the load is illustrated in Fig.5. The fast Fourier transform (FFT) analysis of seven-level modified cascaded inverter is shown in below Fig .6. From the FFT, the THD value is 12.15%.

### C. Nine-Level modified Cascaded Inverter

The Nine-level modified cascaded inverter topology is demonstrated in Fig.7. This configuration of the modified cascaded inverter has a positive cluster and negative cluster. The positive cluster is conducting for giving positive

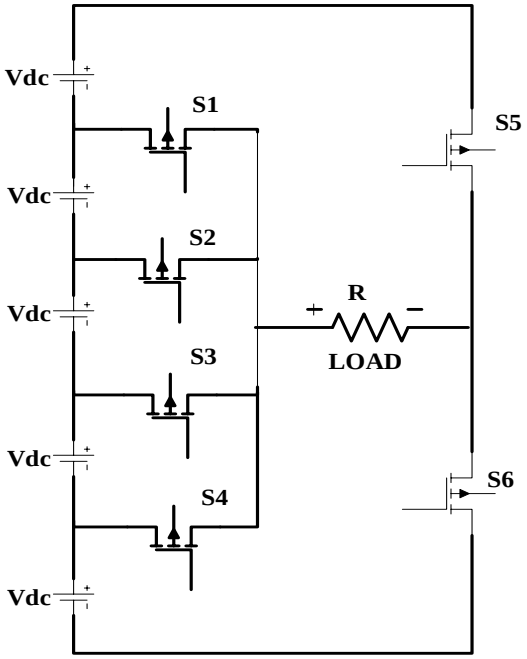


**Fig. 7.Circuit configuration for Nine-level modified cascaded inverter.**

**Table- III: Switching pattern for Seven-level inverter**

| Switching Pattern | | | | | | Output Voltage |
|---|---|---|---|---|---|---|
| *S1* | *S2* | *S3* | *S4* | *S5* | *S6* | |
| OFF | OFF | OFF | ON | OFF | ON | +Vdc |
| OFF | OFF | ON | OFF | OFF | ON | +2Vdc |
| OFF | ON | OFF | OFF | OFF | ON | +3Vdc |
| ON | OFF | OFF | OFF | OFF | ON | +4Vdc |
| OFF | OFF | OFF | OFF | OFF | OFF | 0 |
| ON | OFF | OFF | OFF | ON | OFF | -Vdc |
| OFF | ON | OFF | OFF | ON | OFF | -2Vdc |
| OFF | OFF | ON | OFF | ON | OFF | -3Vdc |
| OFF | OFF | OFF | ON | ON | OFF | -4Vdc |

waveform throughout the load and the sum of voltage level Vdc increases with increase in the switches. In the circuit configuration, when the switches (S4, S6) is in turn on condition and (S1, S2, S3, S5) is turned off, the output voltage +Vdc is generated. When the switches (S3, S6) is in turn on condition and (S1, S2, S4, S5) is turned off, the output voltage +2Vdc is generated. When the switches (S2, S6) is in turn on condition and (S1, S3, S4, S5) is turned off, the output voltage +3Vdc is generated. The output voltage + 4Vdc is generated when the switches (S1, S6) are turned on condition and (S2, S3, S4, S5) are switched off. The output voltage + 0Vdc is generated when all switches (S1, S2, S3, S4, S5, and s6) are switched off. When the switches (S1, S5) is in turn on condition and (S2, S3, S4, S6) is switched off, the output voltage -1Vdc is generated.

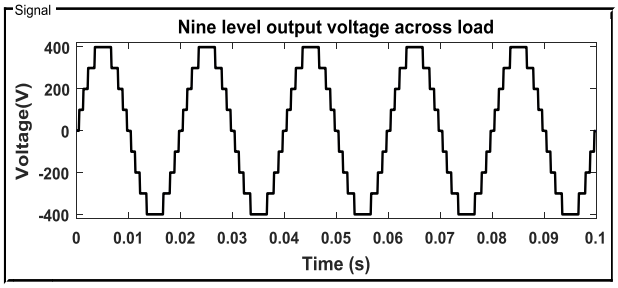


**Fig. 8.Output voltage across the load for Nine-level Cascaded inverter**

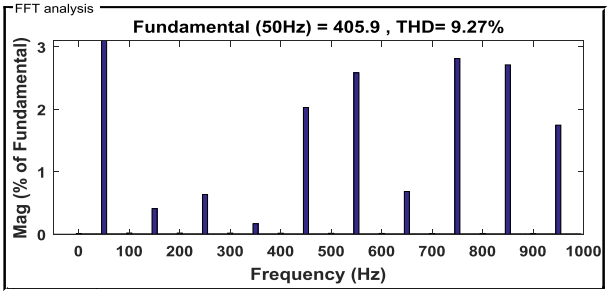


**Fig. 9.FFT analysis for Seven-level Cascaded inverter**

generated. When the switches (S2, S5) is in turn on condition and (S1, S3, S4, S6) is turned off, the output voltage -2Vdc is generated. When the switches (S3, S5) is in turn on condition and (S1, S2, S4, S6) is turned off, the output voltage -3Vdc is generated. When the switches (S4, S5) is in turn on condition and (S1, S2, S3, S6) is switched off, the output voltage -4Vdc is generated.

The switching pattern of five-level modified cascaded inverter is as shown in Table.III. In this circuit configuration, the input voltage for each source is 100V. Then the output voltage across the load is 400V. The output voltage across the load is illustrated in Fig.8. The fast Fourier transform (FFT) analysis of seven-level modified cascaded inverter is shown in below Fig .9. From the FFT, the THD value is 9.27%.

## III. ANFIS CONTROLLER FOR MODIFIED CASCADED INVERTER

Adaptive Network Fuzzy Inference System (ANFIS) architecture is visualized in fig. 1 is a fusion arrangement combining the learning abilities of Artificial Neural Network (ANN) and outstanding knowledge demonstration and inference abilities of fuzzy logic (Jang 1993) that have the skills to Self-modify the role of membership to achieve preferred output [13]. An adaptive network can be assumed to understand the fuzzy inference system which incorporates virtually all breeds of neural network models. ANFIS consumes the hybrid-learning rule and accomplishes intricate schemes for decision-making or diagnosis. ANFIS has been established as an important tool for tuning Fuzzy inference systems of membership functions. [14].

ANFIS is a humble data learning method that customs a fuzzy inference system ideal to convert an agreed effort into objective productivity. This prediction involves membership functions, fuzzy logic operators, and if-then rules. On the other hand, two types of fuzzy systems are generally identified as the Mamdani and Sugeno models [15].

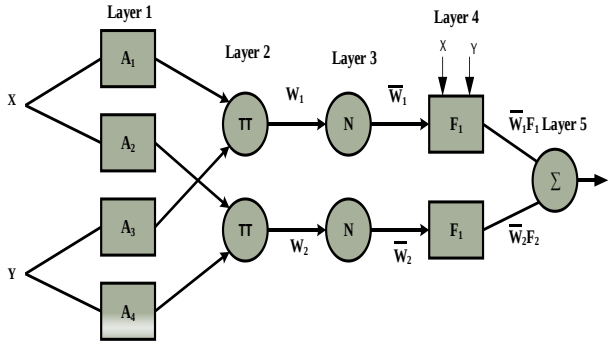


**Fig. 10. ANFIS Architechre**

There are five focal processing periods in ANFIS operation consist of input fuzzification, fuzzy operator application, application technique, output accumulation, and defuzzification.

ANFIS exploits "Depiction of aforementioned knowledge interested in a fixed limitations in network topology to moderate the optimization rifle space", since "an edition of back propagation to the organized network to mechanize Fuzzy controller parametric tuning" and Fuzzy Systems to enhance the performance of Neural Networks. The fuzzy controller's development task is to recognize and function well in the presence of distractions and uncertainties [16]. ANFIS batch learning technique is used to model membership functions, which leads to tuning a FIS based on a set of input-output data pairs with a back propagation algorithm. ANFIS is typically a multilayer feedforward network where each node performs a specific function (node function) on incoming signals. [12]. Two inputs ' x ' and ' y ' and one output ' z ' are considered for simplicity. Suppose there might be two fuzzy if-then rules of Takagi and Sugeno type in the rule base (Jang 1993):

Rule 1: IF x is A1 and y is B1 THEN f1=P1x+Q1y+R1
Rule 2: IF x is A2 and y is B2 THEN f2=P2x+Q2y+R2

Layer-1:

- $O_{1,i}$ is the output of the $i^{th}$ node of the layer-1.
- Every node is an adaptive node with a node function in this layer

$$O_{1,i} = \mu A_i(x) \quad \text{for i = 1, 2, or}$$
$$O_{1,i} = \mu B_{i-2}(x) \quad \text{for i = 3, 4}$$

- x (or y) is the input node I and the linguistic label $A_i$ (or $B_{i-2}$) associated with this node
- Therefore $O_{l,i}$ = is a fuzzy set's membership grade (A1, A2, B1, B2).
- Typical membership function:

$$\mu_A(x) = \frac{1}{1+\left|\frac{x-c_i}{a_i}\right| 2b_i}$$

- The parameter set are $a_i$, $b_i$, $c_i$.
- Parameters are defined to as premise parameters..

Layer-2:

- Every node is fixed whose output (representing firing strength 0 is the quality of the inputs:

$$O_{2,i} = \overline{\omega_i} = \mu_{A_i}(x) \cdot \mu_{B_i}(y),\ i = 1,\ 2$$

- Each node signifies the fire strength of the rule.
- It is possible to use any other T-norm operator that executes the AND operator.

Layer-3:

- Every node in this layer is labeled as a fixed node.
- The $i^{th}$ node calculates the ratio of the $i^{th}$ rule firing strength to the sum of all rule's firing strengths.

$$O_{3,i} = \overline{\omega_i} = \frac{\omega_i}{\omega_1 + \omega_2},\ i = 1,\ 2$$

- Outputs are termed firing strengths that are standardized.

Layer-4:

- In this layer, each node I is an adaptive node with a node function:

$$O_{4,i} = \overline{\omega_i} f_i = \overline{\omega_i}(p_i x + q_i y + r_i)$$

- $\overline{\omega_i}$ is the standardized firing strength from layer-3.
- The parameter set of this node is $(p_i + q_i + r_i)$.
- These parameters are referred to as consequential.

Layer-5:

- The single node in this layer is a fixed node labeled sum, which calculates the overall output as a description of all incoming signals.

$$O_{5,i} = \sum_i \overline{\omega_i} f_i = \frac{\sum_i \omega_i f_i}{\sum_i \omega_i}$$

### A. ANFIS controller five-level modified cascaded inverter

The Fig.11. Shows the Root Mean Square (RMS) value and reference voltage value. It can be noticed from the figure that the reference voltage is initially kept as 100 V and then raised to 142 V after 6Sec. Fig.12, Output Voltage for five-level cascaded inverter with ANFIS. It could be observed that the pulse width in the initial part of the voltage is smaller (while the reference voltage is 100 V) and the pulse width rises to 142 V after 6sec to increase the output voltage. The RMS value and reference voltage value of five-level modified cascaded inverter using ANFIS controller is also obtained in Fig.11. The minimum voltage reference is kept at 100 V and it is maintained till 6sec.

### B. ANFIS controller seven-level modified cascaded inverter

The Fig13. Shows the value and reference voltage value of the Root Mean Square (RMS). From the figure, it can be noticed that the reference voltage was initially maintained as 150 V and then increased to 212 V after 6sec. Fig. 14 shows the output voltage for seven-level cascaded inverter with ANFIS. It can be noticed that the pulse width in the initial part of the voltage is lower (even though the reference voltage is 150 V) and the pulse width rises to 212 V after 6sec to increase the output voltage. The RMS value and reference voltage value of seven-level modified cascaded inverter using ANFIS controller is also obtained in Fig.13.

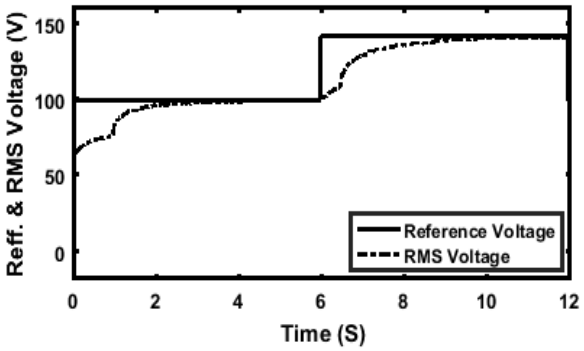


**Fig. 11. Reference and RMS output voltage for a Five-level inverter with ANFIS**

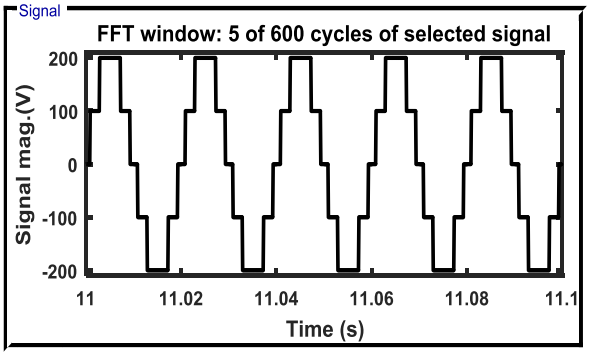


**Fig. 12. Output voltage for Five-level cascded inverter with ANFIS**

The minimum reference voltage is kept at 150 V and it is maintained till 6sec.

### C. ANFIS controller Nine-level modified cascaded inverter

The Fig.15. Shows the value of the Root Mean Square (RMS) and the reference voltage. It can be noticed from the figure that the reference voltage is initially held as 200 V and then increased to 283V after 6sec. Fig. 16 shows the output voltage for nine-level cascaded inverter with ANFIS. It could be observed that the pulse width in the initial part of the voltage is less (while the reference voltage is 200 V) and after 6sec the pulse width increases to raise the output voltage to 283V. The RMS value and reference voltage value of nine-level modified cascaded inverter using ANFIS controller is also obtained in Fig.15. The minimum reference voltage is kept at 200 V and it is maintained till 6sec.

## IV. STEP RESPONSE FOR DIFFERENT LEVELS OF CASCADED INVERTER

The step response parameters consisting with Rise Time, Settling Time, Overshoot, Peak value, Peak Time and RMS Voltage values using Adaptive Network Fuzzy Inference System (ANFIS) for five-level, seven-level, and the nine-level modified cascaded inverter is differentiated in table. IV.

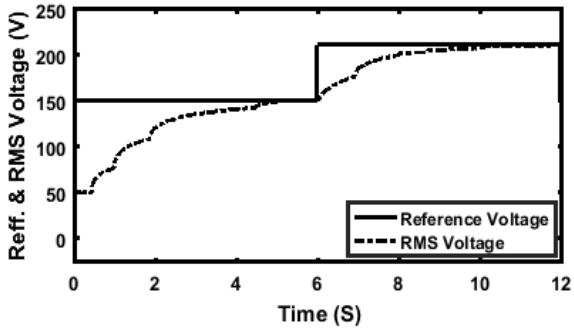


**Fig. 13. Reference and RMS output voltage for a seven-level inverter with ANFIS**

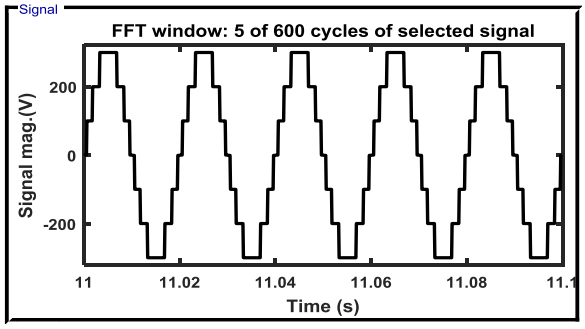


**Fig. 14. Output voltage for seven-level cascded inverter with ANFIS**

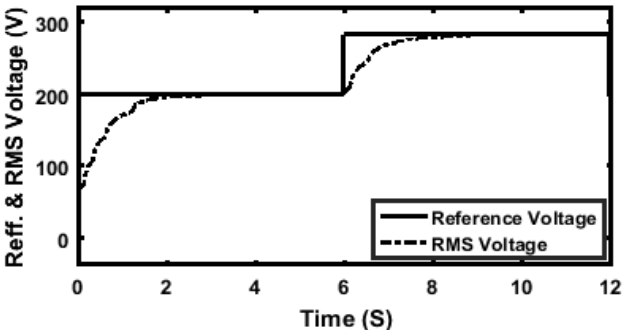


**Fig. 15. Reference and RMS output voltage for a nine-level inverter with ANFIS**

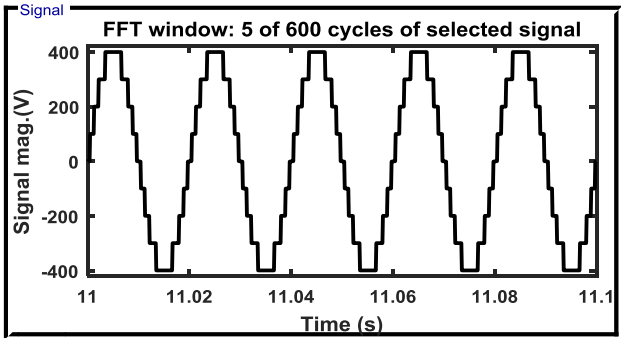


**Fig. 16. Output voltage for nine-level cascded inverter with ANFIS**

## V. THD FOR DIFFERENT LEVELS OF CASCADED INVERTER

The THD for different levels of cascaded inverter without and with ANFIS controller is illustrated in the table. V. The study of THD value without ANFIS controller is 17.55% and with ANFIS controller is 14.52% for the five-level inverter, for seven-level 12.15% of without controller and 9.66% of with controller, for nine-level 9.27% of without controller and 5.49% of with controller. From this analysis increasing the levels, THD is decreased.

**Table- IV: Step response for different levels of cascaded inverter**

| Parameter | 5-Level | 7-Level | 9-Level |
|---|---|---|---|
| Rise Time(s) | 6.9048 | 7.2192 | 6.6101 |
| Settling Time(s) | 9.7472 | 9.9177 | 7.6665 |
| Overshoot(V) | 0 | 0 | 0.0078 |
| Peak value(V) | 142.2812 | 211.5321 | 282.3222 |
| Peak Time(s) | 11.9415 | 11.9868 | 10.2327 |
| RMS Voltage(V) | 142.3 | 212 | 282.3 |

**Table- V: THD for different levels of cascaded inverter without and with ANFIS controller**

| levels | Without ANFIS controller | With ANFIS controller |
|---|---|---|
| 5-Level | 17.55% | 14.52% |
| 7-Level | 12.15% | 9.66% |
| 9-Level | 9.27% | 5.49% |

## VI. CONCLUSION

This paper described proving the significant change in the percentage of THD and a reduced number of switches through the circuit configuration of five-level, seven-level, and nine-level modified cascaded inverter. The analysis of this circuit configuration for the different modified cascaded inverter is done for both with ANFIS controller and without ANFIS controller. ANFIS controller techniques are claimed to provide better performance by the system at the inverter output voltage to eliminate the harmonics. The possibility of this method is addressed and THD results are compared for the different modified cascaded inverter. This study demonstrates the possible value of ANFIS with hybrid learning. The concert of ANFIS was calculated by means of typical error quantities which exposed the ideal setting required for better probability. In Future research, membership function type and numbers, inputs, rules, usage of epoch numbers, to refine further training samples in the ANFIS model. In the future, it can increase the possibility of emerging more effective.

## REFERENCES

1. García Franquelo, Leopoldo, et al. "The age of multilevel converters arrives." *IEEE Industrial Electronics Magazine, 2 (2), 28-39.* (2008).
2. Lai, Jih-Sheng, and Fang Zheng Peng. "Multilevel converters-a new breed of power converters." *IEEE Transactions on industry applications* 32.3 (1996): 509-517.

3. Perez MA, Bernet S, Rodriguez J, Kouro S, Lizana R. Circuit topologies, modeling, control schemes, and applications of modular multilevel converters. IEEE transactions on power electronics. 2014 Mar 5;30(1):4-17.
4. Kala P, Arora S. A comprehensive study of classical and hybrid multilevel inverter topologies for renewable energy applications. Renewable and Sustainable Energy Reviews. 2017 Sep 1;76:905-31.
5. Gupta KK, Jain S. Comprehensive review of a recently proposed multilevel inverter. IET Power Electronics. 2014 Jan 31;7(3):467-79.
6. Hasan NS, Rosmin N, Osman DA, Musta'amal AH. Reviews on multilevel converter and modulation techniques. Renewable and Sustainable Energy Reviews. 2017 Dec 1;80:163-74.
7. Gupta A. Influence of solar photovoltaic array on operation of grid-interactive fifteen-level modular multilevel converter with emphasis on power quality. Renewable and Sustainable Energy Reviews. 2017 Sep 1;76:1053-65.
8. Chandwani HB, Matnani MK. A review of modulation techniques for hybrid multilevel inverter. In2012 1st International Conference on Emerging Technology Trends in Electronics, Communication & Networking 2012 Dec 19 (pp. 1-7). IEEE.
9. Ali JS, Krishnaswamy V. An assessment of recent multilevel inverter topologies with reduced power electronics components for renewable applications. Renewable and Sustainable Energy Reviews. 2018 Feb 1;82:3379-99.
10. Paul Raj MM, Meenakshi Sundaram SS. Cascaded H-Bridge Five-Level Inverter for Grid-Connected Photovoltaic System Using Proportional–Integral Controller. Measurement and Control. 2016 Feb;49(1):33-41.
11. Sumithira TR, Nirmal Kumar A. Elimination of harmonics in multilevel inverters connected to solar photovoltaic systems using ANFIS: an experimental case study. Journal of applied research and technology. 2013 Feb;11(1):124-32.
12. Mohan TK, Mohammed SF. A neuro-fuzzy controller for multilevel renewable energy system. In2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT) 2016 Mar 3 (pp. 4120-4123). IEEE.
13. Suganthi L, Iniyan S, Samuel AA. Applications of fuzzy logic in renewable energy systems–a review. Renewable and sustainable energy reviews. 2015 Aug 1;48:585-607.
14. Buragohain M. *Adaptive network based fuzzy inference system (ANFIS) as a tool for system identification with special emphasis on training data minimization* (Doctoral dissertation).
15. Bonissone P. Adaptive neural fuzzy inference systems (ANFIS): Analysis and applications [Slides]. Class Notes. New York. 2002.
16. Karuppusamy P, Natarajan AM, Vijeyakumar KN. An adaptive neuro-fuzzy model to multilevel inverter for grid connected photovoltaic system. Journal of Circuits, Systems and Computers. 2015 Jun 13;24(05):1550066.
17. Cecati C, Ciancetta F, Siano P. A multilevel inverter for photovoltaic systems with fuzzy logic control. IEEE Transactions on Industrial Electronics. 2010 Mar 1;57(12):4115-25.
18. Jantzen J. Design of fuzzy controllers. Technical University of Denmark, Department of Automation, Bldg. 1998 Aug 19;326:362-7.

## AUTHORS PROFILE

**K.Murali Kumar,** is received his Bachelor of Technology in Electrical and Electronics Engineering from Jawaharlal Nehru Technological University Hyderabad by 2006, and Master of Technology in Power Electronics and Electrical Drives from Jawaharlal Nehru Technological University Anantapur by 2013. He is currently doing research in the field of multilevel inverters. He has published four articles in international/national journals and conferences. His area of interest includes multilevel inverters and fuzzy logic controllers.

**Dr. P. Ponnambalam,** is an Associate Professor with the Vellore Institute of Technology Vellore, India. Over the last 10 years, he completed his B.E in Electrical and Electronics Engineering from Madurai Kamaraj University by 2002, he completed his M.E in Power Electronics and Drives from Anna University Chennai by 2006. He completed his Ph.D. from Anna University Chennai by 2015, he has a good contribution towards the research in the area of Fuzzy Controllers for different multilevel inverters. He has many papers to his credit in many journal in national and international level of repute. His area of interest is on Fuzzy Controllers for power electronic applications.