

# Experimental Verification of Critical Inductance Analysis for LUO Family Converters

Deepa A, K. Sathish Kumar



**Abstract:** Our work provides an experimental investigation over critical inductance analysis (CIA) for fundamental Luo family converters (LFCs). It mainly concentrates on negative output superlift Luo converter (NOSLLC), positive output superlift Luo converter (POSLLC) and negative output boost converter (NOBC) which is carried out with proportional integral controller (PIC) so as to get a control over the LFC's output voltage. Experimental investigation is performed by selecting the critical inductance of LFCs based on average inductor current as well as inductor current repletion, and then the state-space equations of LFCs are attained using the Ziegler–Nicholas tuning method. The experimental analysis provides the researchers a detailed ride over critical inductance for LFCs converters to obtain a better voltage transfer ratio, efficiency and minimised capacitor voltage as well as inductance current ripples as compared with the traditional DC–DC converters. Therefore the performance of the LFCs using PIC is verified at different states by developing both the MATLAB/Simulink and the prototype models. The results of experimental and implementations are provided to represent the importance of the CIA of LFCs with PIC.

**Keywords:** Luo Converter, Critical Inductance Analysis, PI Controller, Continuous Conduction Mode.

## I. INTRODUCTION

Nowadays, novel DC–DC converters are being introduced rapidly, which also satisfy the major constraints such as accurate output voltage regulation, reduced ripples of capacitor voltage/inductor current, minimised size and weight, good voltage transfer gain, good transferring energy capacity with small energy loss and low cost. These types of DC–DC converter topologies are more evident for power supply in many applications such as liquid crystal display (LCD), battery charger, laptop computers, aerospace, solar power systems, defence equipment, medical equipment, traction systems with high voltage level design for DC–DC converters, power supplies, etc. [1–3]. According to theoretical explanations, the traditional DC–DC converters will reach the enhanced voltage transfer gain over a high duty cycle apart from extremely high duty cycles, in real-time applications, that is small due to significance of power semiconductor switches, AC–DC conversion diodes and capacitor's and inductor's equivalent series resistance. Taking this into account, the working of extremely large duty cycles will induce a serious reverse recovery and problems of electromagnetic interference (EMI) [4–6].

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The above-discussed problems are solved by Luo converters (LCs) [7]. The main advantages of LCs are good voltage transfer gain, reduced ripples of current/voltage, simple structure and good power capability than the conventional DC-DC converter. Based on the above-discussed problems, a voltage lift method has been efficiently utilized considering the DC-DC converter design, and in such cases three sequences of Luo converters can be subjected to the stage-by-stage output voltage increase in the arithmetic progression. The NOSLLC, POSLLC and NOBC can perform likewise with a simple configuration as they have great LC topology that converts the positive input DC voltage to the negative/positive output DC voltage. The voltage lift converters and various switching operations based on DC-DC converters have been described in many studies [7]. The modelling methods of DC-DC converters include the signal flow graph (SGF) and the state-space averaging method [9-10]. The SGF is a simple method; however, its dynamic characteristic is imperfect as large frequency elements are normalised in the model. In addition, it turns the controller inappropriate for huge-signal dynamic control in most of the classical controller methods, namely, the proportional controller (PC), PIC, the proportional integral derivative controller (PIDC), etc. Among these classical controller methods, a PIC for LCs provides good static and dynamic responses [11]. The CIA of various topologies of the conventional DC-DC converters has been reported [12]. Moreover, the proportional double integral controller, reduced order linear quadratic regulator and observer-based controller have also been reported for DC-DC converters [13–16]. From the above results, it is evidently observed that the CIA for a super lift converter and a voltage lift converter using controller has not been reported.

Therefore, in this study, it is proposed to design a PIC for CIA of LCs. The critical inductance (coil) is the value that transfers the circuit between the CCM and the DCM. Here, three fundamental topologies of LCs are selected for investigations of CIA, such as NOSLLC, POSLLC and NOBC. At first, the state-space average model for LCs is originated and then the PIC is implemented. The LC's performance utilizing a designed controller is evaluated at various working regions. The tuning of PIC constraints is evaluated by utilizing the Ziegler–Nicholas tuning technique and the parameters are implemented in an analogue platform as well as MATLAB/Simulink.

## II. OPERATION OF FUNDAMENTAL LCS

### A. Operation of a NOSLLC

The topology of the NOSLLC is displayed in Fig. 1 (a) [7].

The high-quality output voltage of NOSLLC is attained by controlling its power switch ( $Q$ ). The power circuit of the NOSLLC (see Fig. 1 (a)) consists of  $V_{in}$  as an input DC source voltage,  $Q$  as the  $n$ -channel MOSFET switch,  $D_1$  and  $D_2$  as free-wheeling diodes, capacitors  $C_1$  and  $C_o$  and inductor  $L_1$  as the energy storage components, output voltage is represented as  $V_o$  and the load resistance is represented as  $R$ . The NOSLLC expected that all the elements are supreme as well as the same converter operates in the CCM. To study the working of the NOSLLC, the circuit can be classified into 2 modes of operations, namely, the ON and OFF modes. Figs.1 (b) and (c) shows the two modes of working of NOSLLC. In the mode 1 operation, the switch  $Q$  is closed, the diode  $D_1$  conducts and  $C_1$  is energised by  $V_{in}$  in a short period of time, and also the  $C_1$  voltage is considered as a fixed value. The inductor current ( $L_1$ ),  $i_{L1}$ , increases with  $V_{in}$ . The output capacitor  $C_o$  offers the energy to the load. In the mode 1 operation, the NOSLLC network is displayed in Fig. 1 (b). In the mode 2 operation,  $Q$  is open, diode  $D_2$  conducts and therefore the  $i_{L1}$  decreases with the  $C_1$  voltage ( $V_o - V_{in}$ ) to give the energy to the output capacitor  $C_o$  and load. The NOSLLC equivalent circuit in mode 2 is exposed in Fig.1 (c). The ripple of the  $i_{L1}$  can be expressed as follows:

$$\Delta_{i_{L1}} = \frac{V_{in} kT}{L_1} = \frac{V_o - V_{in}}{L_1} (1-k)T \quad (1)$$

The voltage transfer gain ratio is

$$G = \frac{V_o}{V_{in}} = \frac{2-k}{1-k} \quad (2)$$

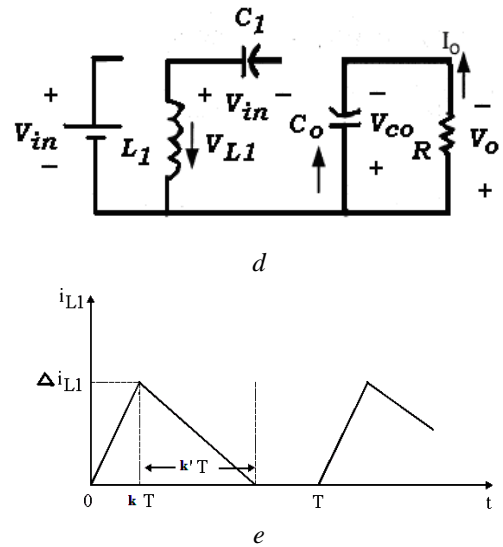
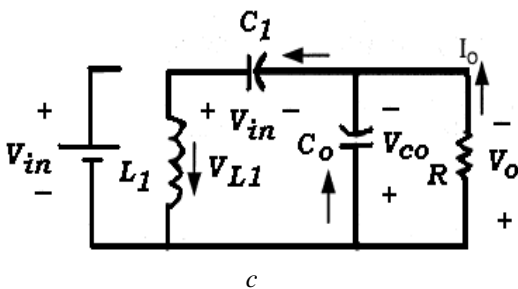
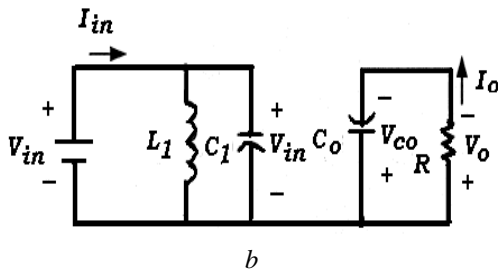
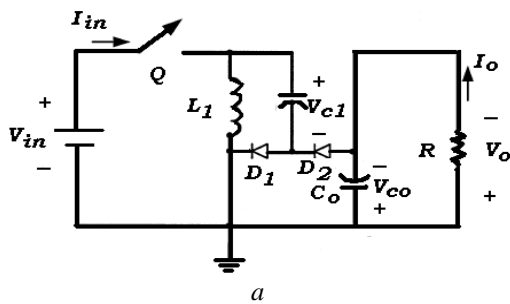


Fig. 1. The NOSLLC

(a) Topology, (b) Mode 1 operation, (c) Mode 2 operation, (d) Equivalent circuit during DCM operation, and (e) Waveform of discontinuous inductor current.

In fixed mode, the normalized charges over the capacitor,  $C_o$  in a period should be zero and it can be written as (3)

$$kTi_{C_{o-on}} = (1-k)Ti_{C_{o-off}} \quad (3)$$

$$i_{C_{o-on}} = I_o$$

The deviation ratio of  $i_{L1}$  is

$$\xi = \frac{\Delta_{i_{L1}}/2}{i_{L1}} = \frac{k(1-k)TV_{in}}{2L_1 I_o} = \frac{k(1-k)}{G} \frac{R}{2f_s L_1} \quad (4)$$

The ripple voltage of  $V_o$  is

$$\Delta V_o = \frac{\Delta Q}{C_o} = \frac{I_o(1-k)T}{C_o} = \frac{(1-k)}{f_s C_o} \frac{V_o}{R} \quad (5)$$

Then, the discrepancy ratio of  $V_o$  is

$$\xi = \frac{\Delta V_o / 2}{V_o} = \frac{(1-k)}{2Rf_s C_o} \quad (6)$$

### B. Operation of a POSLLC

A topology of the POSLLC is displayed in Fig. 2 (a) [7]. It contains the input DC source voltage  $V_{in}$ , and the energy storage components such as capacitors  $C_1$  and  $C_o$ , inductor  $L_1$ , the power switch  $Q$ , the diodes  $D_1$  and  $D_2$  and the load resistance  $R$ . The POSLLC presumed that all of the elements are ideal and moreover the POSLLC functions in the CCM. Figs. 2 (b) and (c) demonstrate the modes of working of the POSLLC. As illustrated in Fig. 2 (b),  $Q$  is closed,  $C_1$  is energised to  $V_{in}$  and  $i_{L1}$  depends on  $V_{in}$ . The input current  $I_{an}$  flows through  $D_1$ .  $R$  is supplied by  $C_o$ . As shown in Figure 2 (c),  $Q$  is open,  $i_{L1}$  decreases with the  $V_o - 2V_{in}$  level.  $i_{L1}$  flows through  $C_o$ ,  $R$  and  $D_2$ , and kept continuous. Consequently, the ripple of  $i_{L1}$  can be given as follows:

$$\Delta_{iL1} = \frac{V_{in} k T}{L_1} = \frac{V_o - 2V_{in} k T}{L_1} \quad (7)$$

$$V_o = \frac{2-k}{1-k} V_{in} \quad (8)$$

The transfer ratio of voltage is

$$G = \frac{V_o}{V_{in}} = \frac{2-k}{1-k} \quad (9)$$

$I_{an}$  is equal to  $i_{L1} + i_{C1}$  in the switch-OFF mode and it is just equal to  $i_{L1}$  in the switch-ON mode. The capacitor current  $i_{C1}$  is equal to  $i_{L1}$  in the  $Q$ -open mode. In the fixed mode, the normalised charges across the capacitor  $C_1$  do not change.

$$i_{in-off} = i_{L1-off} = i_{C1-off}, \quad i_{in-on} = i_{L1-on} + i_{C1-on}$$

$$k T i_{C1-on} = (1-k) T i_{C1-off} \quad (10)$$

If  $L_1$  is large enough,  $i_{L1}$  is almost equivalent to its average current  $I_{L1}$ . As a result,

$$I_{in-off} = i_{L1} = i_{C1-off}, \quad I_{in-on} = i_{L1} + \frac{1-k}{k} I_{L1} \quad (11)$$

$$i_{C1-on} = \frac{(1-k)}{k} i_{L1}$$

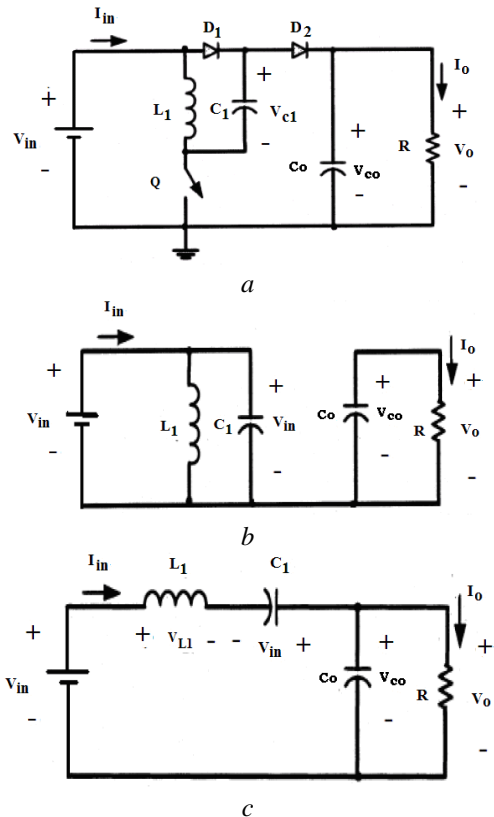


Fig. 2. The POSLLC

(a) Topology, (b) Mode-1 working, and (c) Mode-2 working. In addition the average  $I_{an}$  is

$$I_{in} = k i_{in-on} + (1-k) i_{in-off} = i_{L1} + (1-k) i_{L1} = (2-k) i_{L1} \quad (12)$$

Allowing for  $T = \frac{1}{f}$  and

$$\frac{V_{in}}{I_{in}} = \left( \frac{(1-k)}{(2-k)} \right)^2 \frac{V_o}{I_o} = \left( \frac{(1-k)}{(2-k)} \right)^2 R \quad (13)$$

The disparity ratio of the  $i_{L1}$  is

$$\xi = \frac{\Delta_{iL1}/2}{i_{L1}} = \frac{k(2-k)TV_{in}}{2L_1 I_{in}} = \frac{k(1-k)^2}{2(2-k)} \frac{R}{f_s L_1} \quad (14)$$

The ripple voltage of  $V_o$  is

$$\Delta_{vo} = \frac{\Delta Q}{C_o} = \frac{I_o(1-k)T}{C_o} = \frac{(1-k)}{f_s C_o} \frac{V_o}{R} \quad (15)$$

Consequently, discrepancy ratio of the  $V_o$  is

$$\xi = \frac{\Delta_{vo}/2}{V_o} = \frac{(1-k)}{2Rf_s C_o} \quad (16)$$

**C. Operation of a NOEBC**

The topology of NOBC is displayed in Fig. 3 (a) [7]. The NOBC consists the input DC supply voltage  $V_{in}$ , and storage components  $C_1, L_1$ , power switch  $Q$ , diode  $D_1$  and  $R$ . The NOBC presumed that all the elements are supreme and moreover the NOBC functions in the CCM. To investigate the working of the NOBC, the operation is separated into 2 modes of working. Figs. 3 (b) and (c) shows the modes of working of the NOBC. In the mode 1 operation,  $Q$  is in the closed condition,  $C_1$  is energised by  $V_{in}$  and  $i_{L1}$  depends on  $V_{in}$ . The corresponding circuit of NOBC in the mode 1 operation is illustrated in Fig. 3 (b). In mode 2 operation,  $Q$  is open,  $i_{L1}$  decreases with the  $V_{C1} - V_{in}$  level and moreover  $i_{L1}$  passes through  $D_1$ . The corresponding circuit of the NOBC in mode 2 operation is displayed in Fig. 3 (c). Thus, the ripple of  $i_{L1}$  can be expressed as follows:

$$\Delta_{iL1} = \frac{V_{in} k T}{L_1} = \frac{V_{C1} - V_{in}}{L_1} (1-k) T \quad (17)$$

The voltage transfer gain ratio is

$$G = \frac{V_o}{V_{in}} = \frac{1}{1-k} \quad (18)$$

and inductor average current during open mode of  $Q$  is

$$i_{L1} = (1-k) \frac{V_o}{R} \quad (19)$$

The variation of the  $i_{L1}$  ratio is

$$\xi = \frac{\Delta_{iL1}/2}{i_{L1}} = \frac{k T V_{in}}{(1-k) 2 L_1 I_o} = \frac{k}{2} \frac{R}{f L_1} \quad (20)$$

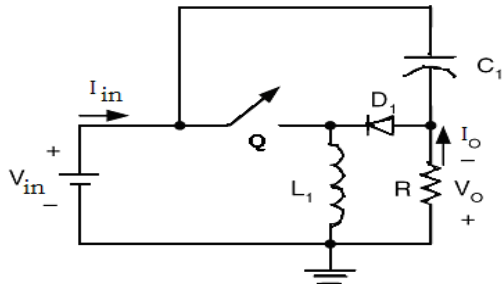
The ripple voltage of  $V_o$  is



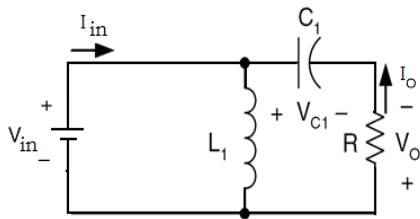
$$\Delta V_o = \frac{\Delta Q}{C_1} = \frac{I_o(1-k)T}{C_1} = \frac{(1-k)V_o}{f_s C_1 R} \quad (21)$$

Therefore, the variation ratio of the  $V_o$  is

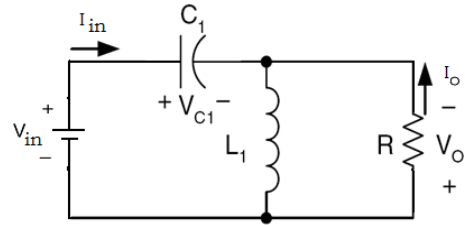
$$\xi = \frac{\Delta V_o / 2}{V_o} = \frac{(1-k)}{2Rf_s C_1} \quad (22)$$



a



b



c

Fig.3. The NOBC

(a) Topology, (b) Mode 1 working, and (c) Mode 2 working.

#### D. Selection of critical inductance analysis for LCs

The critical value of circuit inductance (coil) ( $L_c$ ) is the value that transits the circuit between the CCM and the DCM. More importantly, it is the minimum value of the coil to retain the operation in the CCM. On the other hand, the continuity of current depends on the line, load and circuit-associated parts. The worst-case design could consider the ranges in which the input voltage and load changes take place. The converters are rating more than a few tens of watts then they are designed to operate in the CCM. To guarantee the CCM even under the very light load conditions, obviously large inductance is required. On the contrary, the inclusion of large inductance affects the dynamics of the system. Generally, the inductance value is not found to be more than three times of  $L_c$ . The condition for  $L_c$  selection of the DC-DC converters is also explained [12]. For the average inductor current,  $i_{L1}$ , and the inductor current ripple,  $\Delta i_{L1}/2$ , Table 1 presents the derived relations/equations of  $L_c$  for different fundamental LCs.

Table 1. Critical selection of inductance analysis for fundamental LCs

Topology of fundamental LCs	$\Delta i_{L1}$	$i_{L1}$	$\Delta i_{L1}/2 = i_{L1}$ and $L_c$
POSLLC	$\Delta i_{L1} = \frac{V_{in}}{f_s L_c} k \quad (7)$	$i_{L1} = \frac{(2-k)}{I_{in}} \& \frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 R \quad (12)$	$L_c = \frac{k(1-k)^2 R}{2(2-k) f_s}$
NOESLLC	$\Delta i_{L1} = \frac{V_{in}}{f_s L_c} k \quad (1)$	$i_{L1} = \frac{1}{(1-k)} \frac{V_o}{R} \quad (4)$	$L_c = \frac{k(1-k) R}{2 \frac{V_o}{V_{in}} f_s}$
NOEBC	$\Delta i_{L1} = \frac{V_{in}}{f_s L_c} k \quad (17)$	$i_{L1} = (1-k) \frac{V_o}{R} \quad (19)$	$L_c = \frac{k R}{2 f_s}$

### III. STATE SPACE AVERAGING MODELLING OF LCS WITH CONTROLLER DESIGN

#### A. Modeling of a NOSLLC

The state space equations of the Fig. 1 (b) can be expressed as (23)

$$\begin{cases} \dot{i}_{L1} = \frac{V_{in}}{L_1} \\ \dot{V}_o = -\frac{V_o}{C_o R} \end{cases} \quad \text{Switch closed} \quad (23)$$

The state-space equations of Figure 1 (c) can be expressed by Equation (24)

$$\begin{cases} \dot{i}_{L1} = \frac{V_{in} - V_o}{L_1} \\ \dot{V}_o = \frac{i_{L1}}{C_o} - \frac{V_o}{C_o R} \end{cases} \quad \text{Switch open} \quad (24)$$

Using the charge balance rule of  $C_1$ ,  $T$  can be expressed using Equation (25), where  $k$  is the status of the switch ( $k = 1$  when  $Q$  is closed, and  $k = 0$  when  $Q$  is open).

$$kC_1 \frac{dV_{C1}}{dt} + (1-k)i_{L1} = 0 \quad (25)$$

As there are two capacitors in the NOSLLC, which are  $V_{C1} = V_{in}$ ,  $V_o$ , only a state-space variable is required to be selected except  $V_{in}$ . Simultaneously, with inductor current  $i_{L1}$ , entire space variables of the NOSLLC are selected likewise  $i_{L1}$  and  $v_o$ , respectively  $x_1$  and  $x_2$ .

By using Equations (23)–(25), the NOSLLC modelling can be stated by Equation (26) as follows:

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{V}_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-k}{L_1} \\ \frac{1-k}{C_o} & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \end{bmatrix} V_{in} \quad (26)$$

$$A = \begin{bmatrix} 0 & -\frac{1-k}{L_1} \\ \frac{1-k}{C_o} & -\frac{1}{RC_o} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{1}{L_1} \\ 0 \end{bmatrix} \quad (27)$$

Where, A and B represents the averaged system state space matrices.

### B. Modelling of a POSLLC

The state-space equations of Figure 2 (b) can be expressed by Equation (28) as follows:

$$\begin{cases} \dot{i}_{L1} = \frac{V_{in}}{L_1} \\ \dot{V}_o = -\frac{V_o}{C_o R} \end{cases} \quad \text{Switch closed} \quad (28)$$

The state space equations of the Fig. 2 (c)) can be expressed by equation (29) as

$$\begin{cases} \dot{i}_{L1} = \frac{2V_{in} - V_o}{L_1} \\ \dot{V}_o = \frac{i_{L1}}{C_o} - \frac{V_o}{C_o R} \end{cases} \quad \text{Switch open} \quad (29)$$

By using the charge balance rule in  $C_1$ , Equation (30) for T can be written as follows:

$$kC_1 \frac{dV_{C1}}{dt} + (1-k)i_{L1} = 0 \quad (30)$$

Where, k is duty cycle.

with  $i_{L1}$  and  $v_o$ , respectively  $x_1$  and  $x_2$ . By using Equations (28)–(30) and moreover considering  $k = 1$  when Q is the subinterval of conduction, with  $k = 0$  after the diode is in the on-state subinterval, the state-space average POSLLC modelling can be given by Equation (31) as follows:

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{V}_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-k}{L_1} \\ \frac{1-k}{C_o} & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{2-k}{L_1} \\ 0 \end{bmatrix} V_{in}$$

$$Y = [0 \quad 1] \begin{bmatrix} i_{L1} \\ V_o \end{bmatrix} \quad (31)$$

$$A = \begin{bmatrix} 0 & -\frac{1-k}{L_1} \\ \frac{1-k}{C_o} & -\frac{1}{RC_o} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{2-k}{L_1} \\ 0 \end{bmatrix},$$

$$C = [0 \quad 1], \quad D = [0 \quad 0]$$

(32)

Where, A, B, C and D are represents the matrices of averaged system state space.

### C. Modelling of a NOBC

The state space equations of the Fig. 3(b) may be written as

$$\begin{cases} \dot{i}_{L1} = \frac{V_{in}}{L_1} \\ \dot{V}_{c1} = \frac{V_{C1}}{C_1 R} - \frac{V_{in}}{RC_1} \end{cases} \quad \text{Switch closed} \quad (33)$$

Likewise, state space equations of Fig.3(c) can be inscribed as

$$\begin{cases} \dot{i}_{L1} = \frac{V_{in}}{L_1} - \frac{V_{C1}}{L_1} \\ \dot{V}_{c1} = \frac{i_{L1}}{C_1} + \frac{V_{in}}{RC_1} - \frac{V_{C1}}{RC_1} \end{cases} \quad \text{Switch open} \quad (34)$$

The complete state-space average NOBC modelling with state variables  $i_{L1}$  and  $V_{C1}$  is expressed by the following relation:

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{V}_{C1} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-k}{L_1} \\ \frac{1-k}{C_1} & -\frac{1}{RC_1} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_{C1} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1-2k}{RC_1} \end{bmatrix} V_{in}$$

(35)

### D. Analysis of DCM operation of NOSLLC

The DCM of the NOSLLC network is depicted in Fig.1 (d) and the inductor current  $i_{L1}$  result is demonstrated in Fig.1 (e).

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The values of capacitor are sufficiently high such that the voltages of capacitor can be presumed to be fixed. As shown in Figure 1 (e),  $T$  represents the transferring time period and  $k$  represents duty cycle. In the DCM, the time period  $(k + k')$   $T \leq t \leq T$ ,  $i_{L1}$  through the coil is null,  $Q$  is in the OFF mode and  $D_1$  and  $D_2$  are nonconduction as shown in Figure 1 (d). As shown in Fig. 1 (e), it is clear that the condition of the DCM can be expressed by Equation (36).

$$k + k' < 1 \quad (36)$$

From the Figs. 1(b), 1 (c) and 1(e). During  $0 \leq t \leq kT$ ,  $i_{L1}$  boosts with slope  $V_{in}/L_1$ . During  $kT \leq t \leq (k + k') T$ ,  $i_{L1}$  falls with slope  $-(V_o - V_{in})/L_1$ . As a result,

$$\Delta i_{L1} = \frac{V_{in}}{L_1} kT = \frac{V_o - V_{in}}{L_1} k' T \quad (37)$$

The equation (37) can be changed as

$$V_{in} k = (V_o - V_{in}) k' \quad (38)$$

In a constant mode, the average capacitor current is 0. Assuming the current drawing over the output capacitor  $C_o$  in Figure 1 (b)–(d), it includes the connections given below:

$$k' T \left( \frac{1}{2} \Delta i_{L1} - I_o \right) = k T I_o + (1 - k - k') T I_o = (1 - k') T I_o \quad (39)$$

Using  $\Delta i_{L1} = \frac{V_{in}}{L_1} kT$  from (37),  $I_o = \frac{V_o}{R}$  and  $T = \frac{1}{f}$ ,

substituting them into Equation (39), Equation (40) can be formulated.

$$\frac{1}{2} \frac{V_{in} k' k}{f L_1} = \frac{V_o}{R} \quad (40)$$

Considering Equations (38) and (40), it can be reformulated as follows:

$$k' = \frac{k V_{in}}{V_o - V_{in}} = \frac{2 f L_1 V_o}{V_{in} k R} \quad (41)$$

Then, putting  $G = V_o/V_{in}$  into Equation (41) so subsequently it can be expressed as Equation (42).

$$k' = \frac{k}{G - 1} = \frac{2 f L_1 G}{k R} \quad (42)$$

So,

$$G^2 - G - \frac{k^2 R}{2 L_1 f} = 0 \quad (43)$$

Solving Equation (43), at that moment  $G$  can be written as Equation (44).

$$G = \frac{1}{2} \left( 1 + \sqrt{1 + 2 k^2 \frac{R}{L_1 f}} \right) \quad (44)$$

### E. Design of PI controller for POSLLC

The output voltage of the POSLLC is controlled by using PIC as illustrated in Fig.4(a). The voltage output is calculated and equated (LM 741 IC) with wanted reference voltage output that offers voltage error signal. This process of error signal is done over the PIC to keep the  $V_o$  fixed as well as minimise the steady-state error. In this study, the

PIC (LM 741 IC) output sets the control signal for the converter and it is compared (LM 311 IC) with a carrier triangular signal (using LM 741 IC) to produce the PWM gate pulse of the same converter. Then, the generated gate pulse is applied to the power switch of the converter through a driver circuit (2125 and 6N137). The parameters of the PIC such as proportional gain ( $K_p$ ) and integral time ( $T_i$ ) are determined according to the Zeigler–Nicholas tuning procedure [9–11].

The transfer function (TF)  $G(s)$  of Equation (45) is derived by the state-space average model of equations of Equation (32) with MATLAB. Thereafter,

$$G(s) = \frac{2.27e^{-13} s + 1.65e^8}{s^2 + 666.7 s + 5.5e^7} \quad (45)$$

for simplicity in the design, since the  $2.27e^{-13} s$  term in the TF model numerator is small and it can be omitted. Thus, the TF can be written as

$$G(s) = \frac{1.650e^8}{s^2 + 666.7 s + 5.5e^7} \quad (46)$$

The characteristics equation using proportional control is given as

$$s^2 + 666.7 s + (5.5e^7 + K \cdot 1.650e^8) = 0 \quad (47)$$

The routh array of equation (47) is

$$s^2 : 1 \quad (5.5e^7 + 1.650 e^8 K)$$

$$s : 666.7$$

$$s^0 : (5.5e^7 + 1.650 e^8 K)$$

From this technique, the POSLLC providing a sustained swinging among definitive gain for stability can be obtained with the help of the Routh–Hurwitz condition ( $K_{cr} = 0.022$ ) and its equivalent ultimate period ( $P_{cr} = 0.0012$  s). By employing this technique, the  $K_p = K_{cr}/2 = 0.011$  and  $T_i = P_{cr}/1.2 = 0.011$ s values are determined. Similarly, the same steps are applied to obtain the PIC parameters for NOESLLC and NOEBC and their values are presented in Table 2. Fig.4 (b) shows an analogue PIC circuit using the operational amplifier LM 741.

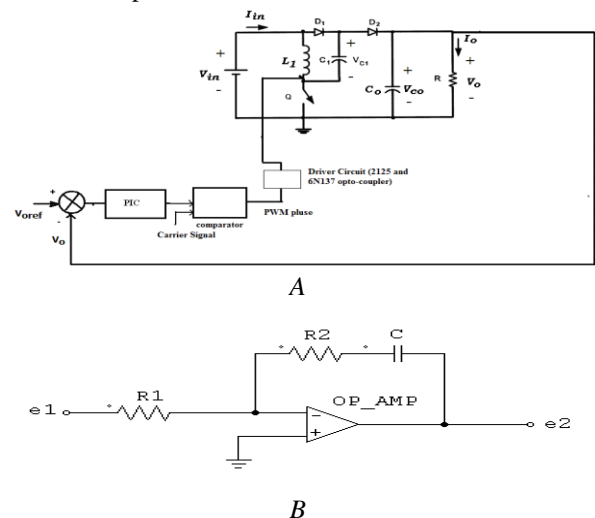


Fig.4. (a) Structure of PIC for POSLLC with critical inductance (37µH) and (b) Analog PIC or Electronic PIC.

From Fig.4 (b), the impedances can be obtained as follows:

$$Z_1=R_1 \quad \text{and} \quad Z_2 = R_2 + \frac{1}{Cs}$$

$$\frac{Z_2}{Z_1} = \frac{R_2Cs + 1}{R_1Cs} = \frac{R_2}{R_1} + \frac{1}{R_1Cs}$$

$$\text{Let, } K_p = \frac{R_2}{R_1} \quad \& \quad K_i = \frac{1}{R_1C} = \frac{K_p}{T_i}$$

$$e_2 = -\left(K_p + \frac{K_i}{s}\right)e_1$$

PIC is designed by using the rules of thumb of Ziegler and Nicholas,  $K_p = 0.011$  and  $K_i = 1$ , and for this value its performance is good.

$$K_p = \frac{R_2}{R_1}$$

$$R_2 = 0.011 \times 10K\Omega \quad \text{assume } R_1 = 10K\Omega$$

$$= 0.11 K\Omega$$

$$K_i = \frac{1}{R_1C} = \frac{K_p}{T_i}$$

$$C = 1/1 \times 10K\Omega \quad \text{assume } R_1 = 10K\Omega$$

$$= 0.0001F$$

**Table 2. PIC values of  $K_p$  and  $T_i$  for fundamental LCs**

LCs	$K_p$	$T_i(s)$
NOBC	0.013	0.001
NOSLLC	0.012	0.01

The above control procedure is applied for NOESLLC to arrived the PI controller parameters ( $K_p = K_{cr}/2=0.0211$  and  $T_i = P_{cr}/1.2=0.0311s$ ).

#### IV. DISCUSSIONS ON IMPLEMENTATION AND EXPERIMENTAL RESULTS

##### A. Critical inductance of a NOSLLC

The primary objective of this segment is to explain implementation and trial outcomes of NOSLLC with  $L_c$  using the PIC. The detailed specifications of NOSLLC are  $V_{in} = 12 V$ ,  $R = 100 \Omega$ ,  $L_1 = L_c = 37 \mu H$ , switching frequency  $f_s = 100 kHz$ ,  $C_1 = 30 \mu F$ ,  $C_o = 30 \mu F$ ,  $V_o = -36 V$  and  $d = 0.66$ . The hardware model is done on the NOSLLC circuits with the similar conditions. The power circuit parameters of NOSLLC are as follows: (refer Fig. 1 (a))

- $Q$  IRFN 540;
- $D_1 \& D_2$  FR306;
- $C_1 \& C_o$  30  $\mu F/200V$ ;
- $L_1$  37 $\mu H/7A$  (Ferrite Core)

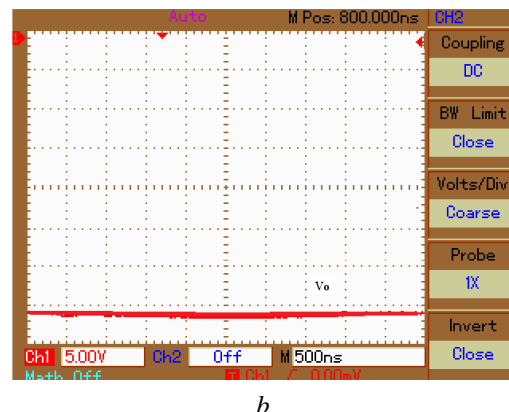
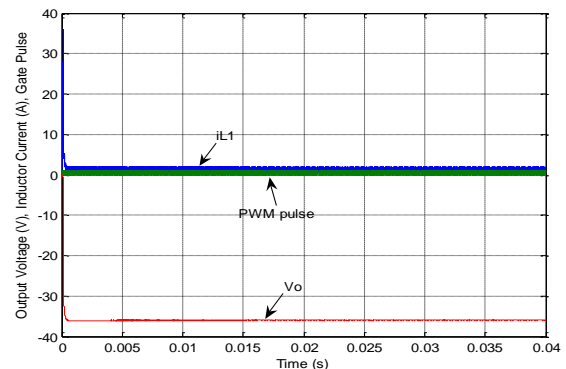
Fig. 5 (a) and (b) illustrates the implementation and experimental output voltage, inductor current and PWM gate pulse waveforms of NOSLLC at  $L_c$  with PIC. From Figure 5, it can be clearly detected that inductor current and output voltage of NOSLLC using PIC have generated null peak overshoots and fast settling time.

Fig. 6 (a)–(c) illustrates the zoomed implementation and experimental output voltage, inductor current and PWM gate pulse responses of NOSLLC at  $L_c$  with PIC. From these results, it can be clearly detected that implementation and experimental inductor current of the NOSLLC have boundary condition between the CCM and the DCM. Fig. 7 (a) and (b) illustrates the implementation and experimental output current of NOSLLC at  $L_c$  with PIC. From these results, it can be observed that output current of same with PIC has produced zero overshoots and quick relaxing time.

Fig. 8 (a) displays the results of the coil current and the output current results of the NOSLLC for higher inductor value (74  $\mu H$ ). From these results, it can be clearly detected that inductor current moves well in CCM. Fig. 8 (b) displays the prototype model of the NOSLLC with PIC.

Fig. 9 (a) and (b) expressions the implementation and trial results of the voltage output of NOSLLC at  $L_c$  with PIC for  $V_{in}$  changing from 12 V to 15 V and 12 V to 9 V. From these results, it shows that outcomes of the output voltage of NOSLLC with PIC have produced a small peak overshoot of -0.3 V and a time of 0.0125 s.

Fig. 10 (a) and (b) displays the experimental and implementation output voltage and output current of the NOSLLC using  $L_c$  with PIC for  $R$  changing from 100  $\Omega$  to 150  $\Omega$  and 100  $\Omega$  to 50  $\Omega$ . It can be observed that output voltage results of the NOSLLC consuming PIC have generated a low overshoot of -0.3 V with a rapid time of 0.014 s.



**Fig. 5. Responses of output voltage, inductor current and PWM gate pulse of NOSLLC with critical inductance (37 $\mu H$ ) using PIC: (a) implementation and (b) experimental [CH1: -5V/Div. output voltage].**

# Experimental Verification of Critical Inductance Analysis for LUO Family Converters

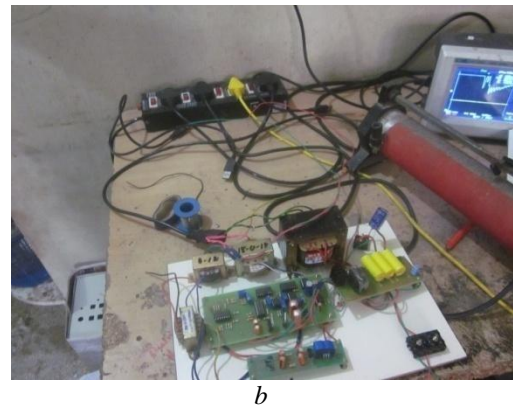
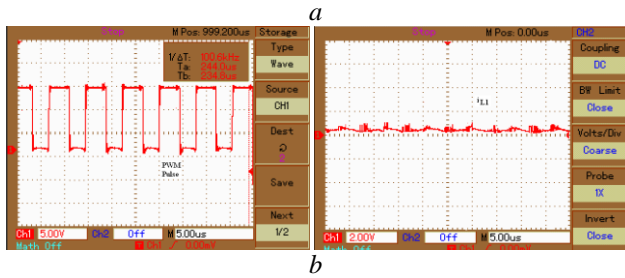
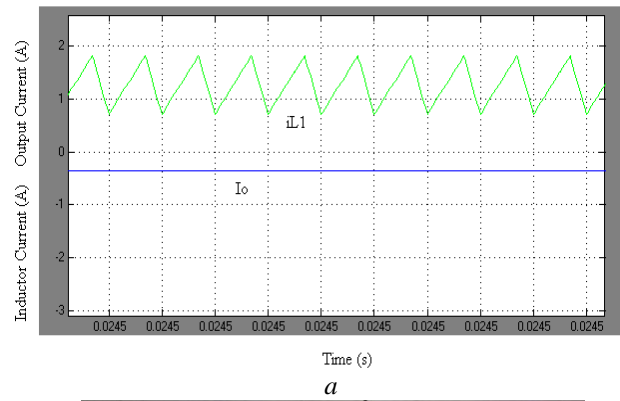
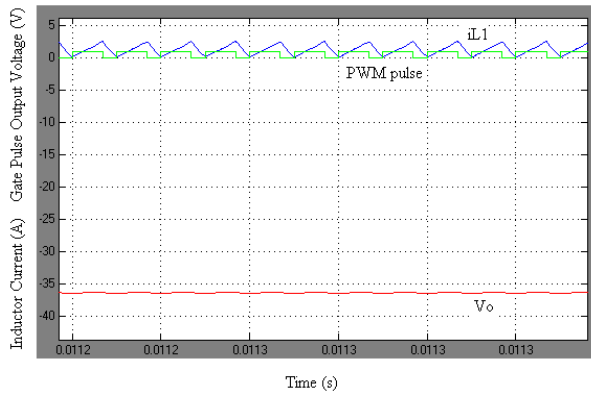


Fig. 6. Zoomed responses of output voltage, inductor current and PWM gate pulse of NOSLLC with critical inductance ( $37\mu\text{H}$ ) using PIC: (a) implementation and (b) experimental.

Fig. 8. (a) Simulated responses inductor current and output current of NOSLLC with inductance ( $74\mu\text{H}$ ) and (b) experimental set-up model of NOSLLC using PIC.

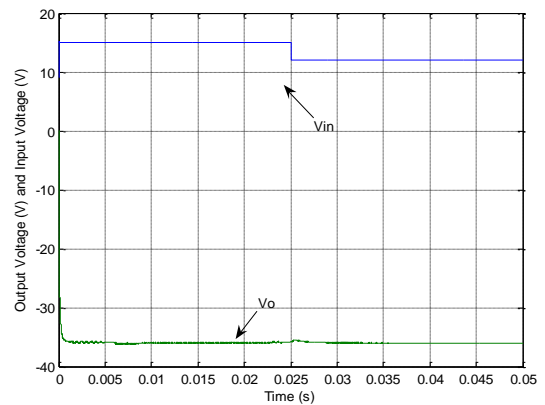
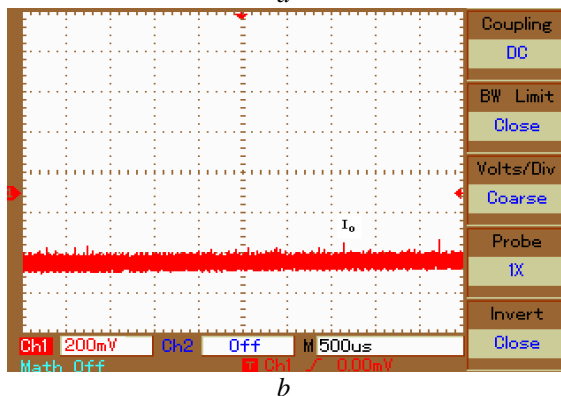
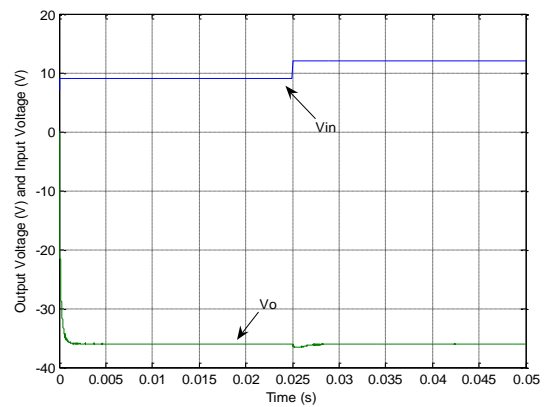
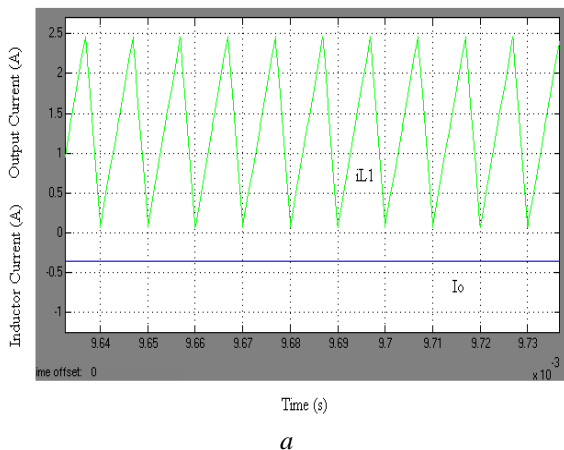
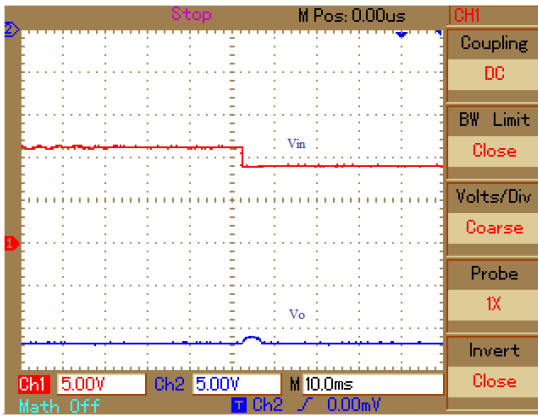
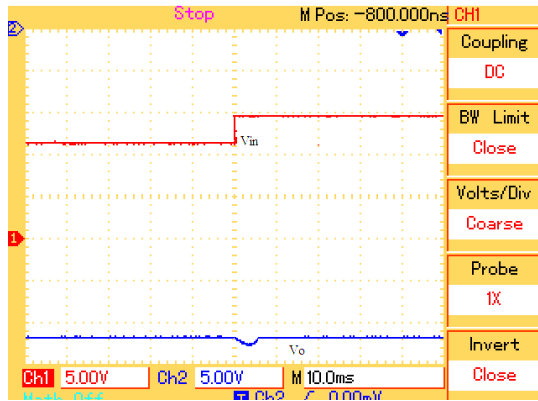


Fig.7. Responses of inductor current and output current of NOSLLC with critical inductance ( $37\mu\text{H}$ ) using PIC: (a) implementation and (b) experimental.

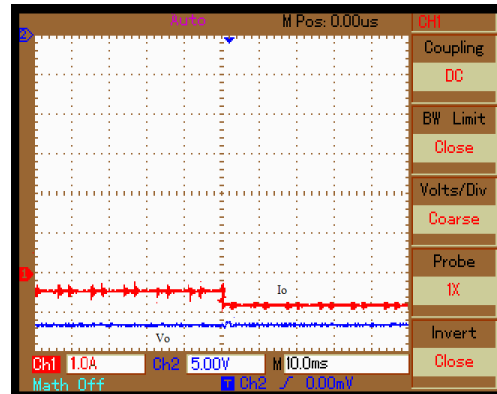
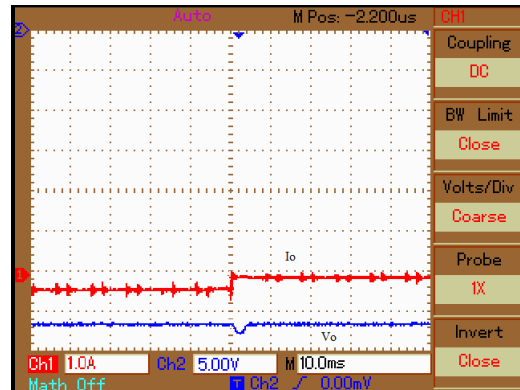
Fig. 8. (a) Simulated responses inductor current and output current of NOSLLC with inductance ( $74\mu\text{H}$ ) and (b) experimental set-up model of NOSLLC using PIC.





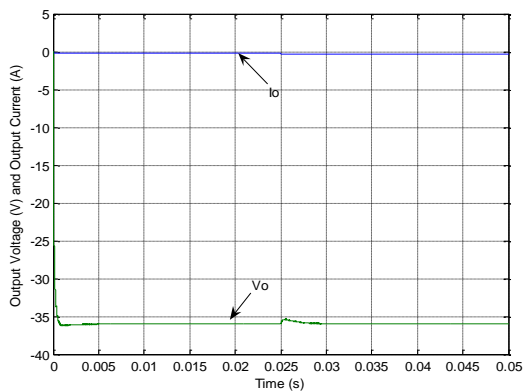
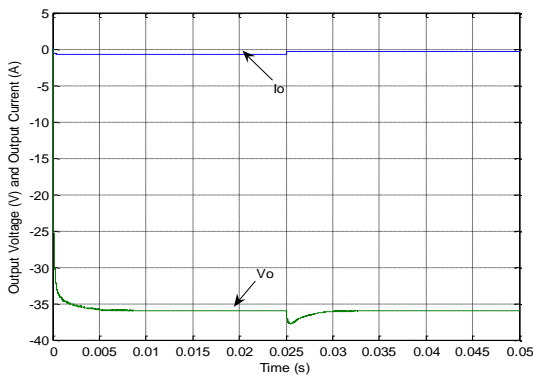
b

Fig.9. Responses output voltage of NOSLLC using controller with critical inductance under  $V_{in}$  change from 12V to 15V and 12V to 09V, (a). Implementation and (b) Experimental.



b

Fig.10. Responses output voltage of NOSLLC using controller with critical inductance under  $R$  changes from  $100\Omega$  to  $150\Omega$  and  $100\Omega$  to  $50\Omega$ , (a). Implementation and (b) Experimental.



a

### B. Critical inductance of a POSLLC

The objective of this segment is to explain the trial and implementation outcomes of POSLLC with  $L_c$  using PIC. The detailed specifications of the POSLLC are  $V_{in} = 12\text{ V}$ ,  $R = 100\ \Omega$ ,  $L_1 = L_c = 37.64\ \mu\text{H}$ ,  $C_1 = 30\ \mu\text{F}$ ,  $C_o = 30\ \mu\text{F}$ ,  $V_o = 36\ \text{V}$  and  $d = 0.56$ . The hardware model is done on the POSLLC circuits with the similar implementation conditions. The detailed power circuit parameters of the POSLLC are the same as those of the NOSLLC.

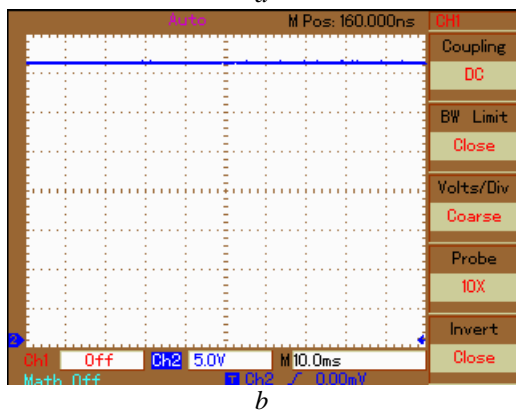
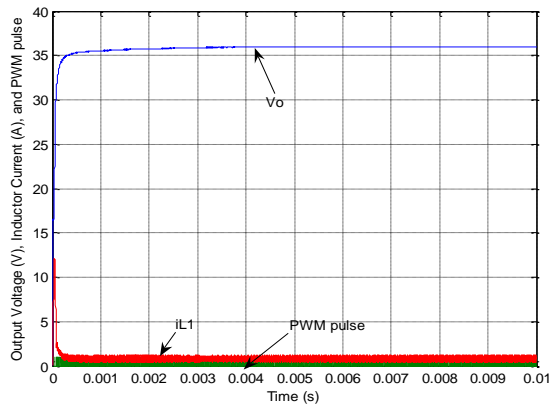
Fig. 11 (a) and (b) illustrates the experimental and implementation output voltage, inductor current and PWM gate pulse waveforms of the POSLLC at  $L_c$  with PIC. From these figures, it is clear that the voltage output of the POSLLC has formed null overshoots and quick settling time. Figure 12 (a) and (b) displays the trial and implementation inductor current and PWM gate pulse of POSLLC at  $L_c$  with PIC. From these figures, it can be clearly detected that inductor current has boundary condition between the CCM and the DCM.

Fig. 13 (a) and (b) illustrates the results of the  $V_o$  output voltage of the POSLLC at  $L_c$  with PIC for  $V_{in}$  changing from 12 V to 15 V and 12 V to 9 V. From these results, it is clear that implementation retorts of output voltage of POSLLC with PIC have produced a peak overshoot of 0.3 V and a time of 0.0125 s.

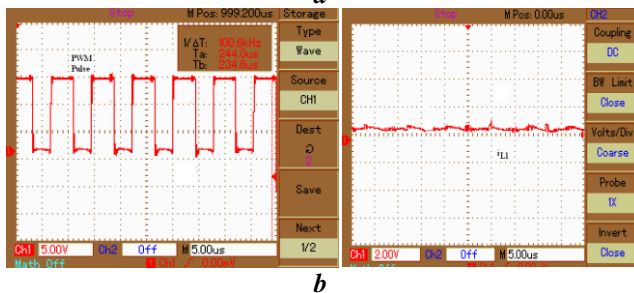
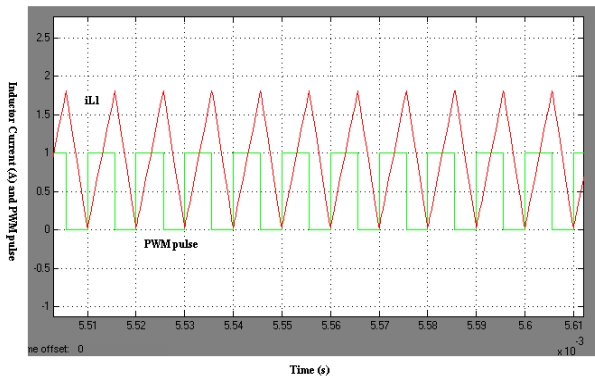
Fig.14 (a) and (d) illustrates the outcomes of the output voltage and output current of POSLLC at  $L_c$  with PIC for  $R$  changing from  $100\ \Omega$  to  $150\ \Omega$  and  $100\ \Omega$  to  $50\ \Omega$ .

## Experimental Verification of Critical Inductance Analysis for LUO Family Converters

It can be detected that implementation the output voltage results of POSLLC with PIC have produced a small overshoot of 0.32 V with a quick time of 0.014 s.

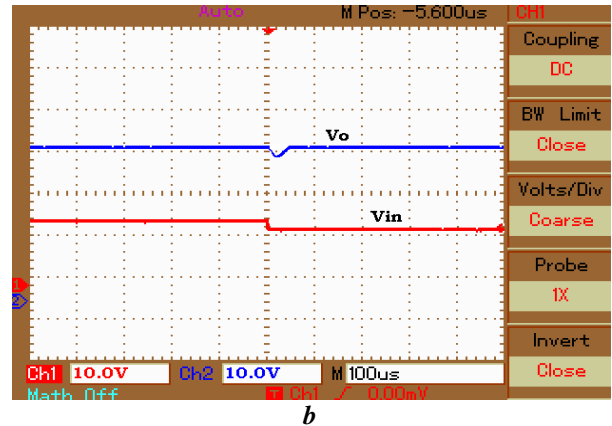
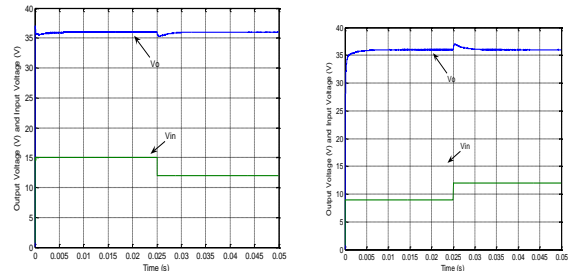


**Fig.11. Responses of output voltage, inductor current and PWM gate pulse of POSLLC with critical inductance (37.64  $\mu$ H) using PIC: (a) implementation and (b) experimental [CH2:5V/Div. output voltage].**

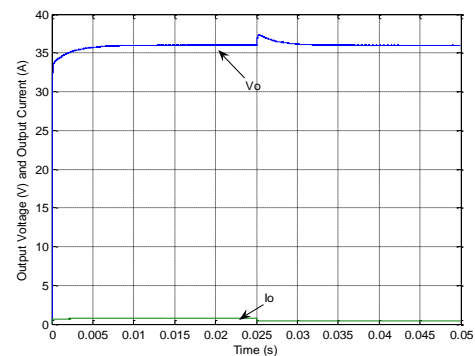
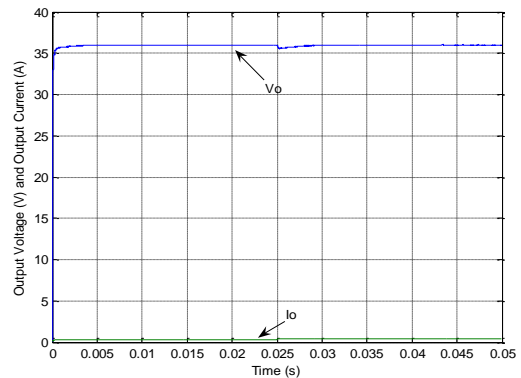


**Fig.12. Zoomed responses of inductor current and PWM gate pulse of POSLLC with critical inductance (37.64  $\mu$ H)**

using PIC: (a) implementation and (b) experimental.



**Fig. 13. Responses output voltage of POSLLC using controller with critical inductance under  $V_{in}$  change from 12V to 15V and 12V to 09V, (a). Implementation and (b) experimental [Ch2:10V/Div-output voltage and Ch1:10V/Div- input voltage].**



**Fig.14. Responses output voltage of POSLLC using controller with critical inductance under R changes from (a).100 $\Omega$  to 50 $\Omega$  and (b).100 $\Omega$  to 150 $\Omega$ .**

## V. CONCLUSION

Thus, the experimental analysis over CIA for the three fundamental LFCs using PIC has been attempted successfully and demonstrated both in MATLAB/Simulink as well as prototype models. In order to strengthen the work results are presented to verify the CIA of the fundamental LFCs such as NOSLLC and POSLLC using PIC for large and small values of inductance current. The implementation and experimental outcomes of the CIA of LFCs with PIC has verified good dynamic performance, proficient line, load variations and excellent start-up transient as well as steady-state responses than the traditional converters. Based on the experimental analysis it evidently proves that LFCs using PIC performs well while considering a better voltage transfer ratio, efficiency and minimised capacitor voltage as well as inductance current ripples for various energy applications and also states that it is one of the important future researches that have to be taken into concern in order to cope up with different applications.

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**Dr. K.Sathish Kumar** (Kanniah Sathish Kumar) received the Ph.D degree from VIT University, Vellore, India, has 17 years of total teaching experience and in 12 years of his research experience. He has worked in various research teams to develop new applications of evolutionary computing algorithms for solving various power system problems like unit commitment, economic dispatch, emission reduction, smart grid, power system reconfiguration and restoration. He is currently an Associate Professor in the School of Electrical Engineering at VIT University, Vellore. His current area of interest is studying interconnection problems in linkages of HVDC and HVAC (765 kV) transmission lines with existing 230 kV high voltage lines, Nano additives for high voltage XLPE cables, Optimization of smart grids and Multi level inverters