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Implementation of full Adder with 2x1 Mux using Optimised Gdi Technique

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Abstract: - The major considerations of any digital circuit are area and power consumption. GDI (Gate Diffusion Input) - an advanced technique is proposed for designing a circuit in order to reach the requirements, reduce power consumption, and effective utilization of area. Despite having many uses, the GDI technique is noted for some drawbacks. The principle point of this paper is to concentrate on the downsides of the existing GDI technique and to propose an improved version of GDI technique to withstand the disadvantages of the earlier one. A full adder with 2x1 MUX is designed using conventional techniques and compared their simulation results with full adder using optimized GDI technique. Simulation and analysis of the full adder are carried out using CADENCE tool at 45nm technology. Simulation results proved that the proposed design had improved the performance of GDI and reduces almost less than 50% of layout area and power consumption is only 1.5% of the power consumed using conventional technique.

Keywords: Drawbacks of GDI, GDI, layout area, low power consumption.

I. INTRODUCTION

From the day transistor has invented to date, there are many developments and advancements in techniques for designing a logic. Each development mainly aims at the area, power, and performance of the circuit. According to Moore's law, for every 18 months, transistors used on a chip are doubled. Precisely, the size of the transistor reduces gradually. As a result, the area used to implement the design decreases. Apart from the reduction in the size of the transistor, improvements in the design techniques also add better performance and reduces the area and power consumption of the circuit.

Heretofore, many advancements took place in implementing a logic. Complementary Metal Oxide Semiconductor (CMOS) logic is one of the most broadly utilized regular methods. Besides its significant usage for implementing any complex logic, CMOS technique has massive circuit power consumption due to a greater number of transistors.

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Nowadays, power consumption has become the most crucial factor in implementing any circuit. So, to implement a power-efficient circuit (low power circuit), the number of transistors must be minimized.

Gate Diffusion Input (GDI) is one of the popular logic design technique which can implement complex Boolean functions using smaller number of transistors, less power and area when compared with CMOS, pass transistor, transmission gate techniques [1]. The most important reason to use GDI technique in realizing a circuit is the transistor count used to design a logic are less, most importantly, reduces power consumed by the circuit than other conventional methods.

GDI enables simple gates, low transistor count, and low power dissipation. With the assistance of this procedure enormous number of complex circuits can be designed by utilizing just two transistors [2]. GDI technique is very effective at designing both combinational and sequential circuits in relatively conventional design techniques [3].

Although, GDI technique implements a power and area efficient circuit, the output voltage levels of the circuit are less when compared to input voltage levels. Because the input signals are directly coagulated with source and drain terminals of PMOS and NMOS, respectively. Depending on the input we may observe transition problems from high voltage level to low voltage level and vice versa, because PMOS and NMOS are strong '1', weak '0' and strong '0', weak '1', respectively.

In this paper, a new design is proposed to overcome the drawback in the GDI technique and to achieve maximum efficiency at the output. The proposed design is compared with CMOS logic and GDI technique. The Full Adder is designed and implemented using proposed design and strict simulation, analysis and comparisons are performed using cadence tool at 45nm technology. Full Adder being a fundamental part of any computational combination circuit, in this paper it is chosen to design and implement using conventional as well as proposed techniques.

The contribution of the paper is accompanied as below; this section is followed by literature review, Section II describes about the methodology and designs, Section III shows the analysis and comparison results implemented in different techniques. Section IV concludes the results and presents the best technique from all the techniques.

A. Literature Review

CMOS is one of the conventional techniques to design a circuit. One of the most significant advantages of this technique is this high noise margin and reliable operation at low threshold voltages [4-6].

But the use of substantial number of transistors results in high input loads, more power consumption and larger silicon area [7]. GDI is another technique to implement low power circuits. This technique allows the reduction in propagation delay, power consumption and area of the circuit while maintaining less design complexity [8,9]. The most complex applications such as convolution, which evaluate the output of the system can be designed with fast and accuracy by using GDI technique [10]. The GDI technique achieved 37% power saving and 30% delay compared to CMOS [11]. Despite having many advantages this technique also has many drawbacks such as low swing issues [12], fabrication cost [13] when compared to CMOS technique. From the literature survey the main drawback of the GDI technique is its voltage swing at output signal. This paper mainly focusses on the drawbacks of the GDI technique and proposes the optimized GDI technique.

II. METHODS AND DESIGN

A. GDI basic cell

Gate Diffusion Input (GDI) is one of the eminent techniques to design a low power and area efficient circuit. The GDI technique is to use a simple cell for designing a convoluted logic, as shown in Fig 1. Even though GDI basic cell looks like as CMOS inverter, there is a subtle contrast among CMOS and GDI basic cell. GDI basic cell has three terminals G (basic entryway contribution for NMOS and PMOS), P (contribution for PMOS channel or source), N (contribution for NMOS channel or source).

The inputs of the GDI cell is charged accordingly to get the desired logic, as shown in TABLE-I. X and Y are the two input signals, '0' and '1' represents GND and V_{DD}, respectively. Unlike CMOS logic, the GDI technique uses P and N terminals as inputs to reduce redundant transistors. Complex function in CMOS, which used (12-16) transistors is designed with just two transistors in the GDI technique.

TABLE-II demonstrates the transistor count essential to realize the logic utilizing GDI technique, proposed design and CMOS logic. Function1 and Function2 are all universal functions in the GDI technique as NAND and NOR in CMOS logic.

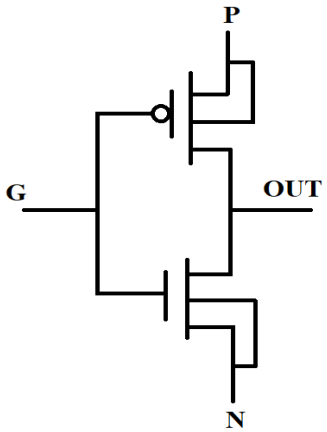


Fig. 1 GDI basic cell

TABLE- I: GDI Truth Table

FUNCTION	G	N	P	OUT
Function1	X	Y	'1'	X'+Y
Function2	X	'0'	Y	X'Y
NOT	X	'0'	'1'	X'
OR	X	'1'	Y	X+Y
AND	X	Y	'0'	XY
MUX	X	Z	Y	X'Y+XZ
XOR	X	Y'	Y	X'Y+XY'
XNOR	X	Y	Y'	XY+X'Y'

TABLE- II: Transistor count for implementing a logic in GDI Technique and CMOS Technique

FUNCTION	GDI	CMOS
Function1	2	6
Function2	2	6
NOT	2	2
OR	2	6
AND	2	6
NAND	4	4
NOR	4	4
MUX	2	12
XOR	4	16
XNOR	4	16

B. Optimized GDI Technique

The optimized GDI technique is proposed to overcome the drawbacks of the GDI technique. The principle for implementing a logic in optimized GDI technique is same as GDI technique as shown in TABLE-I. But the difference between the optimized and conventional GDI technique is an extra circuitry is added at the output as shown in Fig 2. In order to reduce the drawbacks of GDI technique.

This extra circuitry added will increase the number of transistors used for implementing a logic when compared to GDI technique. When compared in terms of performance the optimized GDI technique is better than GDI technique. This design is more advantageous when the circuit is more complex i.e., four more transistors are added at each output signal to enhance the signal.

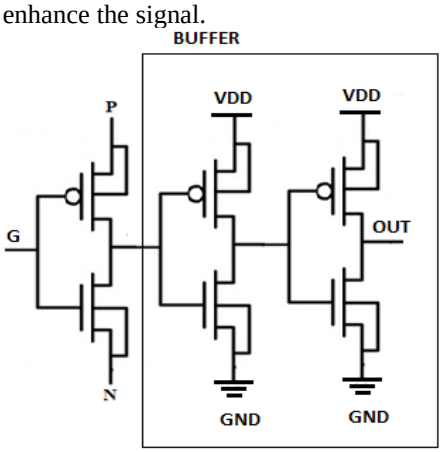


Fig. 2 Proposed Design

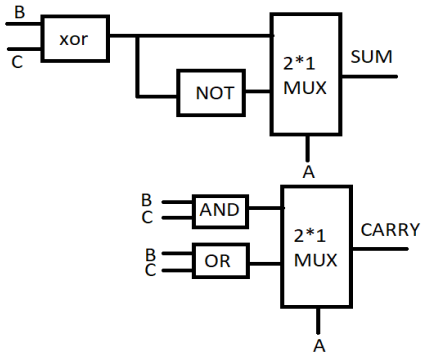


Fig. 3. Block diagram of adder

C. Design of Full Adder

A circuit implemented using MUX will reduces the number of logic gates, complexity and is more economical than a circuit implemented with only logic gates. So, here to reduce the complexity of the circuit the full adder is implemented using two 2x1 multiplexers as shown in Fig 3.

The equations (1), (2), (3) and (4) show variation between designing a full adder. Equations (1) and (2) to design a full adder using complete logic gates. Equations (3) and (4) to design a full adder using 2x1 MUX. Comparing the two sets of equations for SUM and CARRY, it has been observed that there is a reduction in usage of logic gates for full adder designed using 2x1 MUX.

$$SUM = A \oplus B \oplus C \quad (1)$$

$$CARRY = AB + BC + AC \quad (2)$$

$$SUM = A' (B \oplus C) + A (B \oplus B)' \quad (3)$$

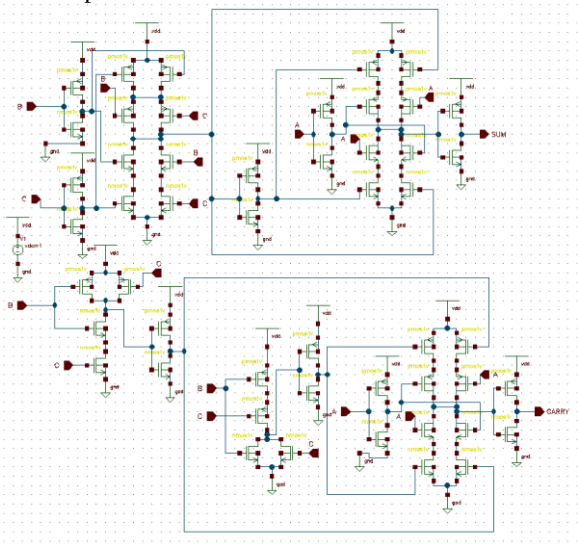
$$CARRY = A'(BC) + A(B+C) \quad (4)$$

Although using MUX as a function generator reduces the number of logic gates and complexity of a design, the design of MUX is very complicated. The block diagram in Fig 3 has some complicated logics gates along with MUX to implement the full adder.

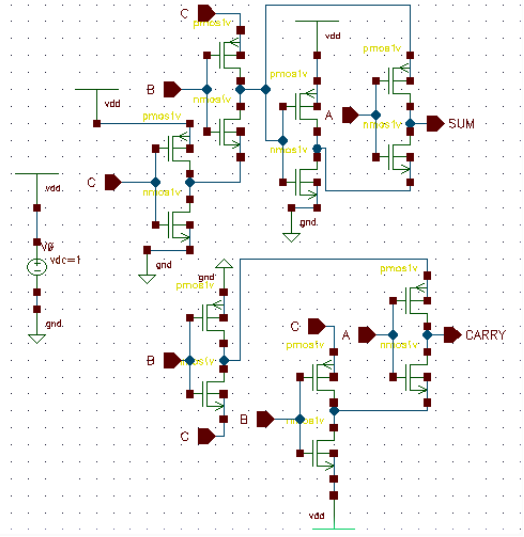
The full adder is implemented in CMOS technique, GDI technique and optimized GDI technique. TABLE 1 shows the logic for basic gates which are used for implementing the full adder in GDI technique. The proposed design also uses the same technique as GDI, but the extra circuit is added at each output signal at sum and carry.

The complexity of the design is known through the schematic. The schematics of the full adder is implemented in different logic techniques are shown in Fig 4. Fig 4a shows the schematic of the full adder designed in CMOS technique. The schematic is more complicated and denser than the schematics of the GDI and optimized GDI design shown in Fig 4b and 4c respectively.

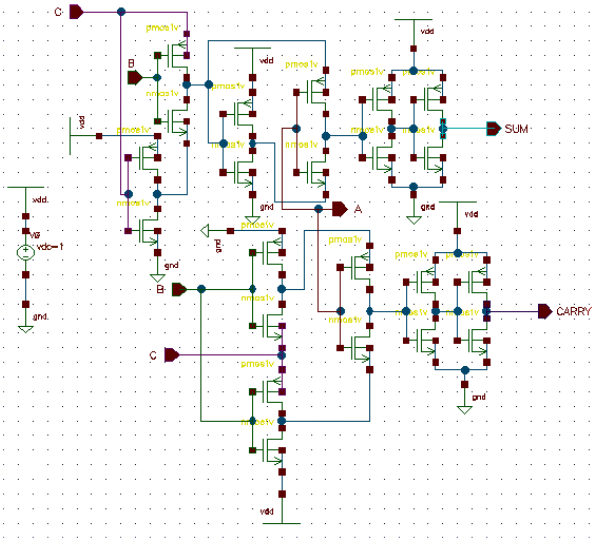
The CMOS technique is more complicated because the number of transistors used to implement MUX, XOR, AND, and OR gates are 12, 16, 6, 6, respectively shown in TABLE 2. Yet, MUX replaces one XOR and one AND gate, the complexity of the circuit remains the same as the number of transistors required for one 2x1 MUX is 12, and there are two such multiplexers in full adder.



4a



4b



4c

Fig 4: Schematic of full adder 4a) CMOS technique 4b) GDI 4c) Optimized GDI design

III. RRESULTS AND ANALYSIS

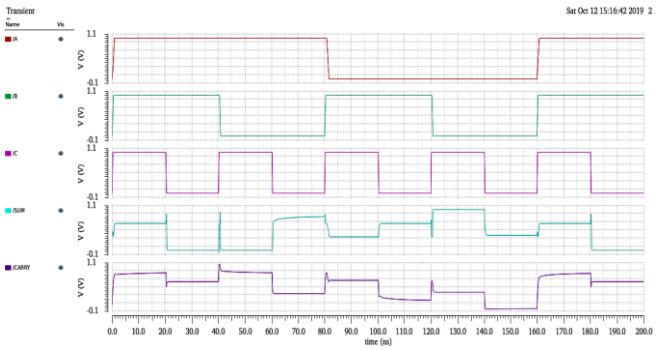
The present section deals with waveforms, layouts and comparison results of CMOS logic, GDI technique, and proposed design. Simulation and analysis are carried with full adder circuit, as discussed in the previous section. Circuit power analysis, layout area analysis, transient analysis carried in the cadence virtuoso tool under 45nm technology is also presented here.

A. Transistor Count

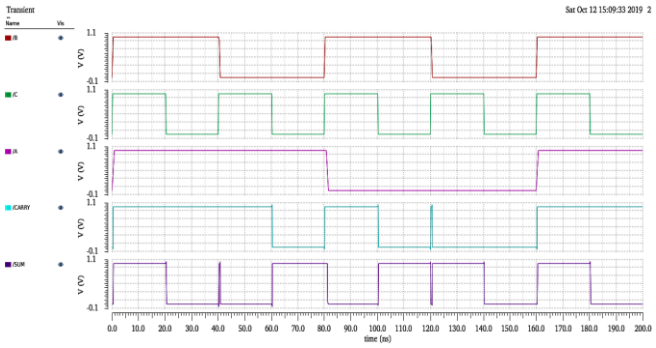
In the previous section the schematics of the full adder designed in different techniques are shown in Fig 4. Among all the schematics, GDI technique uses a smaller number of transistors. The proposed design has same logic as GDI technique, but in order to increase the performance of the circuit extra transistors are added to the circuit. When proposed design schematic is compared with CMOS schematic, it has a smaller number of transistors.

B. Waveforms

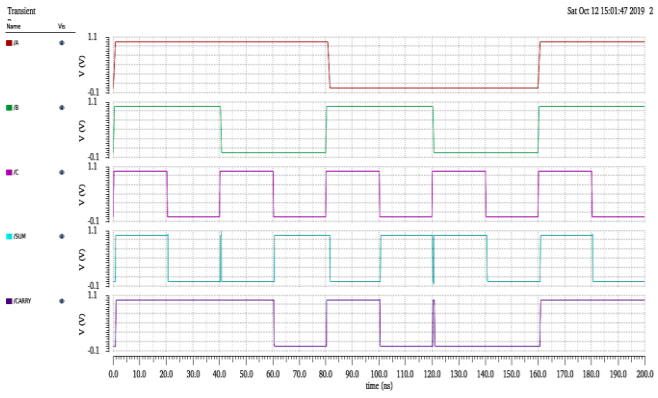
To analyses the performance of the full adder implemented in different techniques transient response is done to the schematics. The waveforms of the transient response are shown in Fig 5. The drawback of the GDI technique is noticed from the transient response waveform shown in Fig 5a, that the output signals of the adder are not as strong as the input signal. And, the output signal lacks a good transition from high to low voltage. Fig 5c shows the transient response of the full adder implemented in proposed design. Here, the drawback of the GDI technique is rectified and the waveforms show better performance than the GDI technique.



5a



5b



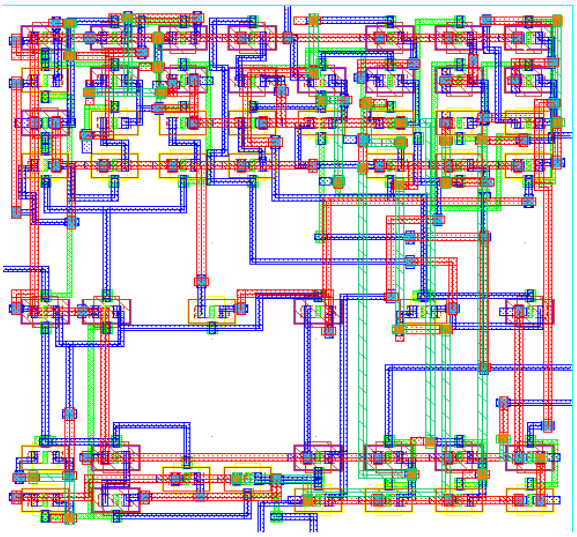
5c

Fig 5: Transient response of full adder implemented with 5a) GDI technique 5b) CMOS technique 5c) Optimized GDI design.

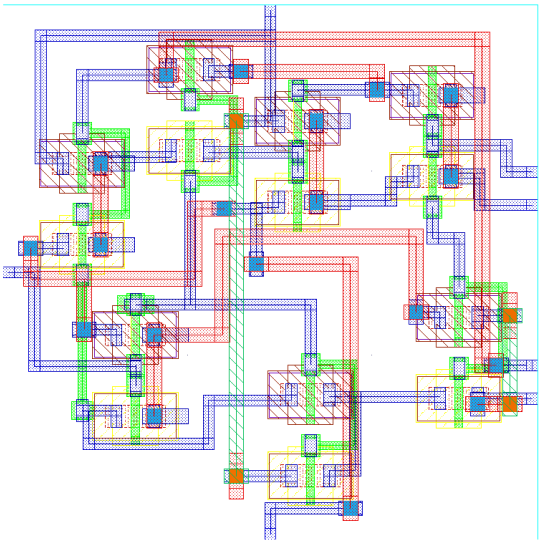
The conventional CMOS technique output waveforms are shown in Fig 5b. As it is a widely used technique in designing a circuit, there is no deviation in the output signal. Among all the schematics and waveforms, the proposed design shows the better performance for the full adder.

C. Area

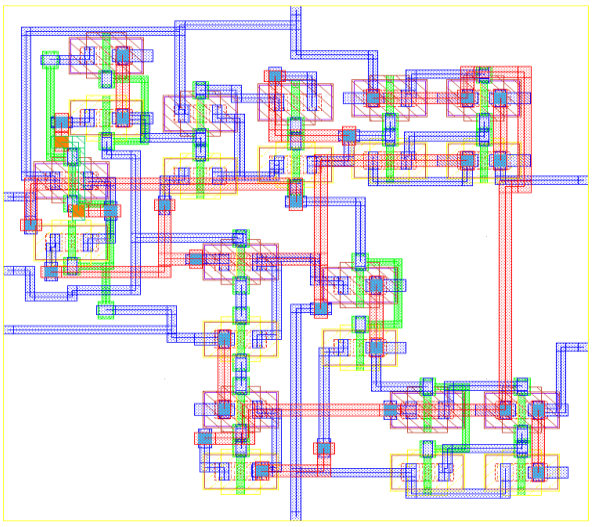
Designing an area efficient circuit is very important to reduce the usage of resources and cost used for implementing a circuit. So, to calculate the area of the circuit, layouts are draw for the schematics of the full adder in cadence virtuoso tool. The layouts are shown in Fig 6. Fig. 6a, 6b, 6c represents layout of the CMOS technique, the GDI technique, and the proposed design respectively. The layout area of each technique is calculated and compared in cadence virtuoso tool. From the results, the area calculated for the full adder design using the proposed technique requires very less area than the conventional CMOS technique.



6a



6b



6c

Fig 6: layout of full adder implemented with 6a) CMOS technique 6b) GDI technique 6c) Optimized GDI design.

The area utilization of each layer in the layout of full adder in different techniques is shown in Fig 7. Although the proposed design occupies slightly more area than the GDI technique, the proposed design recovers the main disadvantage in the GDI technique i.e., at the output signal.

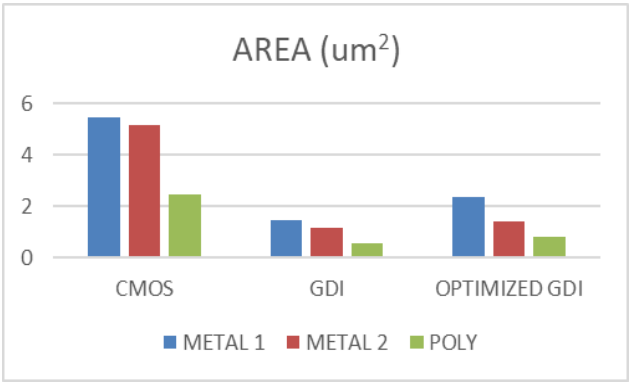


Fig 7: Area of different layers used in the layout of different techniques

D. Power

The primary concern of any designing technique for the circuit is the power consumption of the circuit. The strict analysis is carried to calculate the power consumption of the full adder in different techniques and compared the results for the better performance. The average power consumption of the circuit is calculated using cadence calculator. For theoretical calculation of total power, the equations are shown in equation (5) and equation (9). The equations (6), (7) and (8) represents various terms that leads to total power consumption. The results showed that the power utilized by the proposed design is 1.55% of the power consumed by conventional techniques.

$$P_{total} = P_{static} + P_{dynamic} + P_{short\ circuit} \quad (5)$$

$$P_{static} = V_{DD} I_{leak} \quad (6)$$

$$P_{dynamic} = C_L V_{DD}^2 f \quad (7)$$

$$P_{short\ circuit} = V_{DD}\, I_{max}\, (t_r + t_f)\, f/2 \quad (8)$$

$$P_{total} = V_{DD} I_{leak} + C_L V_{DD}^2 f + V_{DD}\, I_{max}\, (t_r + t_f)\, f/2 \quad (9)$$

Where, V_{DD} is Supply voltage, I_{leak} is Leakage Current, C_L is Load capacitance, f is Input frequency, I_{max} is Maximum static supply current, t_r is Rise time, t_f is Fall time.

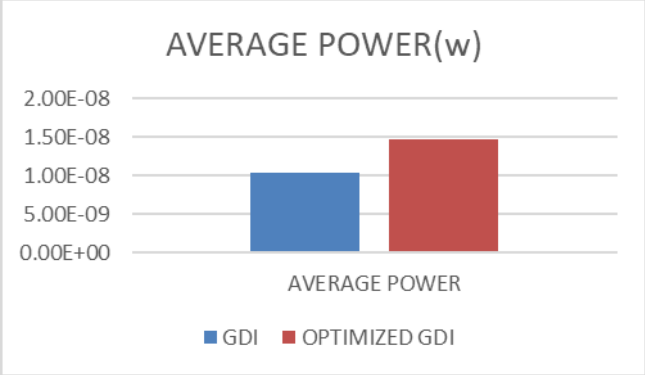


Fig 8: Comparison of GDI and Optimized GDI design in terms of POWER CONSUMPTION

Fig 8 shows the difference in power consumption of the GDI technique and proposed design. Even though GDI consumes only 1.08% of the power consumed by CMOS, the proposed design stands better than the GDI technique in terms of performance.

The careful comparison is done for the better design and the results are tabulated in TABLE-III. Despite the proposed design has little more area and power consumption than GDI technique, the proposed design stands better than GDI in terms of performance.

TABLE-III Comparison of AVERAGE POWER, TRANSISTOR COUNT AND AREA.

PARAMETER	OPTIMIZED GDI DESIGN	GDI	CMOS
AVGERAGE POWER (nW)	14.7	10.3	945.1
TRANSISTOR COUNT	22	14	51
AREA (um^2)	13.17	8.41	29.81

IV. CONCLUSION

The proposed designed is implemented with a full adder, and then compared with the remaining conventional techniques. Simulation and analysis are carried out in the cadence virtuoso tool at 45nm technology. The analysis of the full adder in different techniques showed that the proposed design is better than GDI, as the drawback of GDI is rectified in the proposed design even though there is a slight increase in layout area and power consumption. Also, the proposed design shows better performance in area and power consumption than the CMOS technique. The proposed design layout area is half of the area of the CMOS technique. Also, the power consumption of the proposed design is only 1.55% of CMOS technique, i.e., using the proposed design technique, the power, and area-efficient full adder is implemented.

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