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Full Adders using GDI (With Full Swing) Technique for Power Efficient Computing

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Abstract*: *Adders, Multiplexers and other arithmetic circuits have a crucial role in Digital Signal Processing and various real time applications. Among those, Full adder is a central for most of the digital operations that perform subtraction or addition.
Major component is Adder with High performance and a power efficient in specific applications. In this paper, the adder with high performance and power efficient are designed using Gate Diffusion Logic which reduces threshold voltage problem. We designed the circuits with minimum power consumption and with high performance efficiency. For the simulation of the circuits Mentor Graphics with 130nm technology is used. The obtained result shows that the proposed designs consume the minimum power when compared to other designs which are taken for the comparison.

Keywords*: *hybrid full adder, GDI full adder, Full Swing GDI, Energy Efficient Adder.

I. INTRODUCTION

An adder is a digital circuit that implements binary addition of binary numbers. Full adder is a arithmetic logical circuit which adds three 1-bit binary integers. Full adder gives a sum of 3 inputs along with a carry value. The arithmetic operations a Full adder is a basic hardware block. So the performance of adder effects the overall performance of the system. For a system to be efficient the basic component of the system i.e. the adder should be efficient. Thus, the design of efficient full adder is necessary in order to design an energy efficient system.

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The basic truth table and structure of a full adder are as follows:

Table 1: Full adder truth table

Inputs			Output	
A	B	C_{in}	SUM	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

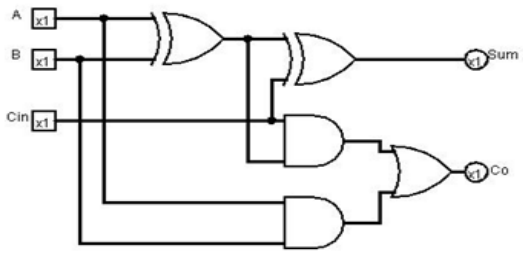


Fig 1 Circuit diagram of full adder

Adders are the basic widely used circuit components in VLSI such as processors and controllers etc. The full adder acts like a core of numerous tasks such as addition, multiplication, subtraction, division and also the count of address. In majority of the computerized frameworks, full adders are the basic way which impacts the general framework execution. Consequently, enhancing adder's presentation is turning into a significant objective.

The intense growth in the compact systems like mobile phones, laptops had intensified research efforts in low power microelectronic devices. The purpose for this is the battery innovation does n't progress at a similar time as microelectronics innovation. The power available for mobile based systems is in limited amount. So, design that consumes less power had become main goal. The criteria for the design of a full adder is generally manifold. The count of transistor is one of the attributes which gives the complexity of a full adder.

Power consumption and speed are two other major criteria with regard to the design of full adders. The performance of the full adders can be optimized to a better extent by a proper selection of gates. The different types of gates generally improve one performance aspect at the cost of other aspect. The most commonly used full adder is that of CMOS logic. The full adder can be designed in various types of logics such as Emitter coupled logic (ECL), Dynamic current mode logic (DCML), Transistor - Transistor logic (TTL), Resistor-Transistor Logic (RTL), Gate diffusion input (GDI) etc. In this paper, we used Gate Diffusion logic (GDI) to design 4 types of full adder circuits.

II. GATE DIFFUSION INPUT

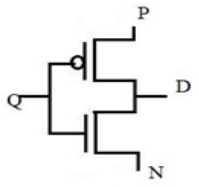


Fig 2: The basic GDI cell

Table 2: logic function of basic GDI cell

N	P	G	OUT	FUNCTION
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	A +B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
0	1	A	$\bar{A}$	NOT

The source, channel and the gate of the transistors can be utilized as an information. Thus, it is named as Gate Diffusion Input. This is a method of low power circuit plan. This strategy permits to diminish zone, time delay and power utilization of computerized circuits by all the while keeping up low intricacy of rationale structure. The GDI strategy empowers the plan of a wide scope of complex function utilizing just 2 transistors. The underneath figure speaks to an essential GDI circuit. The significant contrasts of GDI and CMOS are: a. GDI comprises of three terminals while CMOS has only two terminals. b. In GDI greater part of PMOS and NMOS are associated with p or n so it can be biased random in difference with that of a CMOS inverter. c. The GDI circuit comprises of four terminals: P, N, Q & D. The most significant component of GDI is that there is improved level swing and static attributes of power.

The fumdamental disadvantage of this GDI is that it endures because of drop in limit(threshold) voltage. This decreases the current drive and because of this presentation of gate is affected. The yeild voltage decrease might be repaid with the utilization of swing rebuilding buffers at output(a). Be that as it may, the existance of f buffers at yeild builds transistor tally and furthermore expands general power utilization when they are associated in a steady progression. This methodology utilizes low limit transistors in spots where drop of voltage may happen and it likewise utilizes high limit transistors for invertors. By utilizing such new limit voltage technique, it limits power utilization. But manufacturing is difficult.

Another strategy for swing reclamation of GDI based circuit is utilizing a ultra low power Diode method which is quickly clarified in reference[c]. This designs semiconductor transitor of metal oxide to represent a diode and it it likewise utilized more eight extra transistors to give full swing.It decreases static power dispersal issue as a swing rebuilding buffer yet the manufacturing of circuit utilizing UPLD is tough and in this way considered.The techniques to accomplish full swing at adder(full) yeild which are talked about above either maximise quantity of transistors or increment power utilization due to buffer. Consequently an effort is made to configurate adders. A point by point clarification of equivalent is given next segment.GDI based OR, AND & xor gates for full adder design:The function for a full adder can be represented as:

$$Sum = A \oplus B \oplus Cin \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$Cout = A.B + B.Cin + Cin.A \ldots\ldots\ldots\ldots (2)$$

From equations 1,2 it infers that three fundamental gates are needed for actualizing adder structure. All gates capacities can be accomplished utilizing two transistors in GDI and level graphs of transistors are given. We have taken both the data sources have voltage swing and furthermore yield voltages are given to many input combinations. This reducal in yeild voltage increments with incrementation in stage count. Hence the structure of swing gates in important which is examined futher.

Table 3: Operational characteristics of AND ,OR and XOR gates using GDI logic.

A	B	AND	OR	XOR
'0'	'0'	|Vtp|	|Vtp|	|Vtp|
'0'	'1'	|Vtp|	VDD	VDD
'1'	'0'	Gnd	VDD-Vtn	VDD-Vtn
'1'	'1'	VDD-V_{tn}	VDD-V_{tn}	Gnd

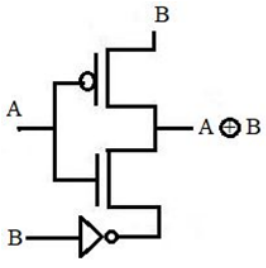


Fig 3 : XOR gate

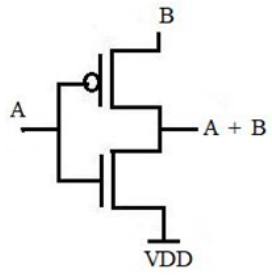


Fig 4: OR gate

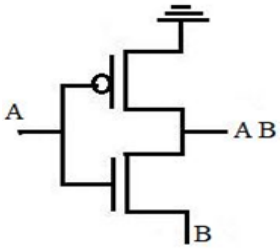


Fig 5: And gate

III. FULL SWING GDI DESIGN OF AND OR & XOR

The disadvantages of the GDI logic is the reduction in voltage swing in the circuit output. The distortion in the swing can be improved with use of the restoring logic for each cell. The above designed circuits of basic gates can be modified for increasing the reduced swing. The universal gates can be used to generate any logical expression. In the same way in the GDI logic there are two functions i.e. Fun1(A'.B) and Fun2(A'+B) in order to generate any logical expression, but even those two functions are also suffering with a threshold drop in the voltage. To overcome this we make use of the full swing logic. The concept of full swing logic is obtained from the reference paper [D]. In the reference [E], a swing restoration transistor is placed near the output to reduce the loss in threshold voltage. The design of the OR, AND, and XOR gates using Fun1 & Fun2 functions which are shown in fig: 6. Though there is an increase in the transistor count from two to three for the design of both OR and AND gates but the operation of full swing may be obtained. In GDI based full swing logic using Fun1 and Fun2 the AND and OR functions construction need three transistors but the implementation with CMOS requires six transistors. Thus this choice of Fun1 and Fun2 for AND and OR gates is better because of a less number of transistors are required and this implementation also provides full swing like that of CMOS. But however, Fun1 and Fun2 based XOR implementation lacks the design based on CMOS.

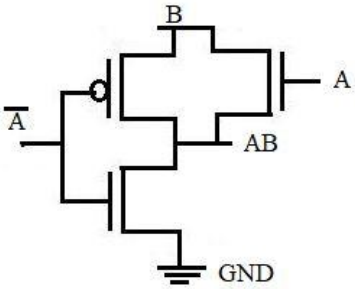


Fig 6(a)

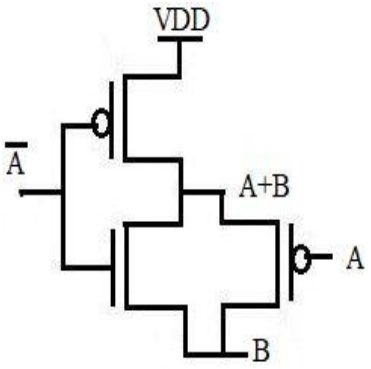


Fig 6(b)

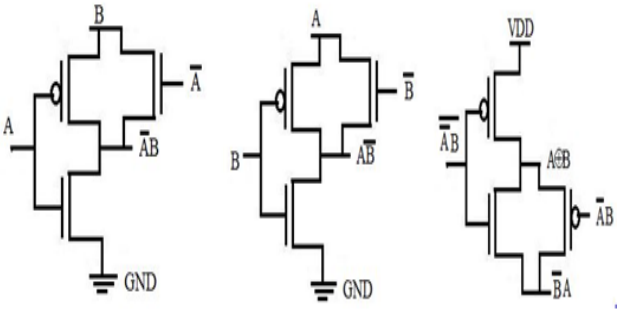


Fig 6(c) Fig 6(d) Fig 6(e)

Fig 6: Full swing gates based on Fun1 and Fun2 (a) AND (b) OR and (c) XOR

Table 4: Operational characteristics of AND, OR and XOR Gates with full swing logic

A	B	AND	OR	XOR
'0'	'0'	Gnd	Gnd	Gnd
'0'	'1'	Gnd	VDD	VDD
'1'	'0'	Gnd	VDD	VDD
'1'	'1'	VDD	VDD	Gnd

Realization of the AND and OR gates can be successfully implemented with Fun1 and Fun2 functions respectively and they operate better when compared to that of the conventional design though these functions are not suitable for realization of XOR. The XOR and XNOR gates are the basic building blocks in many of the arithmetic operations.

The XOR-XNOR gates provides intermediate output for the generation of the full adder.

IV. THE PROPOSED FULL SWING XOR GATE

XOR gate is used as the primary module in implementing full adder design. The XOR gate which is proposed in the reference has four transistors (without including the invertor for the input signal which is complement) that are used for understanding full swing that occur near output. The XOR gate design used with GDI logic and used without full swing are characterized in the below figure:

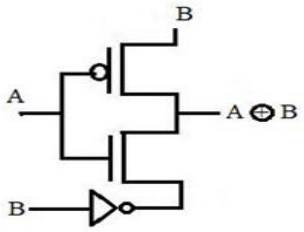


Fig: 7(a)

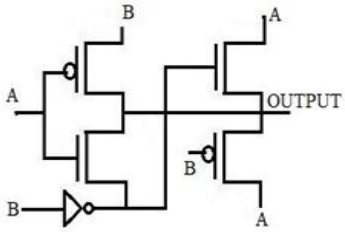


Fig:7(b)

Fig 7: XOR gate

The full adder circuit implementations:

(a) With GDI logic

(b) Design that is prorposed.

The GDI based full adder design having full swing can be designed by using the gates of OR,AND and XOR which has full swing just as shown in the above paragraph.The GDI based full adder design with full swing eliminates the restoration buffers of the swing totally that gives the betterment of device maintenance and all the GDI full adders with full swing can be obtained by again writing the full adder equations in the below full adder designs such that opted equations may include gates with full swing.The fulladder design equations that are expressed with their diagrams in the below full adder designs.

A. Full adder Design-1:

The full adder circuit with both SUM and COUT are expressed in the following expressions of full adder design-1:

$$SUM = Cin'.(A \oplus B) + Cin.(A \odot B)$$

$$Cout = (A \oplus B).Cin + (A \oplus B)'.A$$

This full adder design makes use of the obtained result of XOR gate by the in- between output as a result both Cout and sum will be found.The crucial part of the circuit has an inverter which helps in increase of delay in the full adder circuit.This full adder design should consists of 18 transistors for the full adder function and its design is quite simple.

B. Full adder design -2:

For this full adder design-2 again the SUM and COUT equations are expressed below

$$SUM = A \oplus B \oplus Cin$$

$$COUT = A.B + (A \oplus B).Cin.$$

This design uses transistors of 22 which helps in designing fulladder.

C. Full adder design 3:

Same as the above this design-3 implements both COUT and SUM respectively

$$SUM = A \oplus B \oplus Cin$$

$$COUT = A.B + (A \oplus B).Cin$$

This uses XOR gate calibers the major role because of the sum result in the design is drawn by implementing the XOR gate.

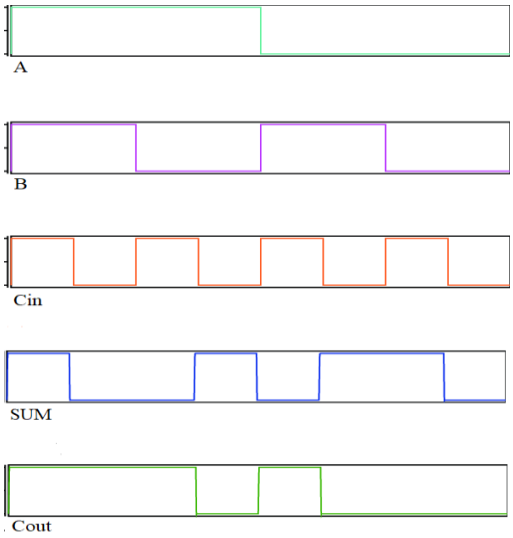
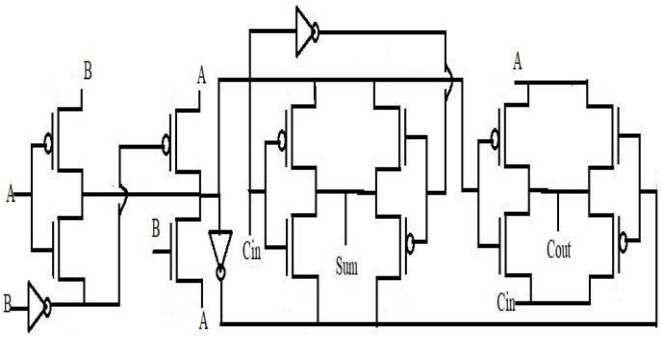
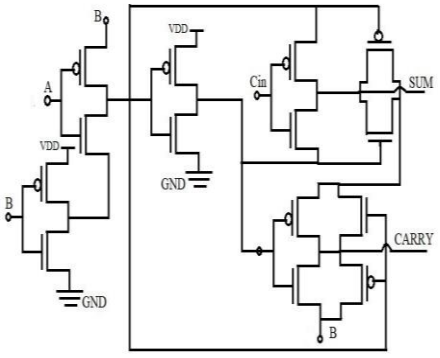


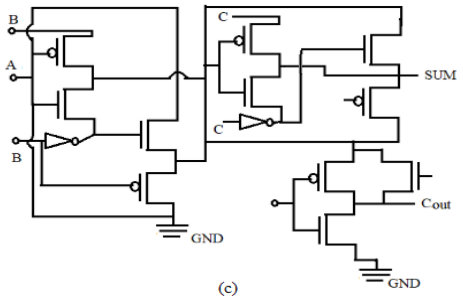
Fig 8: Model Output Waveforms



(a)



(b)



(c)

Fig 9: Proposed Full adder design models a(design1),

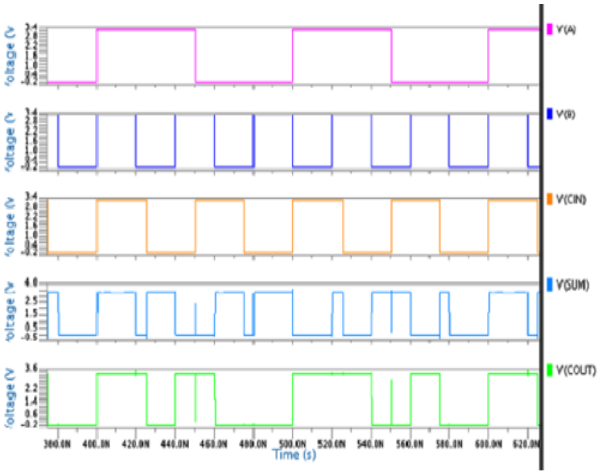


Fig 9(b): Output Waveforms of 18T GDI based Full adder

b(design2), c(design

V. SIMULATION RESULTS

A. Design 1

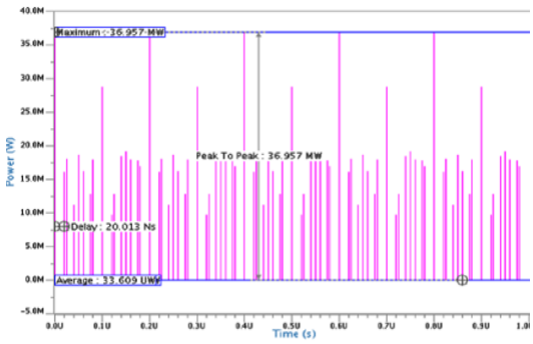


Fig 9(c): Power Analysis of 18T GDI based Full adder

B. Design 2

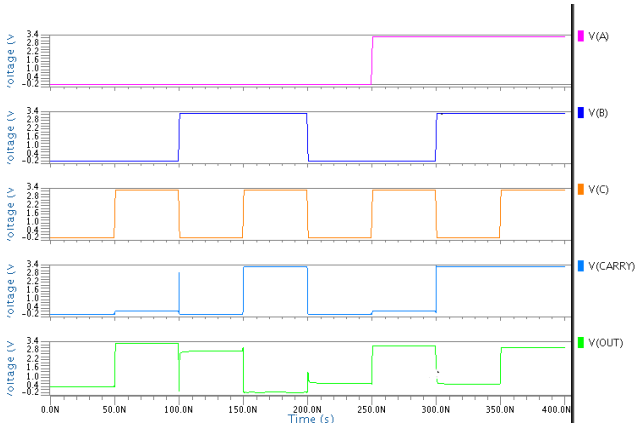


Fig 10(a): Output Waveforms of GDI based Full adder

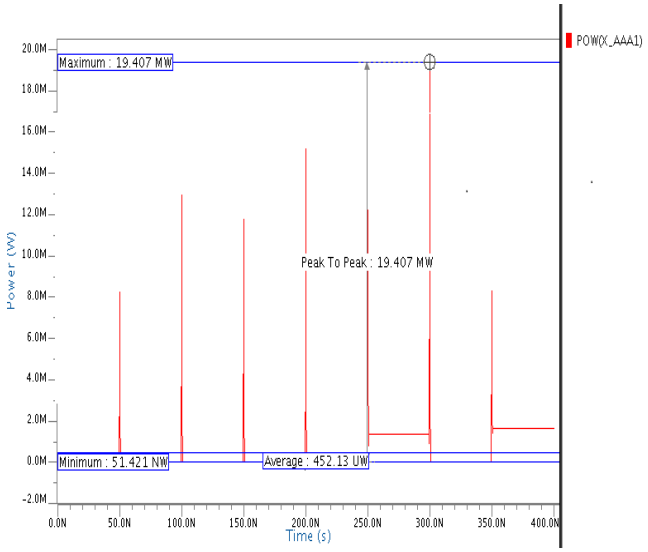


Fig 10(b): Power Analysis of GDI based Full adder

C. Design 3

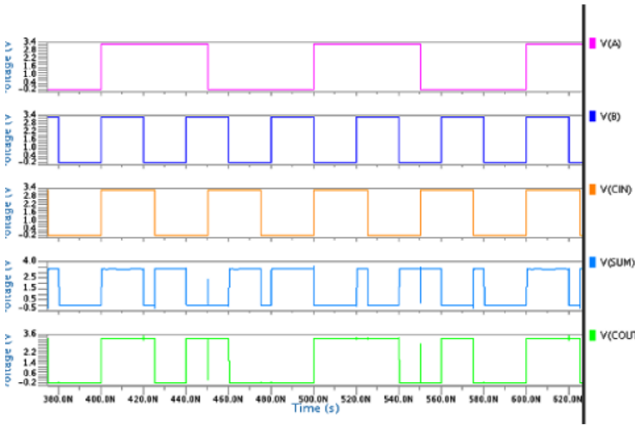


Fig 11(a): output waveforms of GDI based full adder

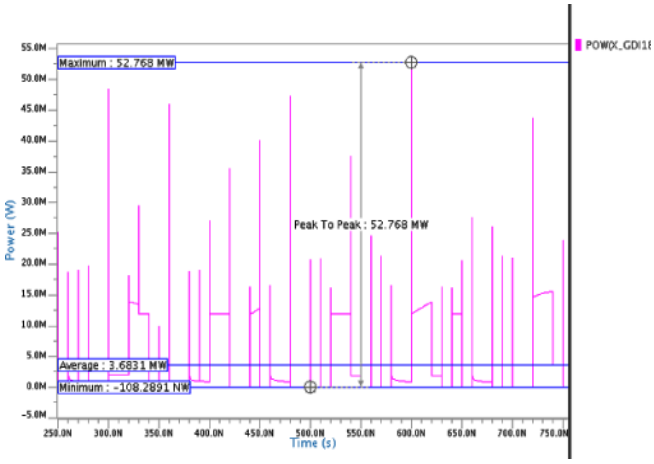


Fig 11(b): Power Analysis of GDI based Full adder

VI. C ONCLUSION

In these paper three full adders ar designed. These designs adopt full swing XOR, OR and AND gates logic so as to reduce the threshold voltage problem in GDI and to enhance the driving capability for the cascaded operation.

The enhanced driving capability also facilitates the lesser voltage and faster operation which finally results in minimum energy consumption. The above designs are simulated using mentor graphics tool and the power analysis is done. The obtained power results are consolidated in the following table:

Table 5: Comparison of Powers

	Max power	Average power	Peak to peak power
Design1	36.9mW	33.6µW	36.9mW
Design2	19.4mW	452µW	19.4mW
Design3	52.7mW	3.6µW	52.7mW

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