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# MFMW: Modified Floor planning with Minimum Wire length

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***Abstract:*** ***Floorplanning is one of the most critical phases inVLSI circuit design. The module alignment has a substantial concentration on the minimization of chip area and total wirelength in slicing floorplan. At foremost, the disadvantages of dead space are investigated and an instinctive and profligate method is proposed to find the equitable part of component. Then, a tormenting for standardized expression is improved to produce new solution, and the proposed simulated annealing algorithm which improves design efficiency is opted for the best floorplan solution. The proposed MFMW method attains less area on the commonly used AMI33 and AMI 49 benchmark circuits.***

***Keywords: Floorplanning, Wirelength, VLSI***

## I INTRODUCTION

In progression with innovation, the outline multifaceted nature is expanding and the circuit measure is improving bigger what's more, bigger so the physical outline turns out to be vital. VLSI physical stage start with Floorplanning [2] stream. It decides the areas and measurements of parts on a chip in order to limit the wirelengths and chip region of interconnect [2]. It is a NP difficult issue [3] from the computational perspective. The dead space increments with the expansion in squares thusly determining an ideal arrangement is a testing assignment. Floorplanning depend on its portrayal [4-15]. The portrayals of design decide the span of dead space and many-sided quality of change among its portrayal and its entire floorplan.VLSI floorplan is used for architecting modules on a single chip. Overall contributions for the floorplanning is an arrangement of m modules W= {w1, w2, w3…… wm}. Widths, statures, and territories of modules are followed as wi, and ai ;1≤ i≤ m. Design target is to mastermind how the modules are placed on a chip under imperatives that any two modules are most certainly not covered and region, wirelength and other execution lists are ideal. Floorplanning has two sets of modules in [2]: **Hard Modules**: A module whose region and viewpoint proportion are settled. **Delicate Modules**: A module is known as a delicate module whose region is settled however angle proportion can change.

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Figure. 1 portraits to floorplanning representations like B-Tree, sequence pair, polish notations and bounded slice grid.

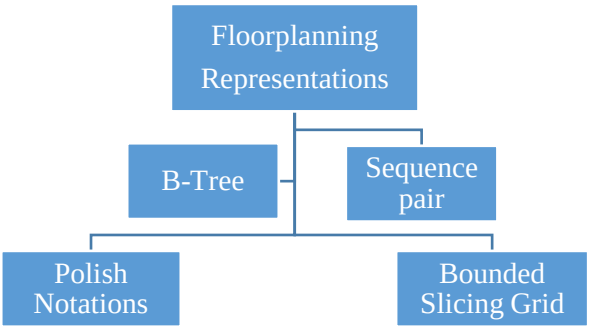


**Figure. 1 Basics of Floorplanning Representations**

Section II portrays about basics of floorplanning. At that point segment III incorporates near General Classification of floorplanning algorithms. Then, Section IV states about the proposed floorplanningalgorithm.At long last, finishes up the letter with conclusion.

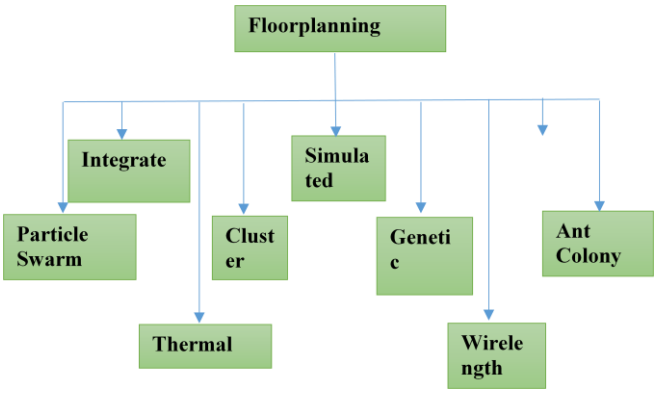


**Figure.1 Classification of Floorplanning Algorithms**

## II GENERAL CLASSIFICATIONS OF FLOORPLANNING SCHEMES

Floorplan algorithms are classified based on the interconnect, sizing, temperature management, clustering and power optimization.

The essential rule behind floorplanning using the Simulated annealing [9] is the delineation of geometric relationship while the logical based approach manages the outright relationship specifically. The calculation turns out to be versatile and powerful as far as wirelength minimization in spite of repetitive division scaled well and demonstrated its accomplishment in minimization of wirelength and strengthening based floorplanning.

Srinivas Katkoori and Pradeep Fernando (2008) [10] considered an algorithm using multi-objective genetic for achieving wirelength and area best floorplanning.

To allocate rank for the solutions, the non-domination concepts are used.Fruitful lessening of inductive exchanging clamor can be refined by the accompanying: Reduce the quantity of yields that switch at the same time by isolating them into bunches with each gathering having various defer supports embedded into their information ways  Use the most minimal evaluated sink present or low-clamor yield cushions as long as speed isn't an issue  Place the at the same time exchanging yield or bidirectional cushions together furthermore, disperse power and ground cushions among them as indicated by their relative commotion rating  Assign static and low recurrence input cushions to higher inductance bundle pins  Reduce the viable power and ground stick inductance by allocating as numerous power and ground cushions as could be expected under the circumstances. By considering this as a main priority the proposed Algorithm is composed.

## III MODIFIED FLOORPLANNING WITH MINIMUM WIRELENGTH

In the wire length placement refinement, apportioning the switch part and therapist part together. Since TSV check is not any more priority. In Figure 3, contract is performing amid the switch process. After each move of the module in the switch part, we contract modules in each layer iteratively to get the most limited wire length. Restore the outcome with the most limited wire length toward the finish of the program.

(1) **Reading the files** of benchmark circuits.
(2) **Generation** floorplan solution.
(3) **Initialization:** temperature Temp0 according to (1).
(4) **Shuffle** the current solution arbitrarily and produce a newsolution.
(5) Once the **new solution** is correct compared to the available solution, replace the current solution with
the new solution
(6) If the number of **reputations** at the current temperature ranges Markov chain the length, Move to the
next step, otherwise go back to step (4).
(7) **Temperature diminution** according to the cooling schedule: Temp (j) =α Temp (j-1).
(8) **Redo** steps 4-7 until the criterion is achieved.
(9) Output the better solution obtained so far.

## III RESULTS AND DISCUSSIONS

The results are taken in the AMI33 and AMI 49 bench mark details of benchmark circuit has good results when compared to traditional method which is discussed in Table I. The constraints of the Simulated Annealing based algorithm are explained in the following: (a) The cooling factor is 0.95. (b) Markov chain length takes 40*n, (n is the number of modules of benchmark) . (c) The algorithm ends while the temperature is minimum than 10-6 Temp0 or the number of accepted agitation is less than 1% at a minimum temperature. The chip area and percentage of dead space are explained in Table II which includes the comparisons between previous work and the proposed work. Floorplan area is calculated by minimum bounding box which includes all modules. Floorplanning results of ami33 and ami49 obtained by the proposed MFMW algorithm. This algorithm can generate a better floorplan whose dead space percentage is less while consuming minimum operation time.

**Table.I Comparisons of various algorithms using AMI33 and AMI 49**

| Number of Placement Constraints | Floorplan Constraints method [5] | | Proposed Floorplanning | |
|---|---|---|---|---|
| | Time (sec) | Wirelength $10^6$ | Time (sec) | Wirelength $10^6$ |
| 4 | 18.0 | 0.0248 | 16.23 | 0.0221 |
| 8 | 20.04 | 0.0252 | 17.91 | 0.0258 |
| 12 | 19.89 | 0.0252 | 19.88 | 0.0214 |
| 4 | 25.63 | 0.0252 | 22.12 | 0.0223 |
| 16 | 24.05 | 0.0252 | 24.20 | 0.0269 |
| 18 | 41.99 | 1.280 | 28.99 | 0.0480 |
| 20 | 42.37 | 1.931 | 29.28 | 0.0482 |
| 22 | 357.39 | 1.467 | 228.11 | 0.977 |
| 24 | 374.71 | 1.448 | 344.71 | 1.403 |

## IV. CONCLUSION

Entire modules have a substantial concentration on the diminution of chip area and total wirelength in slicing floorplan. Already are various floorplan representation have been discussed in this paper. From the analysis, O-tree representation and B*-tree representation is most effective when compared to all representations but with minimum flexibility. At foremost, the disadvantages of dead space are investigated and an instinctive and profligate method is proposed to find the equitable part of component. Then, a tormenting for standardized expression is improved to produce new solution, and the proposed simulated annealing algorithm is opted for the best floorplan solution. Experimental results demonstrate that the proposed MFMW method attains less area on the commonly used AMI33 and AMI 49 benchmark circuits.

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