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High speed VLSI Squaring unit of Binary Numbers Design with Yavadunam Sutra and Bit Reduction

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Abstract: ***Vedic Mathematics is an ancient Indian algebra in which 16 sutras are used to measure. For excellent performance, most high-speed applications such as cryptography and digital signal processing need powerful and high-speed multipliers. Squaring is a specific case of multiplication. A specialized squaring device can greatly boost the measurement period and significantly reduce the delay. This study discusses the concept of a new square architecture utilizing Vedic-mathematics sutra "Yavadunam." The proposed method uses the amount deficit from the closest base to calculate every operand's circle. The square of a larger number of magnitude is reduced by this method to a smaller multiplication of magnitude and an addition operation.***

Index Terms*: *Squaring, Vedic Mathematics, Yavadunam Sutra , Bit reduction

I. INTRODUCTION

The new developments in science and technology contribute to solutions at high speed. Digitalization has allowed us emphasis on system pace as opposed to other outcomes of performance [3]. Squaring operation plays an important role in most high-speed applications. Multiplication and squaring operations are the most important of all arithmetic operations. Much architecture was implemented to achieve high performance [8]. Each circuit's efficiency measurement is determined by two key parameters of region and rate. Multipliers are used in many programs to locate the squares or other control process instructions. Therefore, strong multipliers are used to get the square of a binary integer. Some of the request multipliers like Braun, Wallace tower, Dadda multiplier are used in most high-speed applications[9-12]; Booth multiplier is used in Baugh-Wooley 2's methods[4]. The Vedic multipliers are also evolving into the patterns other than traditional multipliers.

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Vedic sutra-based multipliers, most probably Urdhava Tiryagbhyam and Nikhilam Sutras, are widely used in practice [2], [5]. Comparing Vedic multipliers with conventional ones Vedic multipliers are fast and take up less area [1]. Yavadunam Tavadunikrtya Vargancha Yojayet is a typical sutra for squaring.High speed and area-efficient Yavadunam Square design is introduced in this sense for binary number. The proposed architecture's algorithm is also based on ancient Indian Vedic mathematics [3, 4]. The interpretation of the' Yavadunam ' Sutra algorithm is' whatever the deficiency subtracts the deficiency from the amount and writes the deficiency opposite the Line. The Yavadunam algorithm transforms the large operand Square into the smaller operand Square with additional activity.

II. LITERATURE SURVEY

Vedic Mathematics applies to a collection of 16 mathematical formulas or sutras and their consequence formulas. sutra is meant for numerous mathematical computations, such as division, multiplication, addition, square root, circle, etc. Only three sutras are to conduct squaring procedure among the 16 sutras[6]. The sutras of squaring activities are the following:

1. Yavadunam.
2. Ekadhikina Purvena
3. Dwantwa yoga.

In this chapter, we present a brief discussion of Indian Vedic mathematics ' Yavadunam Sutra that is useful for the rest of this article. Here, together with illustrations, the various Yavadunam Sutra cases are clarified. This Sutra can be used to get numbers squares similar to power bases of 10[3-5]. Two situations are known to locate a number square I when the amount is less than the base (ii) when the number is higher than the base. For case I the deficit is obtained by subtracting the amount from the point, but the surplus is obtained by subtracting the base24 from the number for case (ii). In both instances, by squaring a diminished deficit / surplus ratio, the correct aspect of the outcome (RPR) is produced. In case I the left portion of the outcome (LPR) is determined by subtracting the shortfall in the original number, but in case (ii) the right portion of the result (RPR) is the actual value of the surplus with the original number. Finally, the LPR and RPR are concatenated to locate a decimal number's final circle.

III. METHODOLOGY

The Vedic Square method discussed in Section 2 can be mathematically proven as follows, If the numbers below and above the power bases of 10 can be viewed as (X + Y) where X is the basis and Y is the surplus. The sutra of Yavadunam was extended to the system of binary numbers and found to work exactly the same as in the system of decimal numbers. To measure the square of any n-bit binary number in this proposed method, the basis is taken as 2n. This implies the base is taken as 100 for a 2-bit binary number, the base is taken as 10,000 for a 4-bit integer, and so on. Since the value taken is 2n greater than the n-bit binary sum, the number deficit can be computed by subtracting the total 2n n-bit binary number. So in this article we find only the deficit case of Vedic mathematics ' Yavadunam sutra where the amount is less than the base and we adopt the measures as per the sutra mentioned. Subtracting a n-bit binary integer from base 2n again is almost the same as taking the 2's number complement itself[13]. This can better be described by using an instance i.e. taking a 4-bit binary number say 1101; the basis is then calculated as 2n i.e. 24= $(16)_{10}$= $(10000)_2$. The 4-bit binary number 1101 subtracted from the base 10000 results as 0011 which is the nearest base deficit which is exactly the same as the 2's complement to the given number 1101 i.e. the 2's complement to the 4-bit binary output number 1101 is 0011. Next, the 2's number complement is revealed, which reflects the number deficit from the closest basis. A left shift operation can also conduct the subtraction function of the deficit of the n-bit binary number (2's addition to the specified n-bit binary number) from the n-bit binary number[15][14]. This can be described by a single bit discarding the (n-1)th bit and assigning the value' 0' to LSB as the left shift operation of the n-binary count.

This assertion can also be understood by the above illustration, since the effect of the left shift operation on the 4-bit binary number "1101" ignoring and assigning LSB to' 0' is "1010," which is exactly the same as the performance we obtain by subtracting the 4-bit binary number "1101" deficit "0011." After the shift process, the result is exactly the same as subtracting the deficit from the specified binary number output, and this effect is the right part of the equation.

A generator is then used to produce the LPR as a shortfall calculation. The argument "subtracting a n-bit binary number from base 2n is analogous to having the 2's number counterpart" can be proved as if' a' is the single-bit integer, then

=a+a'=1

For n-bit of number

a[n-1:0]+a'[n-1:0]=11111…..11111(n bits of 1)

adding logic 1 in both sides of equation (3)

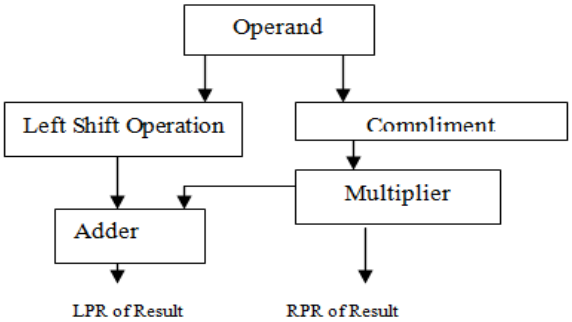


Fig 1. Block diagram for the proposed squaring architecture

The proposed method is to change the current structure of the square to achieve improvement in area, speed and power. This standard methodology of conversion is practiced and thus weight loss is rendered by getting rid of the Most Important Piece. In order to get the square of the given number, Yavadunam Sutra is applied after bit reduction. The number of pieces to the squaring structure is limited by introducing this change to the current architecture. It is also possible to reduce the number of components required while minimizing energy and lag. Let us find a 4-bit square binary number A3A2A1A0. Reduction of weight is allowed and replacement of the MSB.

Now the software output is A2A1A0, a binary number of 3bits. Now the 3-bit number foundation is 8. The squaring architecture's performance will be over 4 bits. Since the input is 4 bits, the output will be 8 bits if the squared number is greater than 2N-1 and if the squared number is less than 2N-1 the output will be 6 bits. Binary numbers squaring involves two modes. One of the modes is when the deficiency is positive, i.e. if the number given is greater than the base value of 2N-1. Of example, when number is 12 the base value is 8 and the deficiency is+ 4. And the other type is when the deficiency is negative, i.e. if the number given is less than 2N-1, the base value. If the number is 4, for example, the base value is 8 and the deficiency is-4.

Mode: 1The number given exceeds 2N-1.

Mode: 2The number given is lower than 2N-1.

Mode algorithm: 1

INPUT: OUTPUT A3A2A1A0: B7... B2B1B0

Step: 1 Reduce the input weight by removing the MSB, now input becomes the deficiency A2A1A0.

Step: 2 Let the deficiency be D2D1D0= A2A1A0

Step: 3 Square the deficiency, squaring output= X5... X2X1X0 Carry= X5X4 X3 and now LHS= X2X1X0= B2B1B0

Step: 4 Add the deficiency and input A3A2A1A0+ D2D1D0= Y4Y3Y2Y1Y0

Step: 5 Add the above output to carry LHS Y4Y3Y2Y1Y0 + X2X1X0= B7B6B5B4B3= RHS

Step: 6 Concatenating LHS and RHS, the output is final.

Mode algorithm: 2

INPUT: A3A2A1A0 OUTPUT: B5.. B2B1B0

Step: 1 Reduce the output weight by eliminating the MSB, now A2A1A0 is input.

Step: 2 Take the two A2A1A0 complement, the performance is the shortcoming. Let the deficiency be D2D1D0= A2A1A0

Step: 3 Square the deficiency, squaring output= X5... X2X1X0 Carry= X5X4 X3 and now LHS= X2X1X0= B2B1B0

Step: 4 Subtract the deficiency from the reduced bit number A2A1A0= D2D1D0= Y2Y1Y0

Step: 5 if the subtractor output is positive then add the above output to the X5X4 X3 carry.

Y2Y1Y0 + X5X4X3= B5B4 B3= RHS

Step: 6 If the output of the subtractor is negative, delete the Y2Y1Y0 output from the X5X4X3 hold. i.e. X5X4X3= B5B4 B3= RHS= Y2Y1Y0.

Step: 7 LHS and RHS concatenating, the performance is B5B4B3B2B1B0= square of A3A2A1A0 All modes are merged into one architecture.

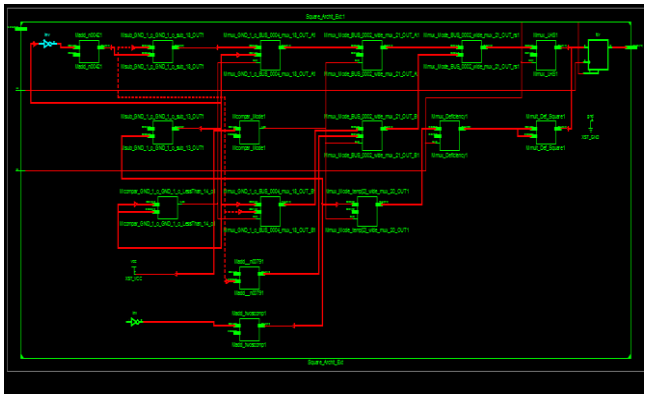
You may classify the number greater than or less than 2N-1 from the number's Most Significant Piece. The multiplexer control signal relies on the most important bit of the Output i.e. AN-1.If the number of the MSB is 0, the number is complemented after bit reduction and squared afterwards. If the number MSB is 1 then the number is immediately subject to bit reduction and squared thereby missing the additional block of two.

The control signal for selecting the adder or subtractor depends on the most important bit of the input i.e. AN-1.When the number is greater than 2N-1,AN-1 is 1 and adder is selected and the output of the adder is applied with the carry. In other instances, if the number is less than 2N-1, AN-1 will be 0 and the choice of the subtractor. The control signal for selecting the carrier or subtractor is similarly dependent when Y N-1 is 0, the subtractor will be applied otherwise.

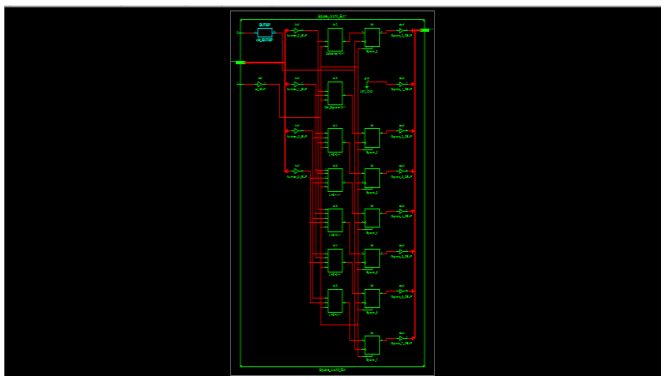
IV. EXPERIMENTAL RESULTS

Simulation output:

RTL schematic:



Technological schematic:



Design summary:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	7	2400	0%
Number of fully used LUT-FF pairs	0	7	0%
Number of bonded IOBs	14	102	13%
Number of BUFG/BUFGCTRLs	1	16	6%

Timing summary:

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Timing Summary:
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Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: 2.829ns
   Maximum output required time after clock: 3.597ns
   Maximum combinational path delay: No path found
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V. CONCLUSION & FUTURE SCOPE

A novel Vedic Squaring structure was suggested in this article using Vedic Mathematics ' Yavadunam sutra. The proposed squaring model is evaluated from 8 bits to 64 bits of operand size in terms of combinational path delay and system utilization. Using Xilinx ISE 10.1 code, the proposed squaring circuit is successfully synthesized and simulated and implemented on FPGA's 4vlx15sf363-12 computer. The synthesis result of the proposed squaring techniques is compared with various existing squaring and multiplication techniques as described in the literature, the results of comparisons show that the proposed architecture of Vedic Squaring appears to have improved speed and area. Nearly all arithmetic operation, squaring unit is usually used in signal34 processing to find the transforms or inverse transforms. More to this the cryptography's backbone is the squaring process. For high-performance computer graphics, cryptography, ALU circuits, and many digital image processing applications, the proposed Squaring architecture can be useful in terms of both speed and space.

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