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Design of XOR and XNOR Based Full Adder Circuits

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ABSTRACT: ***This paper has a XOR / XNOR gate circuits produces separate and establishes a simultaneous XOR - XNOR function.. Due to stubby yield capacity and short-circuit energy dissipation, the power utilization and latency of these circuits is increasing A new one-bit adder hybrid circuit is chosen built on the effective gates of xor xnor or xor / xnor. Each prefer circuit has its own advantages as it is known for its high speed, low current drain, short delay product (PDP), galvanic ability, etc. Simulations of the planned models were carried out using Mentor Graphics to see the quality of these projects. The simulation results are based on the 130-nm CMOS engineering design. A recent technique of transistor sizing is implemented to improve the circuits ' PDP.***

Keywords: ***Transistor sizing method, PSO, XOR–XNOR, Output driving capability, DPL***

I. INTRODUCTION

Today, predominant electronic systems are treated separately in every part of life and the usage of portable devices has been increased tremendously. These devices require to have less power utilization and high speed. While designing a system, power utilization is a parameter which is to be rectified for better system performance. The efficiency that depends on the execution of divider, comparator, multiplier, and adder which comes under arithmetic circuit which in turn shows the impact on numerous digital applications. In Most of the circuits that perform arithmetic operations, full adder plays a important role, because Total adder output affects the entire process. For algebra, adder loops are used logic circuit designs, processor chips. there are 2 types of full adders in which the circuits are existed till now.

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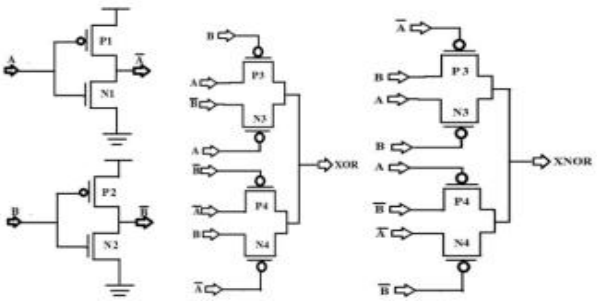
They are the static and the dynamic full adders. The static full adders is having high reliability and they are simple having low power utilization whereas the dynamic full adders have less on chip area. The designs in the circuits includes the characteristics of enhance the W/L ratio of transistors is one way to reduce the circuit energy lag material while minimizing the problems associated with rising the input voltage. The usefulness of various electronic systems is the output of mathematical loops,such as many adder, multiplier and divider.

II. XOR AND XNOR GATES ANALYSIS

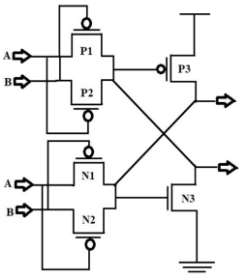
XOR-XNOR CIRCUITS: Using the utilized xor-xnor circuits, new hybrid full adders are proposed. These circuits use different logic styles. Each proposed full adder use simultaneous Xor and Xnor circuits and 2to1 multiplexer structure. The major consumer in the full adder is Xor-Xnor gate. This gate is having many applications in digital circuit design. Hence, The electric energy consumption of the full adder might be reduce by using the optimum design of this xor-xnor gate. Many efficient circuits have been implemented using Xor-Xnor gates. In fig (a) Active XOR/XNOR gate circuit is scrawl designed comprising of 8 transistors. Construction of this circuit is based on double pass-transistor logic (DPL)style. Since it requires Two flexible intake doors not on the loop critical path and also, since these gates (NOT) .The performance power must be powered by the width of the transistors should be increased which becomes a major drawback avoiding the usage of this circuit. In addition to this problem, there comes another one creating an medial node with a very high capacitance. Consequently, this part of the circuit simple terms-circuit capacity and overall power dissipation were extensive. The critical path lag will also be decreased in the optimal PDP scenario. moderately. So, to modify the above circuit i.e Fig.(a). We The XOR / XNOR gate example has been planned for each circuit consisting of six transistors.

Critique For Xor And Xnor Gates

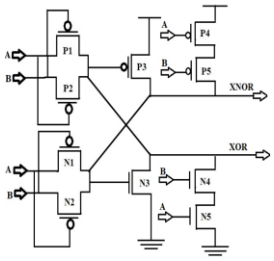


Fig(a) Full-swing XOR/XNOR circuit

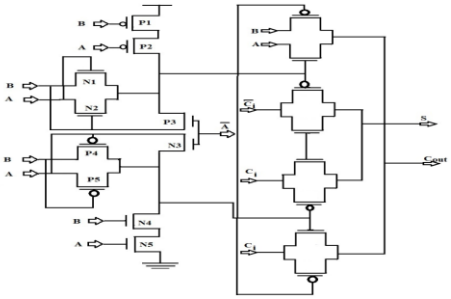
Fig (b) The XOR–XNOR full-swing gate is proposed with a six transistors. The dual additional input transistors (N3 and P3) recovers the faulty logic in output nodes (XOR and XNOR).If AB=00 is the same, 11 outputs are the same.
This loop, though, experiences from either the largest latency in the worse scenario, because once the inputs shift from AB = 01, 10 to AB = 11, 00, the outputs hit their total voltage level in two phases. To discuss the problem, the transistors n2 (xor output) and p2 (xnor output) transfer logic "1" and logic "0" in both when outputs equal to AB = 10. Such poor reaction phenomenon is the worst in minimal-voltage service and also raises quick-circuit current if one of the inputs (XOR or XNOR) is high impedance and the circuit input not yet been fully implemented the flow of the short circuit moves via the device . Even if the transistor scale is not properly chosen by this circuit, the circuit may not always be regulated properly. Fig (c) To address the long wait issue and work in low voltage inputs, two nmos transistors (for AB = 11) and two pmos transistors (for AB = 00) are attached to the XOR / XNOR outputs. The benefits of this design are perfect driving efficiency, full swing performance and robustness toward transistor size and voltage source scaling. Fig (d) It is having 20 transistors and compared to other transistors it is having less power delay. The driving capability is also better than the other circuits.



(b)



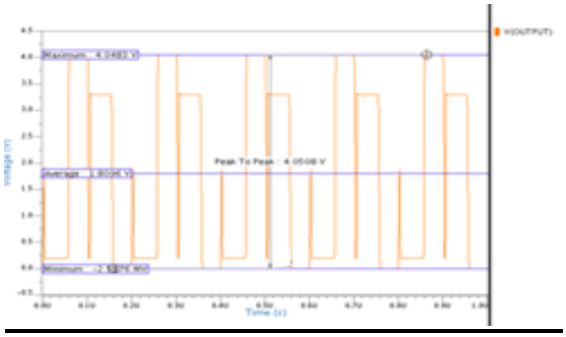
(c)

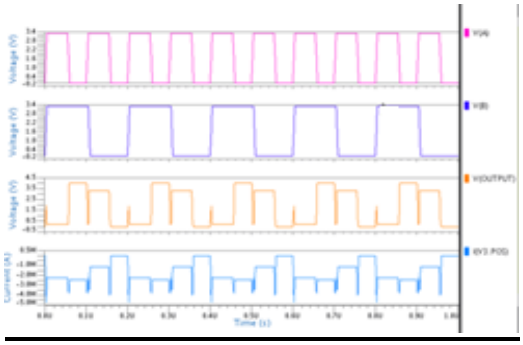


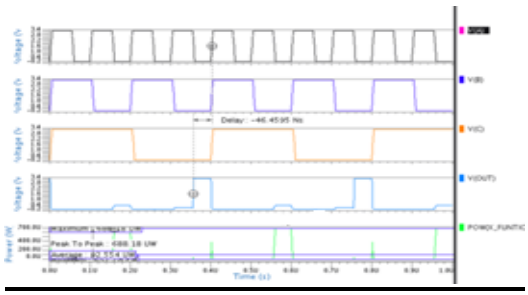
(d)

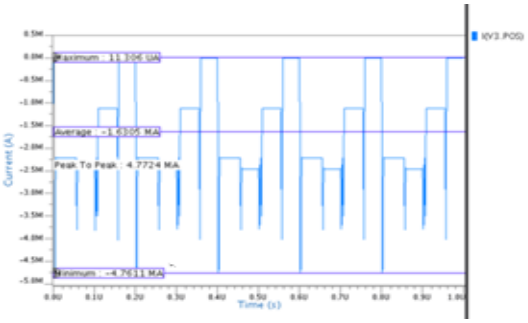
Fig(b),(c) and (d): XOR/XNOR circuits

III. SIMULATIONS/OUTPUTS:

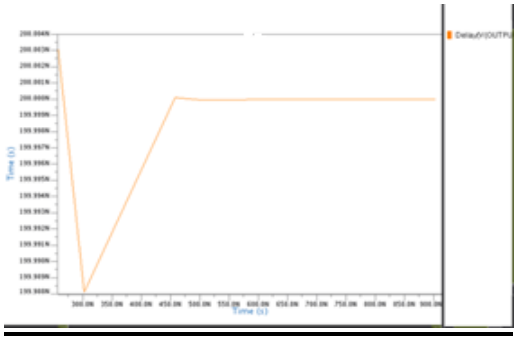




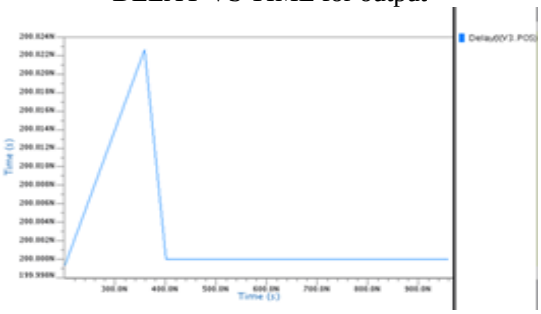




Outputs in terms of power

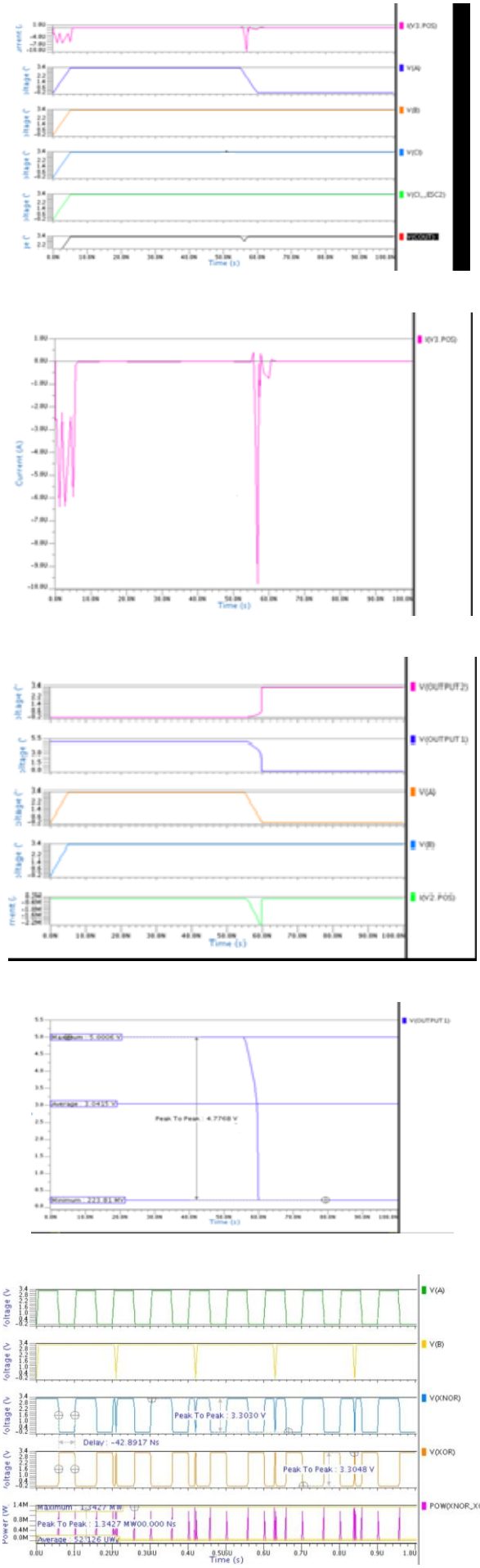


DELAY VS TIME for output



DELAY VS TIME FOR POWER

Simulated results of XOR XNOR Gates for Fig (a)



Simulated results of XOR-XNOR Gates for Fig (b),(c),(d)

Table for power delay product

DESIGN	POWER (watts)	DELAY (us)	PDP
Fig(a)	6.47	41.36	267.5
Fig(b)	4.73	35.62	168.4
Fig(c)	6.82	46.98	320.4
Fig(d)	4.8	59.1	241.1

IV. ADVANTAGES

1) Circuits based on the Transistor logic type transfer (PTL) introduced which eliminates the problem of excessive power consumption.

2) Two transistors have been removed and modified from the XOR–XNOR circuit for through the circuit's energy dissipation.

3)To eliminate and the slow response problem and enable the circuits to operate successively , two NMOS transistors and PMOS Transistors are connected separately to XOR and XNOR outputs.

4) Occurrence of great driving capacity, maximum-swing performance.

5)The question of increasing the size of a transistor and the doubling of the input voltage is over.

6) Circuits have high speed also the response time have been reduced.

V. CONCLUSION:

We initially tested the XOR–XNOR circuits and their characteristics. Also the circuit has a positive feedback on the outputs which results in the increase of the size of transistors, delay, and excessive power consumption making the circuit avoidable. It is the most important components of any software for a digital system. The PDP is a calculation of the increased energy per arithmetic circuit operating period. Different full adder architectures have been reviewed and simulated utilizing mentor graphics 130 nm technology. The CMOS adder offers both logic 0 and logic 1 based on the output comparison of different adders. Also it operates with a extremely high speed an maintains a good accuracy. Simulation results showed us that the proposed circuits have got high speed and energy than the previous ones.

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