International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-2, December 2019

CMOS Transistor and Applications

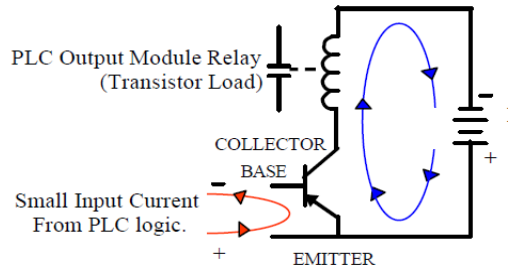
Ahmed H. Almutairi, Esam ALsumait

Abstract: ***This paper is reviewing and discussing the CMOS transistor and how to be used in Logic gates and the power consumption during operation and the application.***

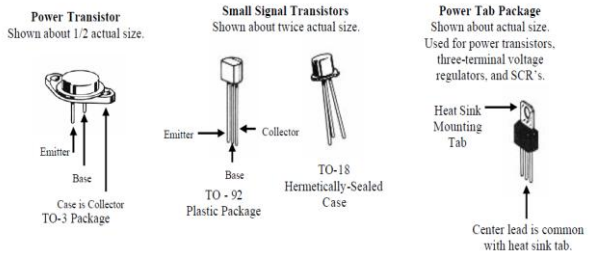
Keywords: ***Semiconductors, Transistors, Logic Gates, CMOS transistors, Power, Applications, Conclusion***

I. INTRODUCTION

[1] Transistors are semiconductor devices that can behave as a signal amplifier or behave as a solid state switch shown in the below fig.
and a low current input signal passing from emitter to base is able to control a much current that will pass from the power supply of the system, passing to the emitter to collector of the transistor , passing to the load, then passing again the power supply.
Transistor is shown as this figure:



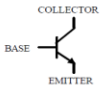
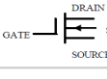
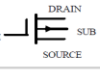
Notice that: direction in this emitter of this transistor illustrates the conventional current flow's direction (+ ve to – ve) inside this shown transistor. We are going to speak about types of transistors and the designs of these transistors. Some of these transistors belongs to JEDEC Standards, are defined by (TO) designations Transistor Outline. Designs of many cases are illustrated as shown in figure:



Revised Manuscript Received on December 30, 2019.
***** Correspondence Author
Ahmed H. Almutairi*, Department of Electronic Engineering, BS West Virginia university Charlottesville.
Esam alsumait, Department of Medical Electronic in College Of Technology, PAAET Adailiyah, Kuwait.

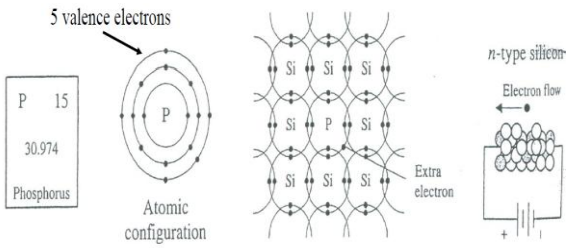
II. TYPES OF THE TRANSISTORS:

[2] Three main types of the transistors and these three types , each has its unique characteristics, and design and symbols parameters, and its own applications. The following and the below papers show extra details an information and applications of those three types of transistors. many types of the transistor of the special function are found which are not fall onto the categories that has mentioned before ,for example and illustration the (UJT) uni junction transistor which is used for delay applications and SCR firing time.
- Bipolar transistor is defined as devices which has current driven and has a almost small input impedance. It is exist as PNP or NPN types.
- Field Effect Transistors are devices that have voltage driven characteristics and that have a large input impedance.

DEVICE NAME	SYMBOL		CHARACTERISTICS
	NPN	PNP	
Bipolar Transistor			A small input *current* signal flowing emitter-to-base in the transistor controls the transistor emitter-to-collector internal resistance. Used as amplifiers or switches in a wide variety of equipment ranging from small signal applications to high power output devices.
	N-CHANNEL	P-CHANNEL	
FET Junction Field Effect Transistor			Input *voltage* signal is applied to the gate-source junction in a reverse biased mode, resulting in a high input impedance. Input signal varies the source-to-drain internal resistance. Applications include high input impedance amplifier circuitry.
	N-CHANNEL	P-CHANNEL	
MOS Metal Oxide Semiconductor Field Effect Transistor			Similar to the JFET above except the input *voltage* is capacitive coupled to the transistor. The device is easily fabricated, inexpensive, and has a low power drain, but is easily damaged by static discharge. Computer chips utilize CMOS
IGBT Insulated Gate Bipolar Transistor			Similar to the Bipolar NPN above except the input *voltage* is capacitive coupled to the transistor as with the MOSFET devices. Main application is as a switch for the output section of small and medium size Variable Frequency Drives (VFD's).

III. SEMICONDUCTORS:

[3] Material which not allows passing of electrons are called insulator .Material which allows Passing of electrons are called conductor. Material which conductivity is between insulators and conductors is called Semiconductors.



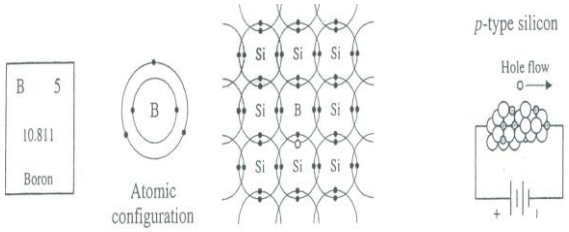
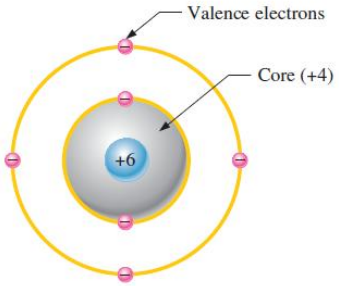


Diagram of a carbon atom:

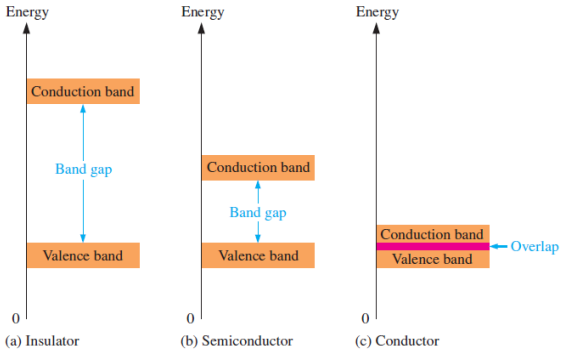


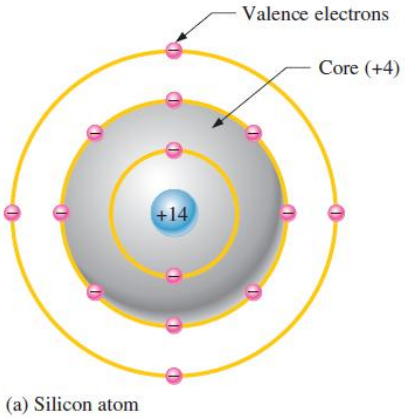
Definition of the Band Gap : the interactions In solid materials among atoms such asthe valence shell onto the energy levels band .

This Valence electronics confined for such a band. And while the electron needs or achieve extra energy, it could go from the valence shell and be a free electron, and it will be found on the conduction band.

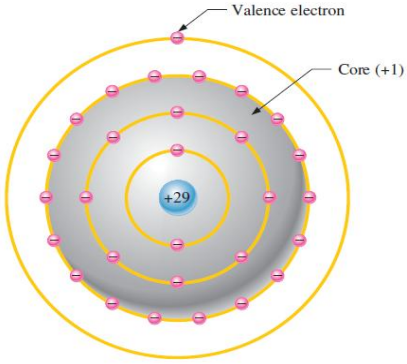
The difference in energy between valence band and conduction band and is called a band gap or energy gap. It is the required energy which a valence electron has to move from this valence band to that conduction band.

[4]The energy gap or the band gap or is the difference between two energy levels





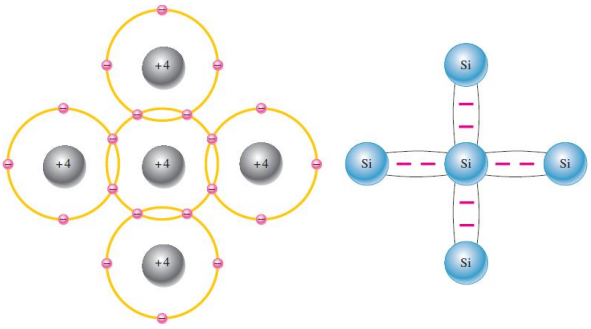
(a) Silicon atom



(b) Copper atom

In germanium we find that The valence electrons are in the 4th shell but these are in the 3rd shell in silicon and close to the nucleus. it means that valence electrons of the germanium arein energy levels higher than these in the silicon and needs a lower amount of energy to move from the atom. it makes the germanium not more stable at high temperatures. so silicon is a most ommonly used semi conductive material.

Covalent Bonds that shown in the below Figure illustrate how the atom of the silicon direct itself with 4 atoms of silicon to make the crystal of silicon,



(a) The center silicon atom shares an electron with each of the four surrounding silicon atoms, creating a covalent bond with each. The surrounding atoms are in turn bonded to other atoms, and so on.

(b) Bonding diagram. The red negative signs represent the shared valence electrons.

Transistors:

Transistor Types:

[5]MOSFET and BJT And JFET(MOSFET) Metal Oxide Semiconductor FET (BJT) Bipolar Junction Transistor PNP and NPN Junction Field Effect Transistor (JFET) N-channel and P-channel (N- and P-channel) The enhancement type and (N- and P-channel) Depletion type

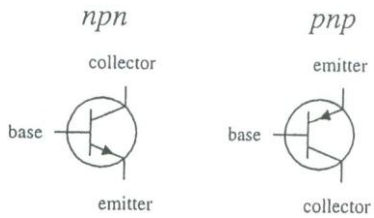
BJT JFET MOSFET

Types of BJT: PNP and NPN

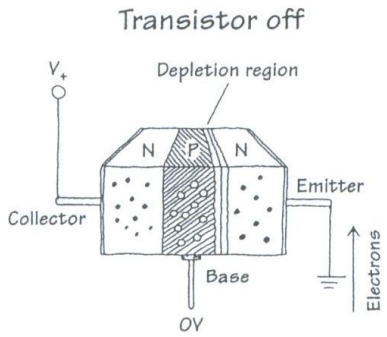
[6] NPN is a Low input current and +ve voltage applied at the base (whichVE less than VB)

Permits a large current to Pass from collector to emitter.

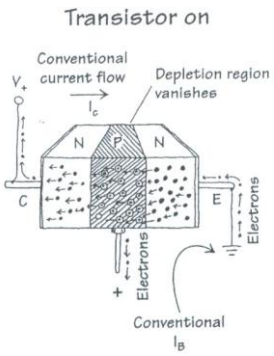
PNP is a low output current and –ve voltage at the base (which VE higher than VB) Permits a larger current to pass from emitter to collector.



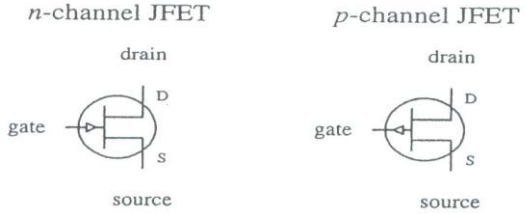
BJT NPN: the electrons which in the emitter are not accepted from moving to the collector side due to the PN junction. If zero voltage is applied to the base of transistor
PN junction between base and the emitter becomes a reverse biased which result to forming of a depletion region that prevents the moving of the current. If we apply –ve voltage to the base the transistor .



Some electrons are being exit in the base and due to the P type base is too thin,
Electrons which exit from the emitter will be close to the collector side and they will pass into the collector. as the increases of base voltage , it will result that the electron will flow from the emitter to collector and +ve current flow is in the direction Reverse to the Direction of electron .

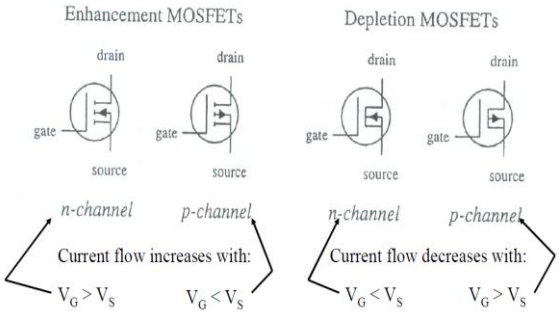


JFET stands for Junction field effect transistors as BJTs
[7] P and N channel are two JFETs types, In the N- channel JFET, a Negative voltage is applied at the gate (witch VS is greater than VG) decreases current Passes from drain to source. It operates at VS smaller than VD.In P-channel JFET, a Positive voltage is applied at the gate (whichVS is smaller than VG) decreases current flow from source to drain. at VD smaller than VS.



MOSFET: [8]Metal oxide semiconductor FET
to get the high input impedance at the gate , a metal oxide insulator is placed at the gate

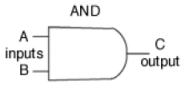
Depletion type, At VS = VG
Almost on, when maximum current Passes onto drain source channel If a voltage is applied onto the gate and result to the drain source channel higher resistance to the flow of the current.
Enhancement type: At VG=VS
Almost off which no current Passes through drain-source channel.
if the voltage is applied at the gate the drain-source channel decreases resistance to the flow of the current .



IV- Logic Gates:
[9] Basic gates are OR AND XOR NANDNOR NOT XNOR
In truth table it shows the Relationships between inputs and outputs are outlined
Truth Tables

AND gate

→ C = A • B



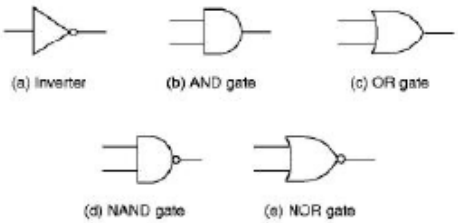
A	B	C
0	0	0
1	0	0
0	1	0
1	1	1

OR gate

→ C = A+B

A	B	C
0	0	0
1	0	1
0	1	1
1	1	1

Logic Gates & Symbols



OR gate :
Output is one (HIGH)
If one of the inputs is one (HIG)
Output is zero (HIGH)
If all inputs are zero (LOW)

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOR gate
It is the reverse of OR

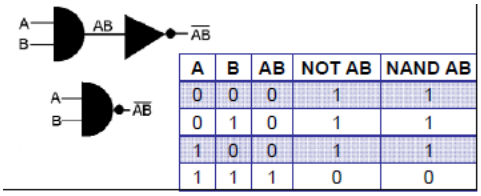
NOR gate cont.

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

NOT gate :
Output is one (HIGH)
If input is Zero (LOW)
Output is Zero (LOW)
If input is one (HIGH)

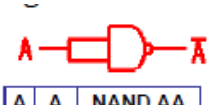
A	A'
0	1
1	0

Logical Equivalence: NAND gate is and gate neither followed by nor gate

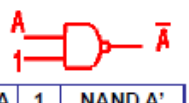


A	B	AB	NOT AB	NAND AB
0	0	0	1	1
0	1	0	1	1
1	0	0	1	1
1	1	1	0	0

NAND gate Like NOT gate :
• The below figure shoes 2 ways that a NAND gate Can be implemented to give a NOT gate.
• We could achieve it using NOR gates.

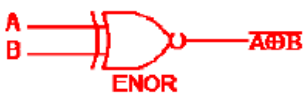


A	A	NAND AA
0	0	1
1	1	0



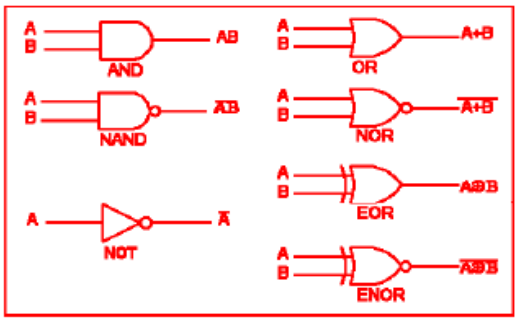
A	1	NAND A'
0	1	1
1	1	0

EXNOR gate :



2 Input EXNOR gate		
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

Logic gate symbols



NAND gate: It is a AND-NOT gate which is equal To AND gate with next NOT gate.

NAND gate Cont.

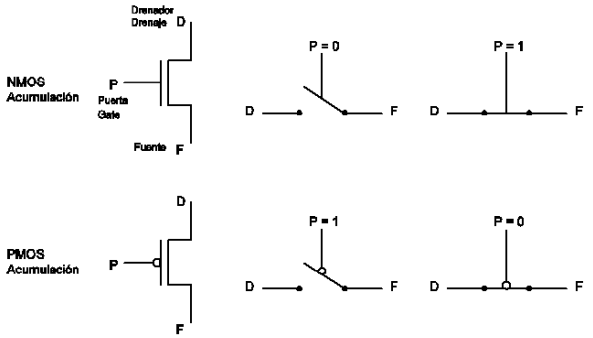
2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

AND Gate:
Output is one (HIGH)
If all input are one (HIGH)
Output is zero:
If one of the inputs is zero (LOW)

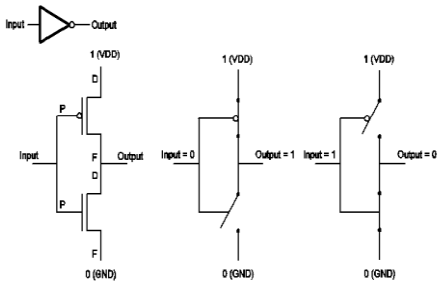
2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

IV. CMOS TRANSISTOR:

[10] The transistor acts as a switch. For NMOS transistors, if the input is "one " so switch is on, if " zero " it is off. And for the PMOS, if the input is " Zero " the transistor is on, and if " one " the transistor is off. It can be represented by the below figure:

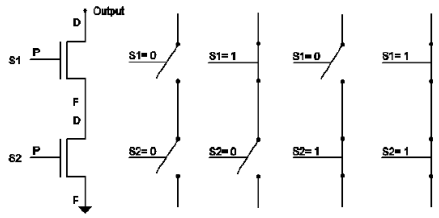


IF the circuit has both PMOS and NMOS transistors it will produce CMOS transistor for this combination.

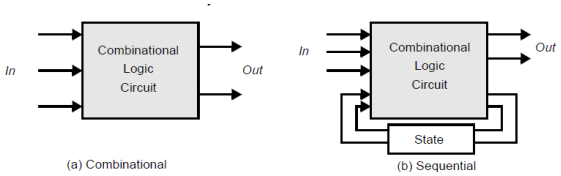


[11] We illustrated implementing a logic gate using transistors. And To produce the other of logical gates we will produce the behavior of the transistors when it will be connected in a "series" or in a "parallel" method .when two NMOS transistors are combined in series, we get an implementation as the following figure :

Output = 0 si S1=1 i S2=1



A sequential circuit Contains a module that holds the state and a combinational logic gates. Such as of the following circuits oscillators, registers, memory, and counters:



To produce a certain logic function, There are such circuit styles with the inverter, is evaluated containing energy, power, area and speed,. Based on the application,

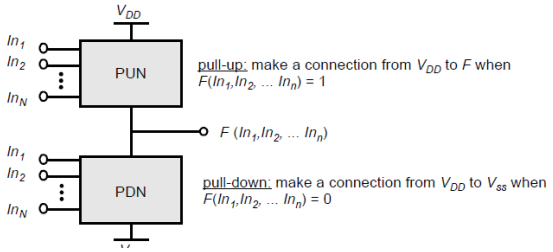
V. DESIGN OF STATIC CMOS:

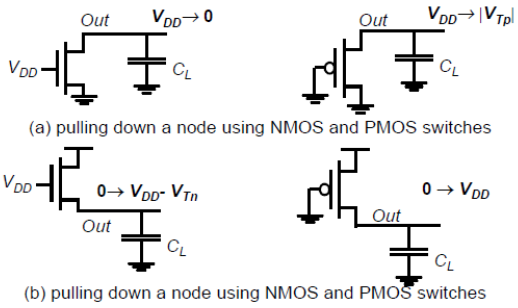
[12] One of The most commonly used is static complementary CMOS. With multiple inputs.

The benefit of the CMOS combination is low power consumption And better performance and low sensitivity to noise.

Complementary CMOS

[13] Combination of two networks produces A static CMOS gate and it is called (PUN) the pull-up network





VI. THE POWER CONSUMPTION IN CMOS LOGIC GATES

[14] We have to minimize the Power consumption in all circuits component which is a function of high frequencies and we have to control the maximum frequency working with the circuits to minimize the power consumption,

There are 2 components that specify the consumption of the power in the circuits of a CMOS transistor:

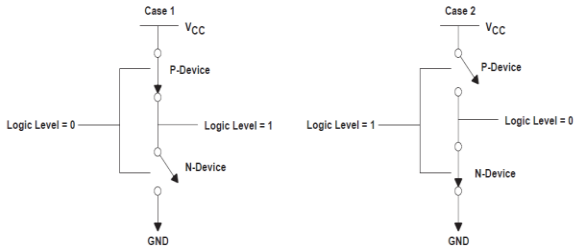
VII. DYNAMICS AND STATICS AND POWER CONSUMPTION

[15] CMOS device has little consumption of static power, because of the leakage current. if switching at a high frequency,

The consumption of the dynamic power: is increased by a capacitive output load discharging and Charging

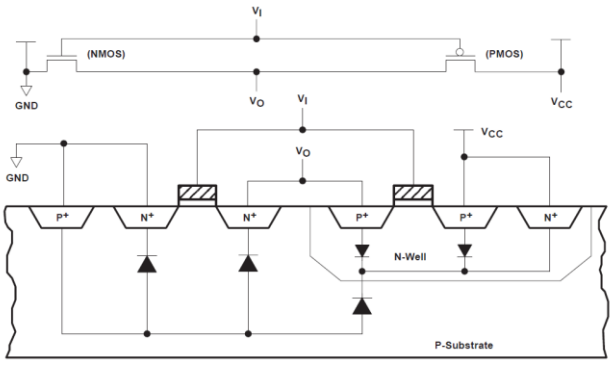
Static Power Consumption

[16] To show how static power consumption operates The low-voltage device has CMOS transistor inverter in the output and input stage, consider the below figure :



it shows it is a little amount of consumption of static power because of reversing bias leakage among the substrate and diffusion regions. And it can be illustrated with a easy model that explain the

parasitic diodes of a CMOS transistor , as illustrate in the below :

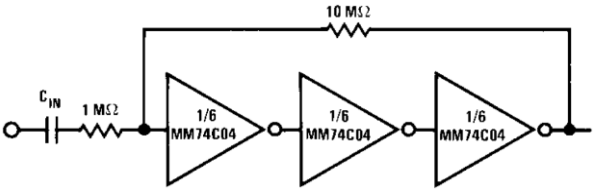


VIII. THE CONSUMPTION OF THE DYNAMIC POWER:

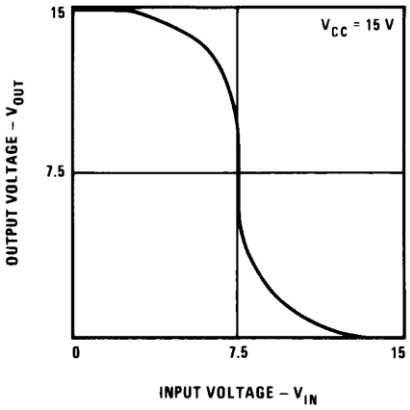
[17] It could be measured by using the addition (PL) The power consumption of the capacitive load and (PT) the consumption of transient power.
The consumption of Transient power is because of the current which pass when the CMOS transistor of this device is switching from one logic state to another.

IX. CMOS APPLICATIONS:

[18] Cascading the basic amplifier block though Cascading Amplifiers for Higher Gain shown in the below figure the high gain amplifier could be implemented. the number of the used stages will produce The times of gain .

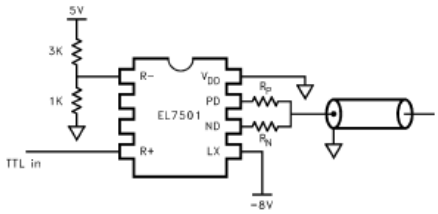


in monolithic form the complementary P and N channels MOS transistors are exists. We can use an inverter The MM74C04 incorporates P an N channel MOS transistors due to the symmetry of them .



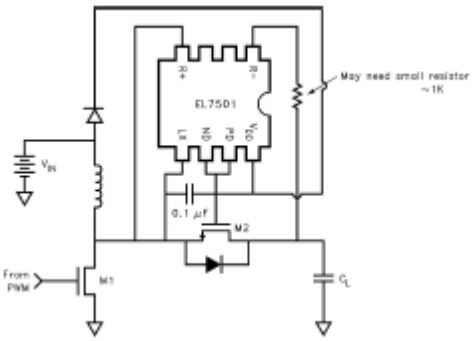
Video Sync Pulse Generator

[19] In the below circuit we can adjust the output resistors to tailor the fall and rise Circuit's times. a ground referenced TTL signal to be allowed to control a ground to Negative 8V output swing.



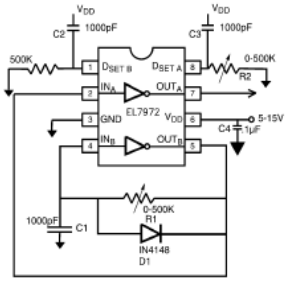
Boost Efficiency increased by Synchronous Switch

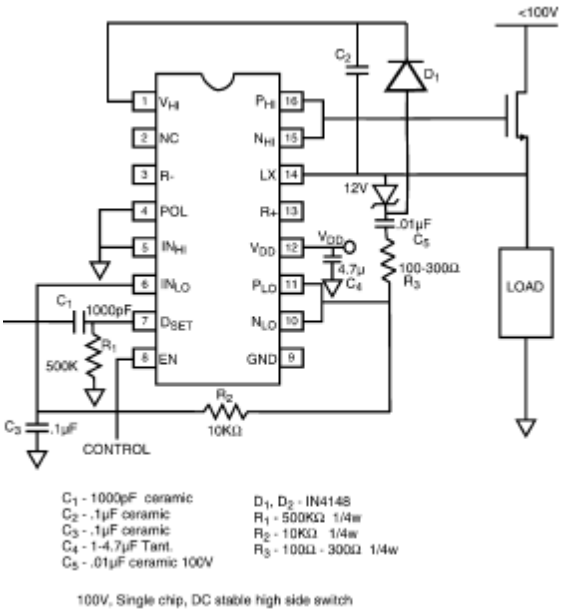
[20] the FET is turned on, When the R- pin is smaller than R+ pin The EL7501 plus a N-FET replaces the catch diode in a boost regulator A small resistor may be added in series with the R- pin to "tune" the turn on delay of this FET.



Pulse Generator

As shown in the below circuits





Self-Powered DC Stable

[21] The EL7972 is used to provide low side drive and the others will act as a charge pump oscillator.

X. CONCLUSION

[22] These papers reviewed and studied CMOS characteristics and Power consumption starting from semiconductors and types of transistors to minimize the consumption of the power in CMOS transistor circuits to use it in the different applications.

REFERENCES:

1. [Yano90] K. Yano et al., "A 3.8 ns CMOS 16 ´ 16 b Multiplier Using Complimentary Pass- Transistor Logic," IEEE Journal of Solid State Circuits, vol. SC-25, no 2,, April 1990.
2. [Chandrakasan95] A. Chandrakasan and R. Brodersen, Low Power Digital CMOS Design, Kluwer, 1995.
3. [Shoji88] M. Shoji, CMOS Digital Circuit Technology, Prentice Hall, 1988.
4. [Dopperpuhl92] D. Dopperpuhl et al., "A 200-MHz 64-b Dual-Issue CMOS Microprocessor," IEEE Journal of Solid State Circuits, vol. 27, Nov. 1992.
5. [Lee86] C. M. Lee and E. Szeto, "Zipper CMOS," IEEE Circuits and Systems Magazine, May 1986.
6. [Uyemura92] J. Uyemura, Circuit Design for CMOS VLSI, Kluwer, 1992.
7. [Heller84] L. Heller et al., "Cascade Voltage Switch Logic: A Differential CMOS Logic Family," Proc. IEEE ISSCC Conference, 1984.
8. [Weste93] N. Weste and K. Eshragian, Principles of CMOS VLSI Design: A Systems Perspective, Addison-Wesley, 1993.
9. [Chandrakasan94] A. Chandrakasan, Low Power Digital CMOS Design, Ph.D. thesis, University of California—Berkeley, Memorandum No. UCB/ERL M94/65, August 1994.
10. R. Chau, et al., in Extended Abstract of International Workshop on Gate Insulator, 2003.
11. [Veendrick84] H. Veendrick, "Short-Circuit Dissipation of Static CMOS Circuitry and Its Impact on the Design of Buffer Circuits," IEEE Journal of Solid State Circuits, vol. SC-19, no 4, August 1984.
12. [Hodges88] D. Hodges and H. Jackson, Analysis and Design of Digital Integrated Circuits,
13. [Elmasry91] M. Elmasry, Ed., Digital MOS Integrated Circuits II, IEEE Press, 1991.
14. [Krambeck82] R. Krambeck et al., "High-Speed Compact Circuits with CMOS," IEEE Journal of Solid State Circuits, vol. SC-17, no. 3, June 1982.
15. R. Chau, et al., in Proceedings of AVS 5th International Conference on Microelectronics and Interfaces, 2004.
16. Goncalvez83] N. Goncalvez and H. De Man, "NORA: A Racefree Dynamic CMOS Technique for Pipelined Logic Structures," IEEE Journal of Solid State Circuits, vol. SC 17 , June 1983.
17. [Liu93] D. Liu and C. Svensson, "Trading Speed for Low Power by Choice of Supply and Threshold Voltages," IEEE Journal of Solid State Circuits, vol. SC-28, no 1,January 1993.
18. [Friedman84] V. Friedman and S. Liu, "Dynamic Logic CMOS Circuits," IEEE Journal of Solid State Circuits, vol. SC-19, no.2, April 1984.
19. [Rabaey95] J. Rabaey and M. Pedram, Low Power Design Methodolgies, Kluwer, 1995.
20. [Chandrakasan92] A. Chandrakasan, S. Sheng, and R. Brodersen, "Low Power CMOS Digital Design," IEEE Journal of Solid State Circuits, vol. SC-27, April 1992.
21. [Annaratone86] M. Annaratone, Digital CMOS Circuit Design, Kluwer, 1986.
22. [Burd94] T. Burd, Low Power CMOS Library Design Methodology, M.S. thesis, University of

AUTHORS PROFILE

Ahmed H. Almutairi, Electronic Engineering BS West Virginia university Training Faculty Member at Telecommunication& Navigation Institute Head of Switching Dept Specialized in control system and coding teaching electronics and electrical subjects theoretically and practical using a educational program system Training courses: self development courses In field training courses Speciality training courses Skills Summary:

• Verified ATD Master Trainer
• Verified consulting skills
• Certified ICDL License
• Iso-9001 Lead Auditor
• Expert WorldSkills in Mobile Robot Skill
• Verified ABET Accreditation Academic Programs
• Design & develop Training Programs

Professional memberships:

• Member of training faculty at Public Authority of Applied Education and Training (PAAET)
• Member of volunteers Group "Environmental Organization"
• Member of Kuwaiti Press Society
• Member of Kuwait Engineers Society
• Member of the Training Association (Secretary of Board) (Public Relation & Media)
• Member of Kuwait Internal Auditors Association

Esam alsumait, High school graduates 1986 science Diploma of medical electronic in college of technology at PAAET Electronic Engineering Bs From the arab academy for science technology
Work at civil aviation for 11 years Training faculty member In higher institute of telecommunication and navigation Attend training courses in Training field Electronic field