

Performance Analysis of 1 bit HPSC Adder

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Abstract: In the technological evolution of integrated circuits, one of the important and considerable issues is the guesstimate of behavioural analysis of the simple circuits. The simplicity of the theory of logical effort is efficient in the evaluation of timing behaviour of the network with normal CMOS implementation. However this concept is inefficacious with the hybrid circuits as the circuit structure becomes intricate. At the same time, innumerable circuits with the hybrid arrangement which are good enough in various parameters when compared with standard CMOS have been proposed for various applications. Elite coordinated circuits frequently use adders to accomplish better speed to the detriment of intensity utilization or structure exertion. Hence it is particularly required to comprehend the working of full adders as they thus make an effect in the general gadget execution. The circuits developed by hybrid approach use perceptible logic styles to intensify the performance. Hence there is a great necessity to have an efficient timing behaviour method to determine the proper performance of hybrid adder circuits. This paper presents an efficient investigation that gives the designer a higher level of structure opportunity to focus on a wide scope of utilizations and foresee their exhibition. For the standard and exact selection and reducing of a hybrid adder cell two parameters are taken; one is gain and the other one is the selection factor. These can be quantifiable on the single test bench for the executives of vitality productivity. The predictive analysis is firmly established by implementing in Mentor Graphics for the chosen adder blocks

Keywords: hpsc, timing behavior, hybrid adder, gain

I. INTRODUCTION

With the rapid growth in electronics industry, it becomes a critical challenge to design devices with high performance. It all started when the transistor scaling is introduced and the researchers faced new challenges to overcome the problems of area, power and size.

Huge numbers of the circuits that get designed for specific purpose depend upon the well-organized usage of adder or multiplier blocks to carry out calculations. Whenever we consider arithmetic circuits one of the rudimentary operations is addition. In spite of the fact that integer addition usually has the smallest delay of all arithmetic functions, it has the biggest effect on the general PC execution. Full Adders can be considered as one of the main focussed parts of the specialists. To implement these cells, there were common as well as rare approaches followed. They are probably going to sustain the capacity to additionally lessen the expense per-work and improve the presentation of incorporated circuits. With the bringing down of limit voltage in ultra profound submicron innovation, bringing down the voltage that is responsible for internal power gives off an impression of being the most prominent intends to diminish power utilization. Be that as it may, the issue emerges if the supply voltage is diminished which is the ascent in delay. To make the constructed network reliable as a whole in terms of utilization of power, minimization of delay and prevent degeneration of supply voltage, a strongly intended design is required. Irrespective of different types of loads in the circuit which consumes power, providing good fan-out is the salient task for the designer. Old style structures of full adders typically utilize just a single rationale style for the entire design. One of the most relevant and basic example of such type of representations is the CMOS structure which follows static logic rather than dynamic logic. This type uses two different types of transistors connected together with the input terminals provided with same signal to execute the operations. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor. This structure format offers almost no static power dissipation which in turn allows integrating more gates, thereby resulting in much better performance. The principle drawback is the low speed of operation which for the most part comes because of high input capacitance. Additionally another significant negative mark is the presence of the PMOS block, as a result of its low mobility contrasted with the NMOS cells. In this way, the PMOS cells should be evaluated to accomplish the ideal execution. The other style of execution that comes into our psyche is dynamic logic as we have examined the characteristics of static style. It is recognized from the alleged static rationale by making use of transitory storage of data with the help of various capacitances. This format uses only NMOS transistors which get benefited with the speed as against static logic. The blocks implemented by this logic are normally quicker than static partners, and necessitate less area, yet are increasingly hard to structure. This representation can be more diligently to work with, however it might be the main decision when expanded handling speed is required.

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The careful examination gives us a clear idea predominantly that clocked logic increases the transistor count by considerable amounts that are switching at any given time, which in succession increases utilization of power over aforementioned logic. Because of these reasons, dynamic logic style isn't given preference. Conversely Pass Transistor Logic is the other way of constructing circuits where the advantage of reduction of transistors comes into picture. Apart from the advantage, there exists the main problem which is the reduction of signal strength after each stage. So for the purpose of eliminating the demerit, Differential Pass Transistor Logic comes into play which is commonly referred as Complementary PTL. It increases the number of transistors while focusing on degradation of signal. Hence it is also considered as inefficient in the design. The other type of implementation of full adder is the Transmission Gate Adder which is able to overcome the problem of Complementary PTL. It also uses less number of transistors than the previous models. Still the area of research in this field thrived the experts to go for another approach which is the hybrid logic approach. That seriously has a great impact to improve the efficiency of the overall circuit or the device because it combines logic styles at a time to implement a new model. The hybrid circuit represents a fine compromise between power and performance. The vast majority of these adders experienced the problem of bad fan-out and the efficient operation gets decreases if there is no involvement of buffers at the termination of each stage. The hybrid pass logic with static CMOS adder (HPSC) was presented here. Despite the fact that every single sort of design has its own benefits just as negative marks, this circuit makes a superior improvement than the others. The motivation behind this sort of approach is to improve the fundamental execution parameters in the circuit plan which makes the scientists of electronics parched without fail.

II. DESIGN CONFIGURATION

The implemented circuit is broken down into 3 small blocks and they are referred as M1, M2 & M3. M1, M2 are the cells that are responsible to generate one of the outputs called sum signal and M3 is solely for carry signal which comes in coordination with M1's output. The portrayal of both the signals can be seen in the figure displayed underneath. Every module is structured separately with the end goal that the whole adder circuit is enhanced regarding performance. In this whole actualized circuit structure xnor devours the more power utilization than others.

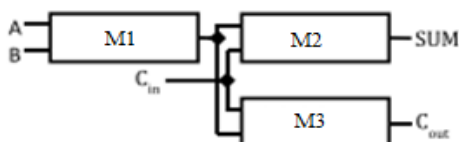


Fig 1. Full Adder in block representation

Thus, we structured a changed xnor module which expends less power than normal module and power gets decreased radically by utilization of two transistor cells. The altered block introduced in this paper offers low-power and rapid. By utilizing level re-establishing strategies we can get full swing of

yield signals. Here the detailed square uses four transistors having low output swing. But the recreated one uses six transistors which has better logic swing in comparison with four transistor block. In this circuit, the carry signal is implemented by using four transistors. Input carry signal reduces propagation path as it can propagate only through one transmission gate. The use of these transmission gates delays of the carry signal gets reduced significantly.

III. REVIEW OF DIFFERENT LOGIC STYLES

A few variations in CMOS structures have been utilized to design low power adder. In hybrid logic there are CMOS and PTL circuits. The CMOS full adder is the conventional style logic which is implemented by using two different networks. The output stage is formed by transistors that are connected in series which form a weak driver. Due to that reason and to provide required drivability to cascaded cells buffers are used.

IV. CONFIGURATION OF PROPOSED ADDER:

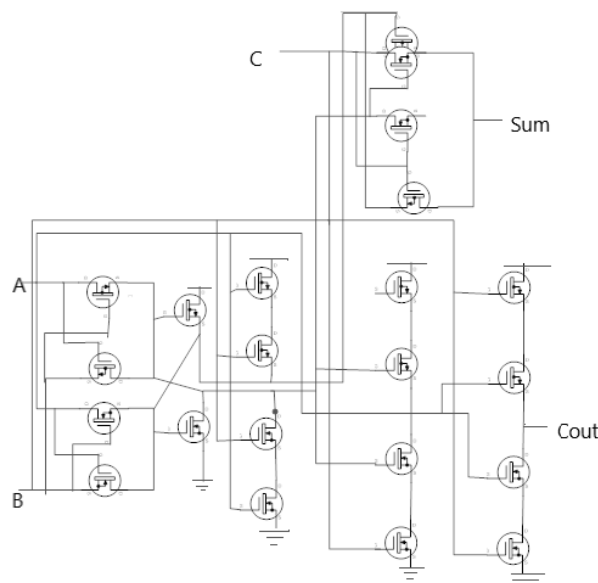


Fig 2: Implemented HPSC

Output sum operation is done by using xnor logic. Adder designed for optimum conditions may have errors and malfunction when operated at room temperature. In this methodology there is reduction in number of transistors and delay when compared to CMOS. All the previous done works are on static CMOS as their structure is fixed but for hybrid circuits we need new method for analyzing the complex behaviour. This irregular structure will make difficult layout and silicon area wastage would be more. In this paper we design hybrid circuit with reliable blocks and better goal parameters. Here we defined a method to reduce power-delay product by reducing transistor count. Here we consider power consumed and delay as critical factor for designing full adder. The presented adder circuit can be defined by different blocks.

$$Y = A \oplus B$$

$$Y' = \overline{A \oplus B}$$

$$Sum = Y \oplus C_{in}$$

$$C_{out} = A \cdot B + C_{in} \cdot Y$$

V. DESCRIPTION OF SIMULATION ENVIRONMENT AND SIMULATION RESULTS:

Mentor Graphics is an innovation chief in electronic plan computerization, giving programming and equipment structure arrangements that empower organizations to grow better electronic items quicker and more cost-successfully. The organization offers creative items and arrangements that assist engineers with beating the structure difficulties they face in the inexorably unpredictable universes of board and chip plan.

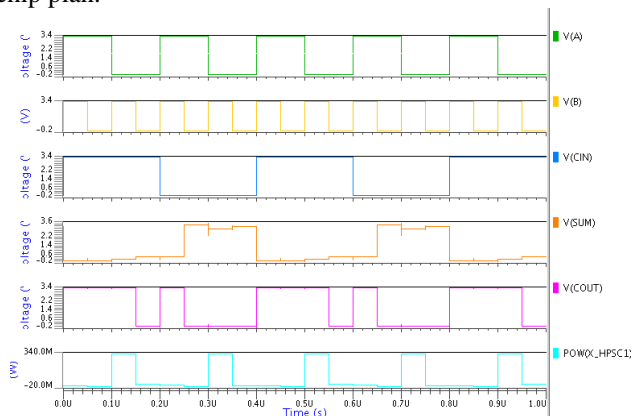


Fig 3: Power Waveforms of the proposed Adder

VI. CONCLUSIONS

Of the adder plans executed beforehand, the presented circuit here is believed to scatter insignificant power in the event that we watch the power analysis in the circuit and have littler region since it utilizes less number of transistor cells. In this manner the recently exhibited circuit performs well than the remaining. Before, adder blocks are regularly assessed in confinement without worry on how they are sent in the real circuit structure. In light of the operational conditions, a powerful circuit advancement calculation is prepared. Another structure was planned in mentor graphics and tried which gave an examination that it utilizes less power. It has better execution when contrasted with that of past actualized structures.

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