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Design of A High Performance 4-Bit Ternary Multiplier using CNTFET

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Abstract*: *In digital world, digital circuits are influenced by binary logic. Ternary logic which follows the multiple valued logic concept for designing the logic circuits which is an great alternate to the normal binary logic due to its less power consumption and chip area is reduces. Carbon Nano-tube Field-Effect Transistors (CNTFET) is selected to implement the ternary logic circuits due to its mechanical , electrical and thermal properties. The unique feature of CNTFETs has the potential of getting required threshold voltage by varying the diameter of carbon nano-tubes that makes them as a best appropriate type for implementing the ternary logic. In this paper a 4-Bit Ternary Multiplier is designed using 1-Bit ternary multiplier by CNTFET 32nm technology node and simulated in Hspice tool. The proposed 1-Bit multiplier has 10% less delay and 18% less power than the 1-Bit multiplier proposed by Srivasu et al.

Keywords* : *Cntfet, Mosfet, Ternary Logic.

I. INTRODUCTION

Conventionally, VLSI chips largely depends on silicon technology. The ITRS (International Technology Roadmap for Semiconductors) has foreseen scaling process is not possible in the nanometer region, and should be replaced by new similar devices. Many problems came across CMOS in nanometer region like short channel effects (SCEs), capability of gate controlling, and also power leakage is high. So the researchers are in research about to find best appropriate new devices like Single Electron Transistors (SET) [3], Quantum dot Cellular Automata (QCA)[2] and Carbon Nanotube Field-Effect Transistor (CNFET)[8]. A suitable alternative device for CMOS transistors is CNTFET. CMOS and CNTFET transistors are similar in terms of built-in electronic parameters, CNTFET will be the best appropriate technology without any major changes in CMOS. The CNTFETs is an 1D band structure which extinguish backscattering and close to ballistic operation. This is the reason for implementing the fast and low power circuits, using CNTFETs. In CNTFETs, there is two different types i.e.,

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P-FET (P-Channel FET) & N-FET (N-Channel FET) have the same mobility and which results , equal current flows through the both devices. Multiple-Valued Logic (MVL) could be preferred in Digital circuits. MVL logic means, unlike binary logic there will be third level which is an intermediate logic level is used to design the MVL circuits and systems. So CNTFETs is suitable to design the MVL circuits. Present almost all devices & circuits which accepts input in binary format are designed using binary logic (two valued logic) till now. The namely two-valued logic, where in binary logic each input/output line will have two states: 0 (logic low) which means 0v and 1(logic high) which means vdd. The response of digital systems are highly depends on however rapidly the signal states are going to be changed, where this change decides the device speed. Multiple valued logic (MVL) system allows more than two logic levels. According to the theory, MVL concept in circuit have the subsequent benefits[9] with the comparison of the binary logic.

(i) For MVL circuits, chip area is reduced because the number of interconnections are reduced to design the logical functions due to its capability of transmitting more information than binary wire.

(ii) Because of the capacitances of interconnects , MVL circuit gives the low power dissipation .

(iii) To overcome the significant pinout drawback raised while designing large chips, output signals within the circuit was permitted to suppose five or additional states instead of using only Binary two states in MVL circuits.

(iv) MVL has more than two logic levels. Ternary logic switches among 3 states namely 2, 1 and 0 voltage states or true, intermediate and false.

Multipliers plays a significant role in designing Arithmetic and Logic unit (ALU).The performance of Arithmetic and logical unit is decided based upon the time taking for multiplication process. Multiplication is a time consuming operation. In DSP, for convolution, Digital Filters, Fast Fourier transform (FFT),Arithmetic and Logic unit(ALU), microprocessors, and many other Digital circuit requires fast multiplier circuits. In our design a high performance multiplier is designed by using proposed fast adder circuits and outcomes are compared.

The remaining part of paper is organize as follows. Section II that discuss about the CNTFETs and its appropriate for ternary logic, Section III describes about ternary logic and 1-Bit Multiplier, Section IV presents the adder modules for fast calculating the partial products, Section V gives the design of ternary 4-Bit Multiplier. The reenactment results are tabulated in Section VI followed by conclusion in Section

II. CNTFET AND ITS APPROPRIATE TO TERNARY LOGIC

Carbon nano-tube (CNT) is an allotrope of carbon with round and hollow structure, which will be single-walled (SWCNT) or multi walled. A SWCNT is acquired, by moving the sheet up of graphite along a wrapping vector Ch = na+ mb, where n and m are sure whole numbers which indicate the chirality of the cylinder, and 'a'and 'b' are cross section unit vectors, as shown in Figure 1.

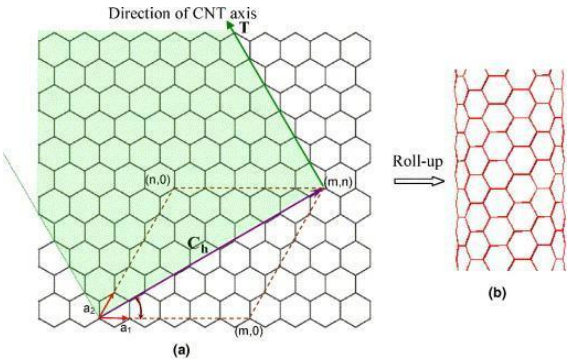

Fig.1 shows the nanotube is defined by the vector (a) Graphene lattice and (b) carbon nanotube.

Depending upon the value of n_1 and m, SWCNT can be either metallic or semiconducting. For m equal to n (m=n) CNT shows metal property and while n-m≠3i where i refers to an integer, CNT act as a semiconducting tube. Similarly, SWCNT is further classified into three groups according to the value of n and m are (1) armchair CNT when n = m = n, (2) zigzag CNT when n,m=0,0, and (3) chiral CNT when m and n are different and nonzero. All armchair CNTs behave as conductors. On the other hand, zigzag and chiral CNTs show conductor behavior when the distinction in the middle of the indices i.e., n-m is an integer multiple of 3 if not they displays a semiconducting properties, these CNTs are used in CNTFET. CNTFET is a type of FET that makes use of a one or an mutliple of semiconducting SWCNTs as a channel formed between the metal electrodes one is acting as a source and the other is drain contacts.

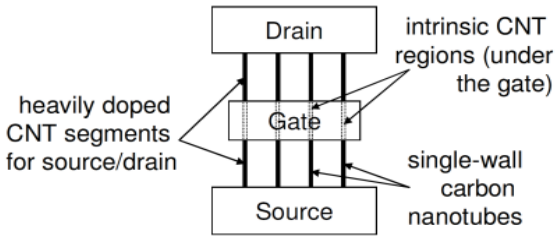

Fig.2 shows the CNTFET top view

CNTFET device is turned ON and OFF through the gate electrode placed around CNT channel. The top view structure of CNTFET is displayed in above Figure 2. Undoped part of carbon nanotubes works as a way for travelling carriers from one side to another side under the influence of gate electrode, while intensely doped carbon nano-tubes part placed between the source,drain electrodes and gate gives the low electrical resistance in the conduction-state of CNTFET. Since the electrons are restricted to travel through the narrow CNTs. With the comparison of bulk MOSFET, carrier mobility increasing remarkably on account of ballistic transport operation in CNTs. These are three distinct types of CNTFETs:MOSFET like CNTFET, band-to-band tunneling CNTFET(BTBT-CNTFET) and Schottky barrier CNTFET (SB-CNTFET). The V-I qualities of MOSFET type CNTFET is same as that of the conventional Si based MOSFETs. The CNTFET structure like MOSFET is utilized in presented work which is shown in Fig.3. The parameters of CNTFET device is shown in table-I. From Stanford CNFET model [5], the device model is taken. Using this model [6][7], the N-channel and P-channel circuit are designed and simulated in Synopsys Hspice tool which used later to implement the different ternary gates.

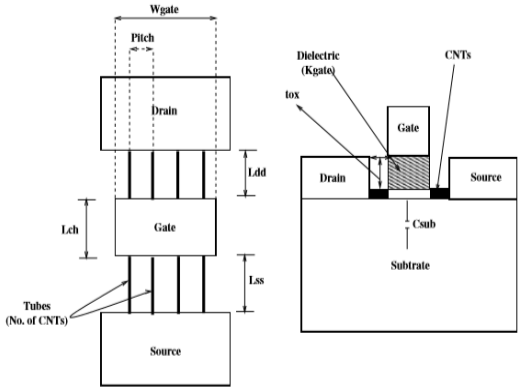

Fig.3 shows the CNTFET structure like MOSFET.

Table-1

CNTFET DIFFERENT PARAMETERS

Symbol	Parameters	Values
L_{geff}	MFP in the intrinsic CNT chanel region due to non-ideal elastic scattering	200nm
L_{ch}	Physical channel length	32nm
L_{ss} / L_{dd}	Source / Drain extension length	32nm
C_{sub}	Coupling capacitance between the channel region and substrate	20pF
(n,m)	Chirality of tube	(19,0)
pitch	Distance between two adjacent CNTs	20nm
T_{ox}	Thickness of dielectric material	4nm
C_{sub}	Coupling capacitance between the channel region and substrate	20pF
W_{gate}	Width of metal gate	6.4nm

The model is reenactmented by changing distinct device parameters and the drain characteristics is acquired. The drain characterstics of n-channel CNFET plot is shown in Fig.4.

In conventional,MOS devices, sizing of MOSFET is done by changing the gate width while in MOSFET-like CNFET by varying the number of cylindrical tubes.

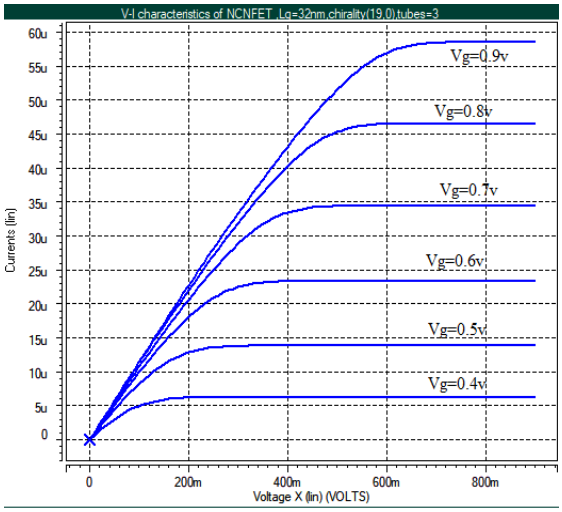

Fig.4 shows the V-I characteristics of n-channel CNFET.

The diameter of CNT is calculated by using equation.1

$$D_{CNT} = \frac{\sqrt{3}\, a_0\left(\sqrt{n^2 + m^2 + nm}\right)}{\pi} \quad \ldots(1)$$

The inter atomic seperation between each atom is given by a_0 = 0.142 nm and

(n,m)= chiral vector.

The threshold voltage can be varied with the help of diameter of the CNT, which can be calculated using equation.2

$$V_{th} = \frac{\sqrt{3}\, a\, V_{\pi}}{3\, D_{CNT}} \quad \ldots(2)$$

The carbon to carbon atom distance is given by a=2.49 Å ,

The carbon $\prod$-$\prod$ bond energy in the tight bonding model is given by $V_{\prod}$ =3.033 eV.

D_{CNT}, which gives the diameter of the Carbon nano-tube (CNT).

III. TERNARY LOGIC & TERNARY 1-BIT MULTIPLIER

In multiple valued logic concept (MVL), Ternary logic is one of the most important type. Ternary logic is three valued state which represents themselves as 0,1 and 2. The voltage leves of ternary logic levels is 0V,V_{dd}/2 and V_{dd}. The basic gates in the digital system is ternary inverter which is also categorize into three types i.e, Negative Ternary Inverter (NTI), Simple Ternary Inverter (STI) and Positive Ternary Inverter (PTI). The Ternary NOR, Ternary NAND ,Ternary AND ,Ternary OR are the different Ternary logic gates[4]. From all the logic gates Ternary AND and OR gates is known to be as minimum and maximum gates. Lets takes an eaxmple, if X_1 and X_2 are the two inputs of the Ternary OR gate then the output will be the maximum of two inputs. Similarly the Ternary AND gate output is minimum of two inputs. The symbol of Ternary inverter gates are shown below figure 5.And different logic gates are also shown in fig 6.

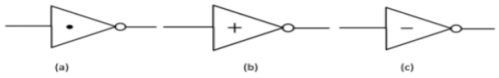

Fig.5 shows the different types of Ternary inverter (a)STI (b)PTI and (c)NTI.

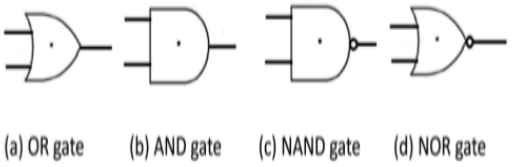

Fig.6 shows the different gates used in Ternary logic.

Ternary 1-Bit multiplier which accepts the two ternary inputs namely multiplicand and multiplier and generates two outputs namely ternary product and ternary carry. For Binary multiplication, Binary AND gate is used to generate the partial products where as ternary multiplier requires some additional circuit for generating the ternary product and ternary carry. The ternary multiplier is designed using two multiplexers in [1]. Instead of using multiplexers, we use gate level representation for achieving high speed. The Ternary 1-Bit multiplier behaviour for different possible combinations is shown in table II.

Table-II

1-Bit Multiplier Truth table

Input A	Input B	Product	Carry
0	0	0	0
0	1	0	0
0	2	0	0
1	1	1	0
1	2	2	0
2	2	1	1

The k-map for product and carry is shown in figure 7.

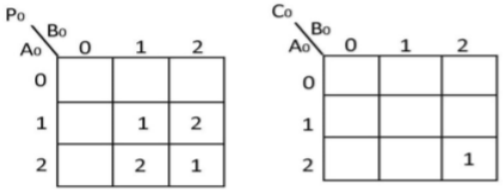

Fig.7 shows the k-map for P_0 and C_0.

The Equations for Ternary product (P_0) and Carry (C_0) is given by 3 and 4 .

$$P_0 = (A_1.B_2 + A_2.B_1) + 1.(A_2.B_2 + A_1.B_1) \ldots (3)$$

$$C_0 = 1.(B_2.A_2) \qquad \ldots (4)$$

The gate level representation of 1-Bit Ternary multiplier is displayed below figure 8.

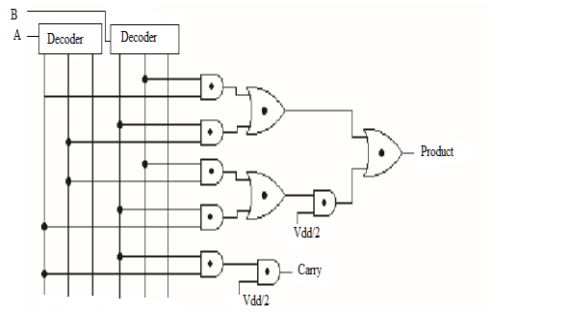

Fig.8 shows the gate level representation of Ternary 1-Bit Multiplier .

The output waveform of 1-Bit Ternary multiplier is shown in figure 9.

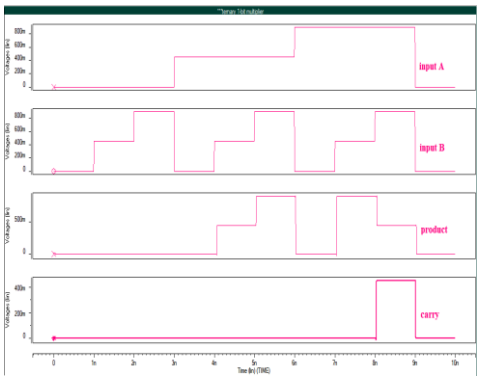

Fig.9 shows the Input & Output waveforms of Ternary 1-Bit Multiplier .

IV. PROPOSED TERNARY ADDERS

To design a 4-Bit Ternary Multiplier,1-bit multipliers ,halfadders and fulladders are used. A novel Ternary Modified halfadder (TMHA) is used which accepts two inputs i.e, one input is in ternary form (0,1 and 2) and another one is in binary form (0,1)and generates the sum and carry which is similar to halfadder. The truth table of TMHA is given in table III. The gate level representation is shown in fig 10.

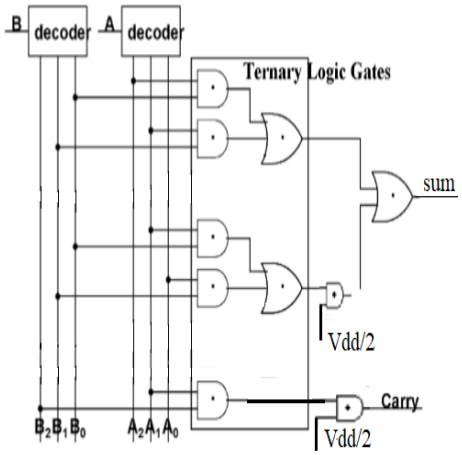

Fig.10 shows the gate level representation of Ternary Modified Half adder .

Table-III

Ternary Modified Half Adder Truth table

Input A	Input B	Carry	Sum
0	0	0	0
0	1	0	1
0	2	0	2
1	0	0	1
1	1	0	2
1	2	1	0

The output of TMHA is shown in fig 11. By using this ternary modified halfadder , the delay,area and power is also gets reduced.

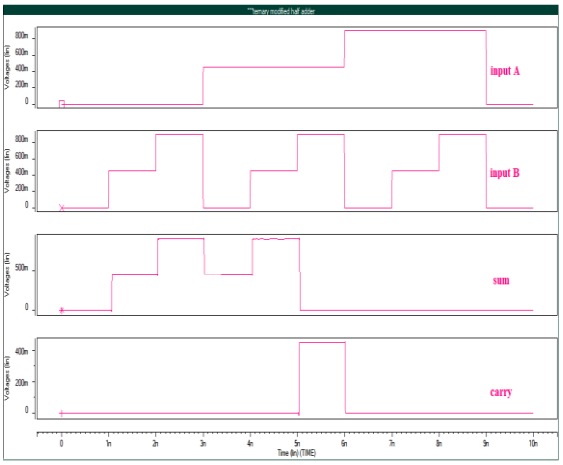

Fig.11 shows the input and output waveforms of Ternary Modified Half adder .

The Ternary Fulladder (TFA) is also designed using three halfadders and which gives the best delay and power with repect to normal Ternary fulladder . The truth table of TMHA is given in table IV. The architecture of ternary fulladder is shown in fig 12. The output of TFA is shown in fig 13.

Table-IV

Ternary Full Adder Truth table

A	B	Sum	Carry	Sum	Carry	Sum	Carry
		C_{in}=1		C_{in}=2		C_{in}=0	
0	0	1	0	0	0	2	0
0	1	2	0	1	0	0	1
0	2	0	1	2	0	1	1
1	0	2	0	1	0	0	1
1	1	0	1	2	1	1	1
1	2	1	1	0	0	2	1
2	0	0	1	2	0	1	1
2	1	1	1	0	0	2	1
2	2	2	1	1	1	0	2

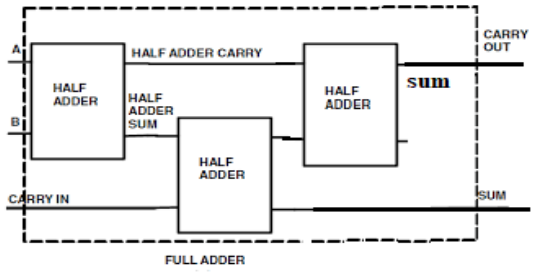

Fig.12 shows the architecture of Ternary Full adder .

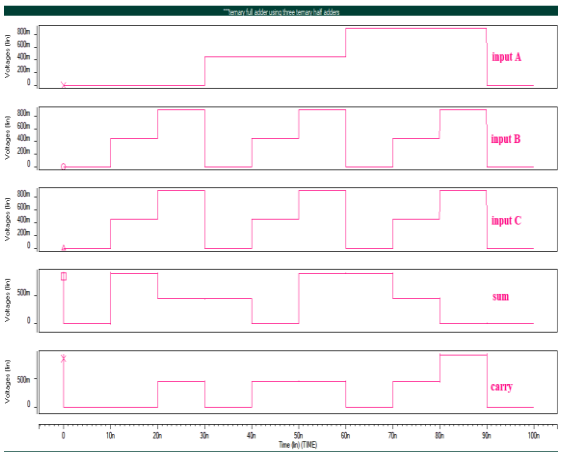

Fig.13 shows the Ternary Full adder output .

VI. PROPOSED TERNARY 4-BIT MULTIPLIER

The 4-Bit Ternary multiplier uses 16 number of ternary 1-bit multipliers ,8 number of modified half adders ,4 number of halfadders and 17 number of fulladders. The architecture of 4-Bit Ternary Multiplier is shown in fig 14.

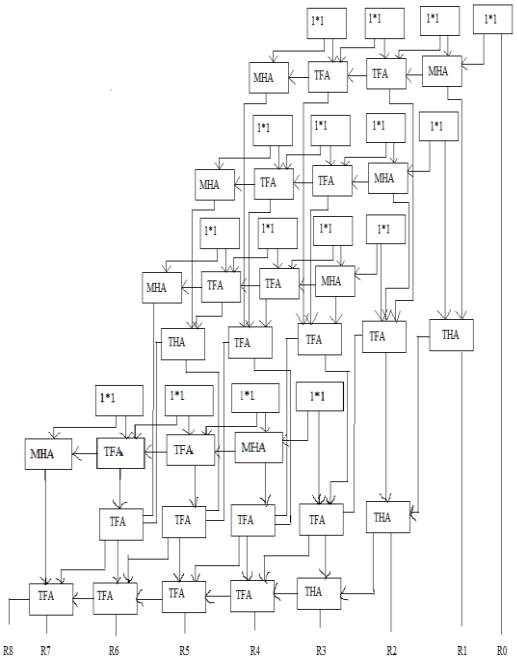

Fig.14 shows the architecture of 4-Bit Ternary multiplier.

V. SIMULATION RESULTS & DISCUSSIONS

The 4-Bit Ternary Multiplier uses a novel type fulladder using halfadder, and also a modified half adder. This will gives the best delay and also power consumption is less.

Circuit type	**Delay(pS)**	**Power (uW)**
Proposed Ternary Modified Half Adder	18.22	0.96
Ternary FullAdder[4]	23.02	8.752
Proposed Ternary Full Adder	21.52	8.34
Ternary 1-Bit Multiplier[1]	20.02	60.25
Proposed Ternary Multiplier	19.72	52.49
Proposed Ternary 4-Bit Multiplier	180.58	225.86

VII. CONCLUSION

This paper outlined the novel design of Ternary 4-Bit multiplier circuit using Carbon Nano-tube Field Effect Transistor(CNTFET). This is the future technology which leading now binary logic. For designing a large complex circuit binary logic requires more hardware so it leads increase in chip size and also high power dissipation in CMOS technology. Lesser power dissipation and less delay is achieved in the CNTFET based ternary logic circuits. The threshold voltage is depends upon the diameter of the nanotube, so the controlling of threshold voltage will be easy for designing MVL circuits rather than CMOS technology.

By the above results we can conclude that , CNTFET based Ternary circuits is the best shows potential in MVL circuits in future.

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