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Design and Implementation of PERES based 128 bit Parallel Adder using FPGA

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Abstract*: In this work, the parallel adder is designed using the PERES reversible logic gate with the resolution of 128 bits. The reversible logic gates have a unique property of one to one mapping between the input and output vectors. The simulation design is verified using the NI lab view tool for the resolution of 24 bits. For higher resolution designs, the HDL code is developed by making use of the Xilinx Spartan FPGA device. The HDL has several advantages like parallel processing, design compatibility, cost effective, reconfigurable, versatile language and design hierarchy. The performance of the proposed method is validated by comparing the area and power consumption with two FPGA devices.

***Keywords* : Adders, Reversible Logic Gates, NI Labview, Field Programmable Logic Gates**

I. INTRODUCTION

In most of our designs we use the basic logic gates for the design of many real time applications. The use of Reversible Logic Gates (RLG) in complex digital design reduces the complexity of the design. The RLG based division circuit exhibits improvisation in the performance characteristics compared to the conventional circuit [1]. The reversible computing gives advantages like high performance and improved energy efficiency [2]. The computation of RLG based design minimizes the power [3]. The power dissipation of the RLG based digital design reduces with the technology scaling [4]. The use of RLG in digital designs proves to be more cost-effective than the superior gates with respect to gate cost and quantum cost [5]. The testability of digital design developed using the RLG can be obtained at low operating cost [6]. The RLG based sequential circuit uses the online testable design so as to detect the single line faults [7].

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The reduction in the garbage outputs can be achieved using the developed VHDL code for the RLG based digital design [8]. The RLG is used in applications like quantum computing, cryptography, DNA and optical computing, signal processing and automata [9].

The logic gates which takes n inputs and gives 'n' outputs. It works in both forward and backward directions. There are several types of reversible logic gates, namely PERES, FEYNMAN, TOFFOLI, and FREDKIN. The descriptions of the RLGs are as given below

A. PERES Gate

PERES is a 3*3 input and output reversible logic gate which takes A,B,C has inputs and give P, Q, R has outputs respectively.

P=A
Q=A⊕B
R=AB⊕C

B. FEYNMAN Gate

FEYNMAN is a 2*2input and an output, reversible logic gate which takes A, B, has inputs and give P,Q, has outputs respectively.

P=A
Q=A⊕B

C. TOFFOLI Gate

TOFFOLI is a 3*3 input output reversible logic gate which takes A,B,C has inputs and give P, Q, R has outputs respectively.

P=A
Q=B
R=AB⊕C

D. FREDKIN Gate

FREDKIN is a 3*3 input And output reversible logic gate which takes A,B,C has inputs and give P, Q, R has outputs respectively.

P=A
Q=A'B⊕AC
R=A'C⊕AB

In this work, the PERES RLG is utilized for the design of 4 bit parallel adder and BCD adder for the purpose of the validation in the NI LabView Tool. The high resolution design of 128 bit Parallel adder is verified for the parametric evaluation of power and area using the Xilinx Spartan 3 A DSP FPGA.

II. DESIGN OF 128 BIT PERES BASED PARALLEL ADDER CIRCUIT

The proposed 128 bit adder involves the PERES reversible logic gate for its manipulation. The 128 bit adder utilizes two inputs "A" and "B" with 128 bit lengths and output sum as 129 bits. The carry is assigned as 127 bits with the Input carry as "Cin". Conventionally, the parallel adder design is built using logic gates, which consumes more power and area. In order to reduce the power and area, the PERES RLG is utilized within the generation of the Sum and Carry.

The design of full adder circuit using the PERES RLG consists of using two PERES RLGs connected in sequence. The PERES based Full adder uses the inputs of A,B and logic "0" as inputs for the first PERES gates to yield the outputs as A, A⊕B and AB respectively, and the AB is obtained because of the logic "0" input to the first PERES gate.

The three inputs of the Second PERES gate are given as A (B, C and AB, which gives the output as A⊕B, A⊕B⊕C and (A⊕B)C+AB respectively. The unused outputs are assigned as G1= A and G2=A⊕B for the designer's reference. The Boolean expressions for the PERES based Full Adder are as given below

$$G1=A \quad (1)$$

$$G2=A\oplus B \quad (2)$$

$$S=A\oplus B\oplus C \quad (3)$$

$$Ca_1=(A\oplus B)\ C\oplus AB \quad (4)$$

The carry equation of (4) is logically equivalent to the carry Ca2=AB+BC+CA and requires 4 logic gates consisting of two Exclusive OR and two AND gates whereas the Ca2 requires 5 logic gates consisting of two OR and three AND gates. With the development of PERES based Full adder circuit, the design of PERES based parallel adder with the resolution of 128 bits sums to 512 logic gates, which is comparatively high to conventional parallel adder with 640 logic gates leading to the decrease in the power consumption and area for the proposed 128 PERES method.

III. RESULTS AND DISCUSSION

The proposed 4 bit PERES based parallel adder is developed using the NI Labview for the verification in simulation. The developed NI based PERES RLG is shown in the Fig 1 which exhibits the connection of inputs A, B and C with Exclusive OR and AND gates to produce the output of P, Q and R and it verified using the truth table as given.

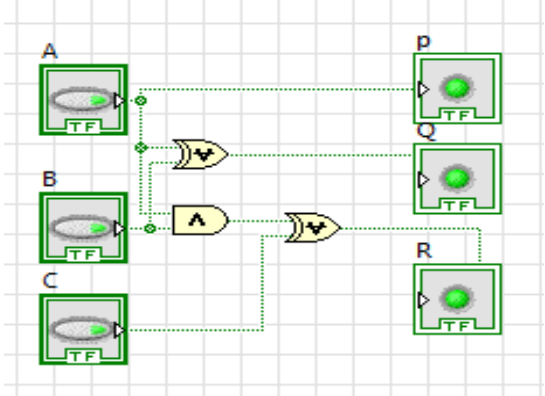


Fig. 1. PERES Reversible Logic gate design in NI LabView

The above PERES design is used to create the SubVI so as to develop the PERES based Full Adder. The front panel connection for 3 inputs, namely A, B and C are connected as given by the Boolean expressions. The four outputs G1, G2, S and C in the front panel are utilized to validate the developed circuit in the NI labview environment. Fig. 2 shows the PERES Sub VI based Full adder implementation in which the Logic "0" input is given using FALSE assignment "F".

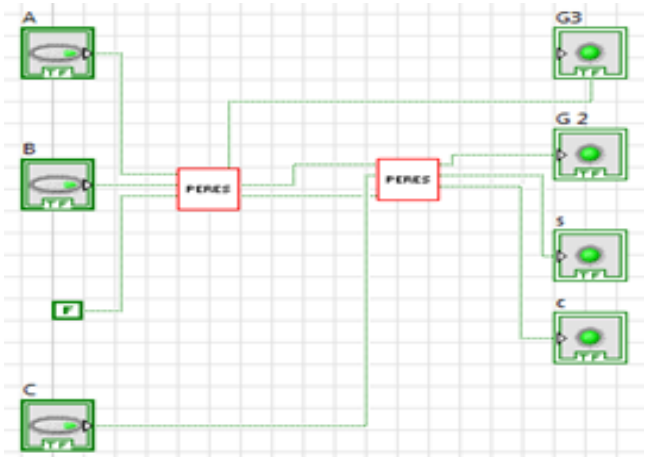


Fig. 2. Realization of Full adder using PERES gate in NI LabView

Further the PERES based Full adder circuit is used in the design of two parallel adder circuits. 1) PERES based Four bit parallel adder and 2) PERES based BCD adder. The four bit parallel adder and the BCD adder uses 4 PERES based full adders as shown in Fig. 3(a) & 4(a). The simulation output of the 4 bit parallel adder and BCD adder is presented in Fig. 3(b) and 4(b) respectively.

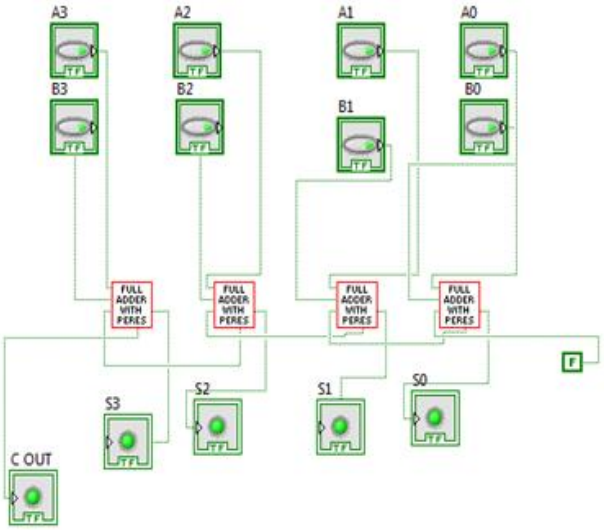


Fig. 3(a). PERES based Implementation of 4 bit parallel adder using the NI LabView

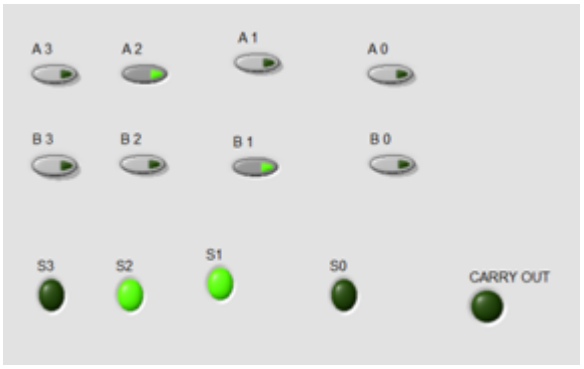


Fig 3(b) depicts the output of Sum "0110" and Carry "0" for the inputs of "0100" and "0010"

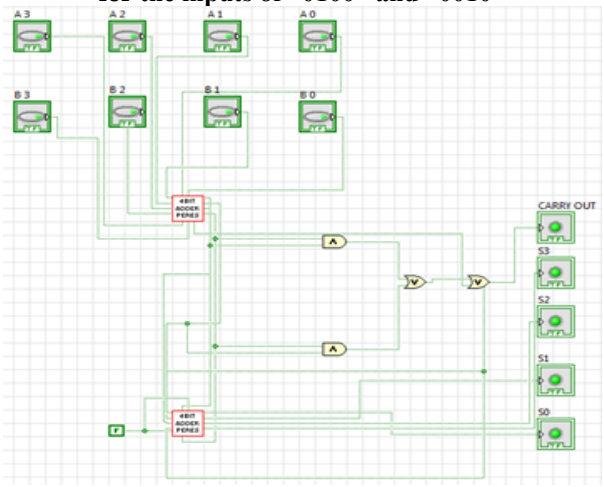


Fig. 4(a). PERES based Implementation of BCD adder using the NI LabView tool

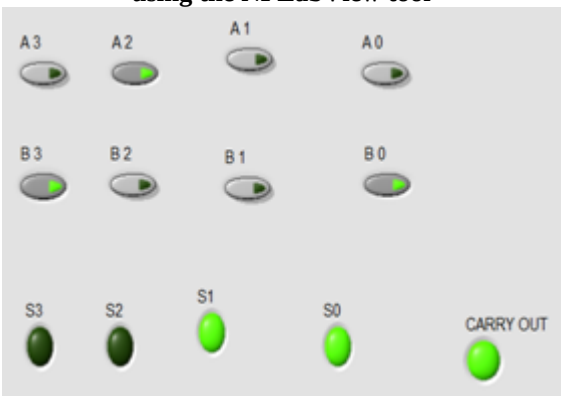


Fig. 4(b). depicts the BCD output of "10011" for the inputs of "0100" and "1001"

The hardware implementation of the PERES based parallel adder is extended to the FPGA device. The resolution of 2^7 bits of the proposed design is developed using the structural model of the VHDL code. The simulation results of the 2^7 bit parallel PERES adder are shown in Fig. 5. The Xilinx Spartan family devices, namely 3A and 6 are utilized for the feasibility of the proposed method in realtime. In comparison, the device utilization chart of the proposed method benefits the Spartan 6b Low Power device as it consumes less area in Table 1 and low power as depicted in Tables 2. The RTL schematic of the proposed method is shown in the Fig. 6. The floorplan and its routing are depicted in Fig.7 and 8 for the proposed 128 bit parallel adder method.

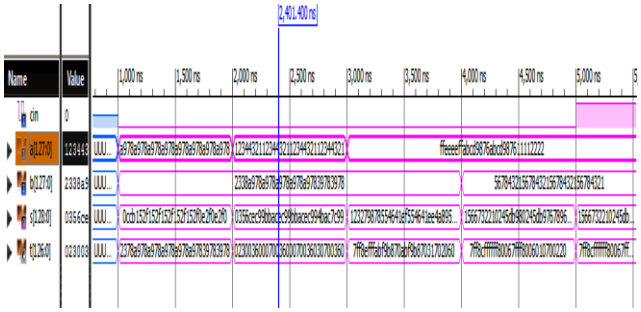
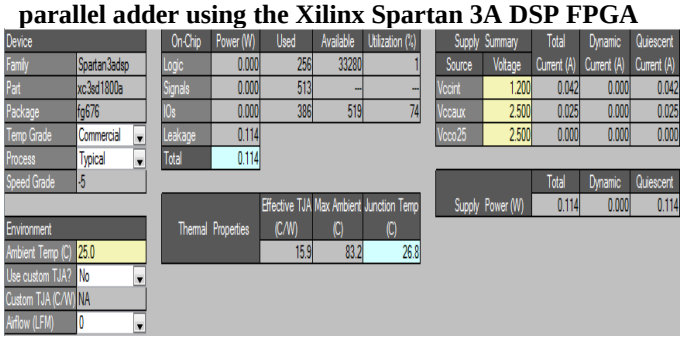


Fig.5: Simulation output of the 128 bit parallel adder using the Xilinx ISE tool

Table. I: Device Utilization chart for the 128 bits using Spartan FPGA family

Logic Utilization	Spartan 3A DSP XC3SD1800A	Spartan 6 XC6SLX100T
Number of 4 input LUTs	256 out of 33280	128 out of 63288
Number of occupied Slices	192 out of 16640	76 out of 15822
Total Number of 4 input LUTs	256 out of 33280	--
Number of bonded IOBs	386 out of 519	386 out of 498
Average Fanout of Non-Clock Nets	1.75	1.43

Table2 Power consumption of the proposed 128 bit parallel adder using the Xilinx Spartan 3A DSP FPGA



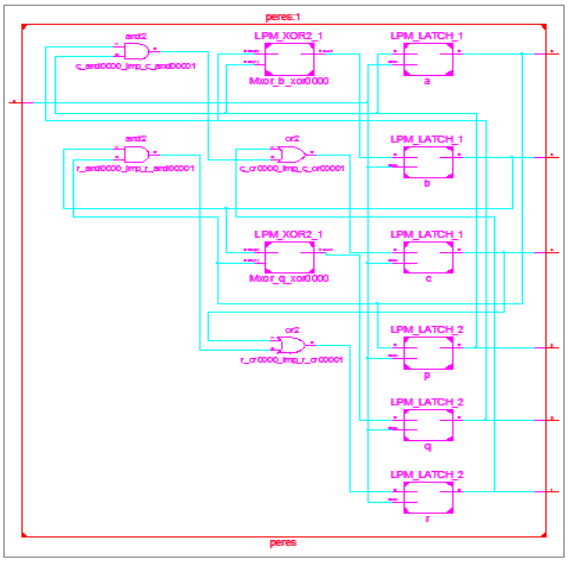


Fig. 6. RTL view of the proposed method using the Xilinx ISE Tool

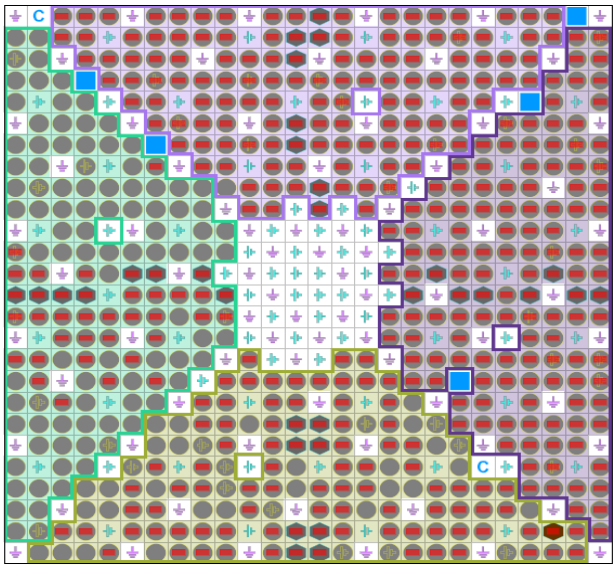


Fig. 7. Floorplan of the proposed parallel adder using the Xilinx Plan Ahead tool

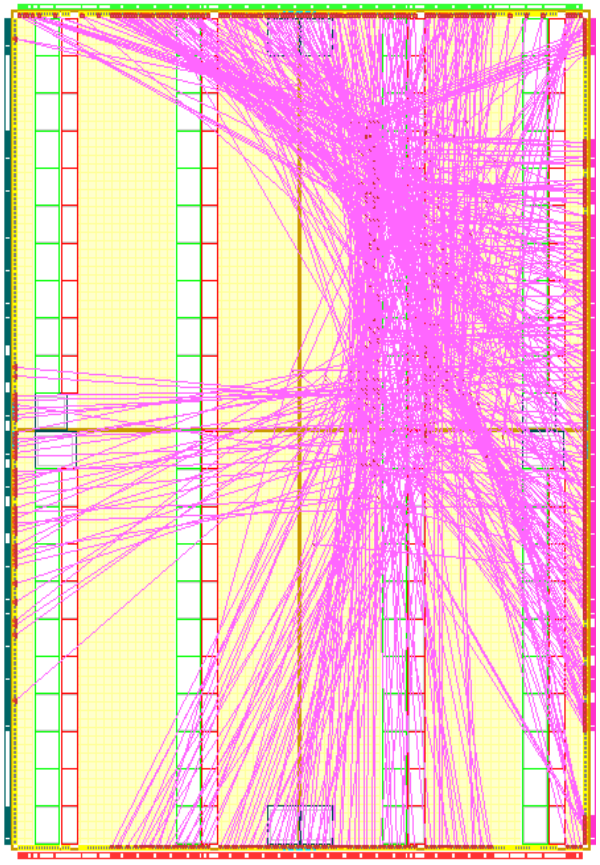


Fig. 8: Routing of the proposed 128 bit parallel adder using the Xilinx Plan Ahead Tool

IV. CONCLUSION

The design of PERES based parallel adder is designed using the NI labview in simulation. The performance of the developed simulation model is satisfactory. The high resolution design of the PERES based parallel adder is implemented using the Xilinx Spartan FPGA device seems to be feasible. The future trend of this work would be towards the utilization of the reversible logic gates in the design of complex multipliers and division algorithms.

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Joseph Anthony Prathap was born in 1981 in Puducherry. He has obtained B.E [Electronics and Communication] and M. Tech [VLSI Design] degrees in 2003 and 2007 respectively, and the Ph.D. in FPGA based Power Converters in 2017 from Annamalai University. He has put in 15 years of service in teaching and research. He is currently Associate Professor in the Department of Electronics and Communication Engineering at Vardhaman College of Engineering, Shamshabad, Telangana, India. His research interest includes VLSI design, development of digital switch patterns, FPGA control techniques for power converters, photovoltaic power electronics converters.

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