International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-2, December 2019

# Effect Of Body Biasing On 0.13 Um CMOS Transistor

**Noorfazila Kamal, Nadhira Mohamad Fauzi**

***Abstract*: Complementary metal-oxide semiconductor (CMOS) consist of n-type metal-oxide semiconductor field effect transistor (NMOS) and p-type MOSFET (PMOS). In common practice, only three terminals of these transistors are used, namely gate, source and drain. Meanwhile, the fourth terminal, which is body terminal is tied to source. Changing body terminal bias causes the transistor to have a body effect. In this work, optimum body biasing for 0.13 µm NMOS and PMOS are identified. Effect of body biasing to the MOSFETs are investigated. In addition, how body biases affect CMOS circuits are also observed. Three type of body biasing are considered, namely Forward Body Biasing (FBB), Reverse Body Biasing (RBB), and Dynamic Threshold MOS (DTMOS). Drain current, $I_d$ versus gate voltage, $V_G$ and drain current, $I_d$ versus drain-source voltage, $V_{DS}$ for FBB, RBB and DTMOS are simulated to determine the optimum operating point for each biasing technique. To observe the effect of body biasing techniques on the circuits, inverter and common source amplifier are constructed using FBB, RBB and DTMOS. In addition, the circuits also constructed in zero body biasing (ZBB) for comparison. The results show that, optimum body biasing is at 0.6 V for all three body biasing techniques. FBB and DTMOS cause the threshold voltage, $V_{th}$ to decrease but increase the leakage current. On the other hand, RBB causes increase in threshold voltage, $V_{th}$ yet reduces the leakage current of the CMOS. The results obtained in this work will enable other circuit designers to determine the optimum FBB, RBB and DTMOS operating point.***

***Keywords*: Body biasing, dynamic body biasing, forward body biasing, reverse body biasing, threshold voltage.***

## I. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) technology has been one of the most popular technologies in the computer chip design industry and is now widely used in many applications for integrated circuits [1-3]. This technology makes use of both NMOS and PMOS transistor devices. The transistors consist of four terminals, namely gate, drain, source and body. In practice, the body terminal (also known as bulk terminal) of the MOSFET is simply assumed to be tied down to the source terminal, which give a zero voltage drop between source and body terminals, $V_{SB} = 0$.

**Revised Manuscript Received on December 30, 2019.**
***** Correspondence Author
**Noorfazila Kamal***, Department of Electrical, Electronic and Systems Engineering, Faculty of Engineering and Built Environment, Universiti Kebangsaan Malaysia, Selangor, Malaysia.
**Nadhira Mohamad Fauzi**, Department of Electrical, Electronic and Systems Engineering, Faculty of Engineering and Built Environment, Universiti Kebangsaan Malaysia, Selangor, Malaysia.



If the body terminal is biased, source-body voltage, $V_{SB}$ is no longer zero, causing body effect. Body effect changes the threshold voltage of the transistor.

There are three body biasing techniques, namely Forward Body Biasing (FBB), Reverse Body Biasing (RBB) and Dynamic Body Biasing (DBB). DBB is also known as Dynamic Threshold MOS (DTMOS). Several studies have been carried out to adopt techniques of body biasing in circuits such as low noise amplifier (LNA) [4], wireless sensor network (WSN) [5], power amplifier (PA) [6], floating current source (FCS) circuit [7], voltage differencing buffered amplifier (VDBA) [8], ultrahigh frequency (UHF) micropower rectifiers [9] and static frequency divider [10]. FBB helps to achieve low power consumption [4-5]. Meanwhile, RBB helps to improve linearity and power added efficiency (PAE) of the PA [6]. Besides, DTMOS allows the circuit to operate at ultra-low voltage and ultra-low power consumption [8-10].Each body biasing technique requires different dc biasing and has different effects on the circuit. A proper body biasing is needed to ensure that the circuit functions properly. The aim of this work is to determine the optimum operating point for NMOS and PMOS transistor when body biasing is applied to the transistor. In addition, the effect of each body biasing technique to circuits are observed.

## II. BODY EFFECT

In MOSFET structure, P-N junction between substrate and doped region (source/drain terminals) forms intrinsic body diodes (also known as parasitic diode). Fig. 1 shows the intrinsic body diodes in an NMOS. In MOSFET operation, these body diodes must be in reverse bias. Normally, the body terminal is assumed to be connected to the source terminal resulting in no biasing for the body diode between source and body terminals. Nevertheless, the difference in voltage between source and body terminals in body biasing technique causes the body diode to influence the MOSFET. Therefore, a proper biasing of the body is necessary to ensure that MOSFET operates in an appropriate region.

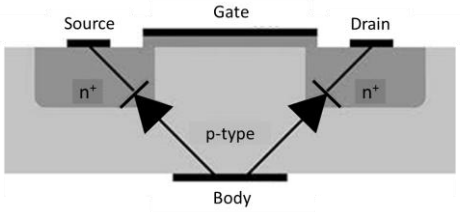


**Fig. 1. Intrinsic body diodes in NMOS structure**

A non-zero voltage drop between source and body terminals, $V_{SB}$ cause the MOSFET to have a body effect. The body effect describes the threshold voltage, $V_{th}$ changes due to the change in the voltage of the source-bulk, $V_{SB}$. The effect can be expressed by the following equation, where Eq. 1 and 2 represents threshold voltage for NMOS and PMOS, respectively.

$$V_{th\_N} = V_{th0} + \gamma\left(\sqrt{2\phi_N + V_{SB}} - \sqrt{2\phi_N}\right) \quad (1)$$

$$V_{th\_P} = V_{th0} + \gamma\left(\sqrt{2\phi_P + V_{BS}} - \sqrt{2\phi_P}\right) \quad (2)$$

where $V_{th0}$ is the threshold voltage when $V_{SB} = 0$, $\gamma$ is body threshold parameter, $\phi_N$ & $\phi_P$ are surface potentials for NMOS PMOS, respectively and $V_{SB}$ & $V_{BS}$ voltage drop across source and body terminals for NMOS and PMOS, respectively. For a low supply voltage, surface potentials, $\phi_N$ (or $\phi_P$ for PMOS) can be neglected when compared to $V_{SB}$ (or $V_{BS}$ for PMOS) [11]. As depicted in Eq. 1 and 2, the positive $V_{SB}$ value increases the NMOS $V_{th}$ but reduces the PMOS $V_{th}$ value. On the other hand, the negative $V_{SB}$ value decreases the NMOS $V_{th}$ but increases the value of PMOS $V_{th}$.

## III. BODY BIASING TECHNIQUES

Three body biasing techniques are available, namely Forward Body Biasing (FBB), Reverse Body Biasing (RBB), and Dynamic Body Biasing or also known as Dynamic Threshold Voltage (DTMOS). FBB can be obtained if the body voltage, $V_B$ is greater than the source voltage, $V_S$ for NMOS or $V_B$ is lower than $V_S$ for PMOS. On the other hand, $V_B$ must be smaller than $V_S$ for NMOS or $V_B$ greater than $V_S$ for PMOS to obtain RBB. For DTMOS, the gate terminal needs to be connected to the body terminal. Fig. 2 shows the symbol of FBB, RBB and DTMOS.

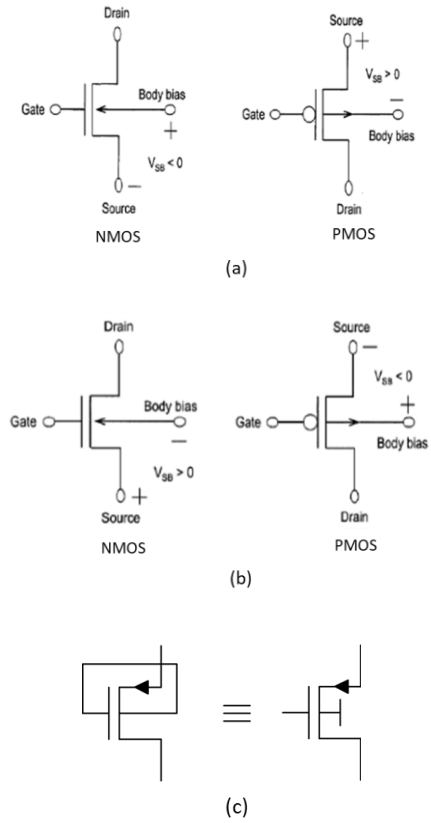


Fig. 2. Symbol for MOSFET with (a) Forward Body Biasing (FBB), (b) Reverse Body Biasing (RBB) and (c) Dynamic Body Biasing (Dynamic Threshold Voltage, DTMOS).

## IV. OPERATING POINT

In this work, circuits are constructed and simulated in 0.13 µm CMOS technology using Mentor Graphic. Fig. 3 shows the FBB and RBB operating point simulations for NMOS and PMOS. For DTMOS operating point simulation, body terminal is connected to gate terminal as shown in Fig. 4. In addition, zero body biasing was also simulated for benchmarking purposes. For the zero biasing, the body terminal is connected to the source terminal for both PMOS and NMOS.

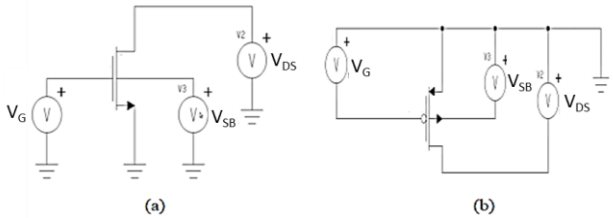


**Fig. 3. The FBB and RBB operating point simulation for (a) NMOS and (b) PMOS**

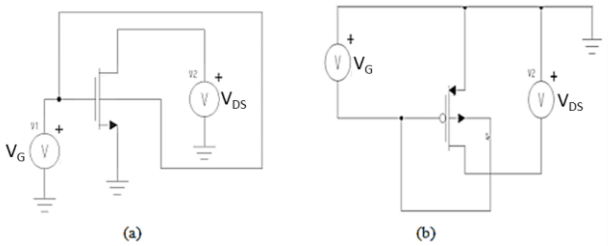


**Fig. 4. The DTMOS operating point simulation for (a) NMOS and (b) PMOS**

In these simulations, DC sweep analysis were used. The $V_{DS}$ was swept from 0 to 1.2 V, with 0.1 V step, and drain current, $I_D$ were observed. For FBB and RBB, the $V_{SB}$ was swept according to biasing technique. The $V_{DS}$ sweeping is to determine the optimum supply voltage, meanwhile $V_{SB}$ sweeping is to determine the optimum body voltage. The $V_{SB}$ sweeping voltage for FBB and RBB is shown in Table 1. The gate voltage, $V_G$ was biased so that the transistor remains on. Therefore, for NMOS, $V_G$ was set to the supply voltage, meanwhile for PMOS, $V_G$ was connected to ground.

**Table- I: $V_{SB}$ sweeping voltage for FBB and RBB**

| Transistor | Biasing technique | $V_{SB}$ (V) |
|---|---|---|
| NMOS | FBB | 0 to 1.2 V |
| | RBB | 0 to -1.2 V |
| PMOS | FBB | 0 to 1.2 V |
| | RBB | 0 to -1.2 V |

For DTMOS, the body voltage was connected to the gate voltage, $V_G$. The $V_G$ in Fig. 4 is swept from 0 to 1.2V with 0.1 V step.

### A. Effect on circuit

Inverter and common source amplifier circuits as shown in Fig. 5 and 6, respectively,

were constructed using FBB, RBB and DTMOS. In addition, for benchmarking purposes, circuit with zero body biasing (ZBB) was also constructed and simulated.

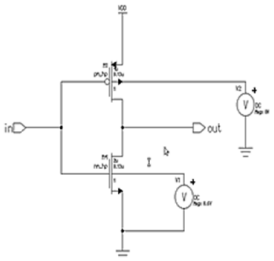


**Fig. 5. Inverter**

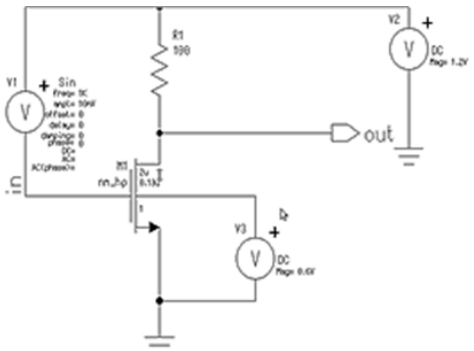


**Fig.6. Common source amplifier**

Supply voltage of 1.2 V was used for inverter and amplifier circuits with ZBB, FBB, and RBB. On the other hand, the supply voltage of 0.6 V was used for DTMOS. The selected body voltage for FBB and DTMOS was 0.6 V. It was -0.6V for RBB. The voltages were selected based on the optimum point of operation obtained in simulations. For each body biasing technique, power dissipations were observed. For the common source amplifier circuit, the gate terminal was given an input signal with an input frequency of 1 kHz and amplitude of 10 mV. In this work, to investigate the effects of dynamic biasing on the circuit, DTMOS was applied to both NMOS and PMOS. In reality, however, dynamic body biasing for NMOS cannot be implemented in bulk CMOS technology [12]. This is because in a single chip, p-type NMOS substrates (body terminal) are shared together. Due to the connection of the body terminal to the gate terminal, which is the input terminal, the voltage always changes according to the input signal. Different NMOS carries different input signal that gives multiple voltage to the shared body terminals.

## V. RESULT AND DISCUSSION

Results of simulation show that for each biasing technique there was an optimal body biasing point resulting in the highest drain current, $I_D$ when the transistor is on, and lowest leakage current when the transistor is off. Fig. 7 shows the $I_D$ versus $V_{SB}$ for NMOS and PMOS with FBB at 1.2 V supply voltage. As shown in the graph, before the start to current falls, the peak $I_D$ occurs at $V_{SB}$ = 0.7 V. Nevertheless, $V_{SB}$ cannot be set at 0.7 as p-n junction in the parasitic diode (body diode) becomes forward biased at this point. It causes the drain current decreases when $V_{SB}$ reaches 0.7 V. MOSFET operations requires the parasitic diode to be in reverse biased. Thus 0.6 V was selected for the voltage of the body. PMOS also gives the same pattern where the optimum voltage of the body is 0.6 V.For RBB, the chosen body voltage for NMOS and PMOS is -0.6V. Since this project is to compare the three biasing techniques, DTMOS has selected the same body voltage value that is 0.6 V.

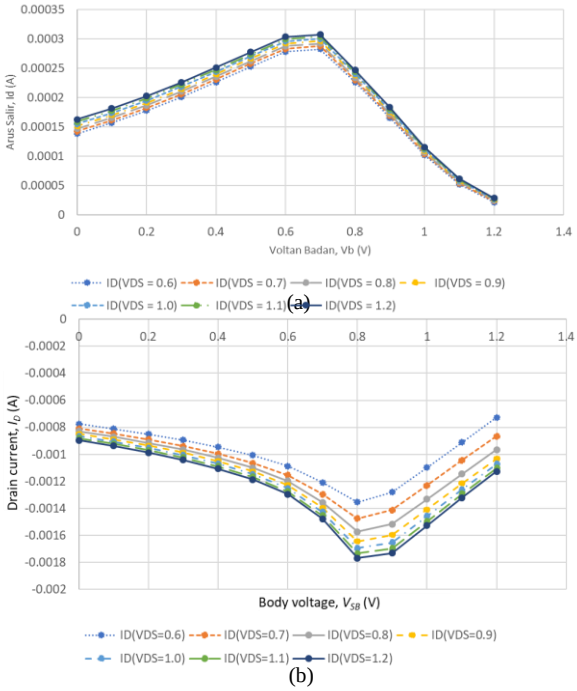


**Fig. 7. Drain current, $I_D$ vs $V_{SB}$ for FBB of (a) NMOS and (b) PMOS**

Fig. 8 shows the drain current, $I_D$ versus gate-source voltage, $V_{GS}$ for all body biasing techniques of NMOS and PMOS. The threshold voltage differences for ZBB, FBB, RBB and DTMOS can be seen from this graph. In comparison to ZBB, FBB offers a lower $V_{th}$, while RBB gives a higher $V_{th}$. DTMOS also gives a lower $V_{th}$, but a little higher than FBB. Due to the connection of the gate terminal to body terminals in DTMOS, the $I_D$ is almost saturated after $V_{GS}$ crosses 0.7 V for NMOS and 0.8 V for PMOS.

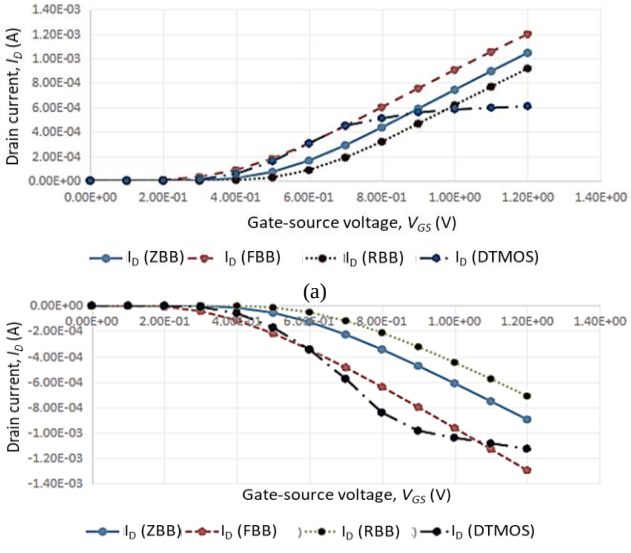


**Fig. 8. Drain current, $I_D$ vs gate-source voltage $V_{GS}$ for FBB (a) NMOS and (b) PMOS**

Fig. 9 shows $I_D$ versus drain-source voltage $V_{DS}$ for ZBB, FBB, RBB and DTMOS of NMOS and PMOS. The highest drain current is provided by FBB followed by ZBB, RBB and DTMOS. DTMOS supposed to produce high $I_D$ [13]. However, as this work sets $V_{SB}$ = 0.6 V for all biasing techniques for comparison purposes, $V_G$ for DTMOS also sets to 0.6 V automatically. That gives the low current of the drain in DTMOS.

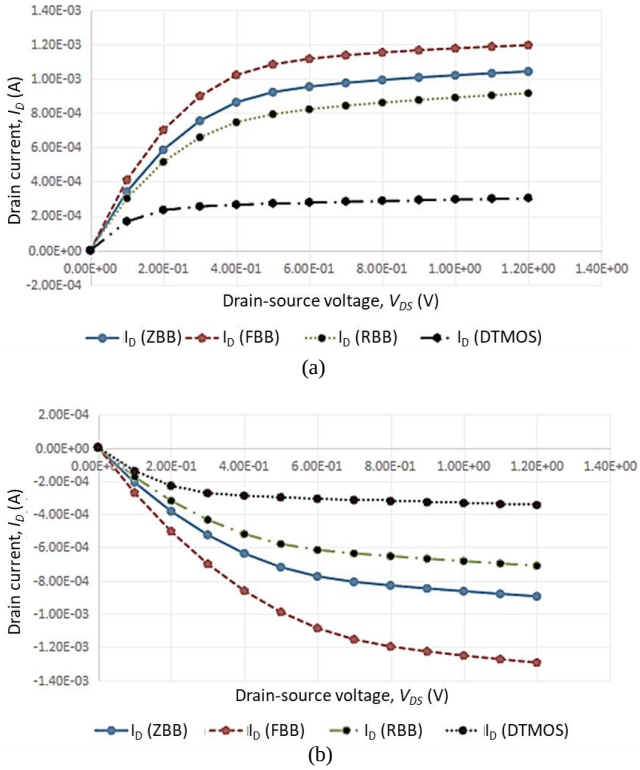


**Fig. 9. Drain current, $I_D$ vs drain-source voltage $V_{DS}$ for (a) NMOS and (b) PMOS**

Table-II and III show leakage current and power consumption of each body biasing technique for NMOS and PMOS, respectively. As depicted in the Table, FBB shows the highest leakage current and power consumption for NMOS and PMOS. Meanwhile, RBB gives the lowest leakage current and power consumption. RBB causes the depletion region in p-n junction of body diode to become wider resulting in the parasitic diode being reverse biased. Therefore, very minimum electron can travel through the p-n junction resulting in very low leakage current for RBB. In contrast, for FBB, the depletion region of p-n junction in the body diode decrease due to the $V_B$. Therefore, only minimal electron can travel through the p-n junction, resulting in very low RBB leakage current.

**Table- II: Leakage current and power consumption of ZBB, FBB, RBB and DTMOS for NMOS**

| | ZBB | FBB | RBB | DTMOS |
|---|---|---|---|---|
| Leakage current | 0.7 nA | 59.0 nA | 0.07 nA | 0.7 nA |
| Power consumption | 0.8 nW | 1100 nW | 0.08 nW | 0.8 nW |

**Table- III: Leakage current and power consumption of ZBB, FBB, RBB and DTMOS for PMOS**

| | ZBB | FBB | RBB | DTMOS |
|---|---|---|---|---|
| Leakage current | 0.9 mA | 1.3 mA | 0.7 mA | 1.1 mA |
| Power consumption | 1.1 mW | 1.6 mW | 0.9 mW | 393.3 mW |

As for the effect of body biasing techniques on circuits, drain current, leakage current and power consumption for inverter and common source amplifier were compared between different body biasing techniques. Two supply voltages, namely 1.2 V and 0.6 V have been used. Table IV and V show current and power consumptions for inverter and common source amplifier.

**Table- IV: Drain current, leakage current and power consumption in inverter for ZBB, FBB, RBB and DTMOS**

| Supply voltage | | ZBB | FBB | RBB | DTMOS |
|---|---|---|---|---|---|
| 1.2 V | Drain current | 0.76 nA | 6.53 µA | 0.13 nA | - |
| | Leakage current | 0.47 nA | -327.5 µA | 0.02 nA | - |
| | Power consumption | 0.56 nW | 393.0 µW | 0.24 nW | - |
| 0.6 V | Drain current | 0.41 nA | 6.42 µA | 0.03 nA | 6.38 µA |
| | Leakage current | 0.36 nA | 3.39 µA | 0.07 nA | 0.36 nA |
| | Power consumption | 0.21 nW | 3.02 µW | 0.08 nW | 0.21 nW |

**Table- V: Drain current, leakage current and power consumption in common source amplifier for ZBB, FBB, RBB and DTMOS**

| Supply voltage | | ZBB | FBB | RBB | DTMOS |
|---|---|---|---|---|---|
| 1.2 V | Drain current | 0.06 mA | 0.15 mA | 1.97 µA | - |
| | Leakage current | 0.7 nA | 58.8 nA | 0.07 nA | - |
| | Power consumption | 0.84 nW | 1.06 µW | 0.08 nW | - |
| 0.6 V | Drain current | 13.8 µA | 70.8 µA | 1.9 µA | 44.1 µA |
| | Leakage current | 0.41 nA | 43.0 nA | 0.02 nA | 0.41 nA |
| | Power consumption | 0.24 nW | 1.02 µW | 0.02 nW | 0.24 nW |

As shown in Table IV and V, there were no DTMOS parameters for 1.2 V supply voltage circuits. This is because the design of DTMOS is not suitable for supply voltages of more than 0.6 V [14]. If the supply voltage exceeds 0.6 V, the p-n junction of body diode becomes forward bias and allows current flows through substrate. As can be observed, RBB provides the smallest drain current, leakage current and power consumption for both inverter and common source amplifier circuits.

## VI. CONCLUSION

In this study, three body biasing techniques are investigated, namely Forward Body Biasing (FBB), Reverse Body Biasing (RBB), and Dynamic Body Biasing or Dynamic Threshold Voltage (DTMOS).

Drain current, $I_d$ versus gate voltage, $V_G$ and drain current, $I_d$ versus drain-source voltage, $V_{DS}$ for FBB, RBB and DTMOS were simulated to determine the optimum operating point for each biasing technique. To observe the effect of body biasing techniques on the circuits, inverter and common source amplifier were constructed using ZBB, FBB, RBB and DTMOS. Current and power consumption for each circuit was observed and compared. The results proposed that optimum operating point for FBB and DTMOS is at $V_B$ = 0.6 V, while RBB is at $V_B$ =-0.6. At its optimum operating level, the supply voltage for FBB and RBB is 1.2 V, while the optimum supply voltage for DTMOS is 0.6 V. In fact, due to the forward biased parasitic diode, DTMOS cannot be operated at supply voltage greater than 0.6 V. The results also show that the threshold voltage was reduced by FBB and DTMOS but high leakage current was generated. On the other hand, RBB increases the threshold voltage but produces the lowest leakage current. For the effect of each body biasing technique on inverter and common source amplifier, RBB shows the lowest power consumption for both circuits due to the low leakage current.

## ACKNOWLEDGMENT

This study was financially supported by Geran Universiti Penyelidikan (GUP-2017-084) Universiti Kebangsaan Malaysia. The authors would like to thank Prof Dr. Mamun Ibne Reaz for his support in this project.

## REFERENCES

1. Mohammadi, H., A., H., & Dee, C. F. “A review on modeling the channel potential in multi-gate MOSFETs”, in Sains Malaysiana, 2014, 43(6), pp. 861-866.
2. Afifah M., A. H., Menon, P. S., Ahmad, I., & Shaari, S. “Optimisation of process parameters for lower leakage current in 22 nm n-type MOSFET device using Taguchi method”, in Jurnal Teknologi, 2014, 68(4), pp. 45-49.
3. Romli, N. B., Mamun, M., Bhuiyan, M. A. S., & Husain, H. “Design of a low power dissipation and low input voltage range level shifter in CEDEC 0.18-µm CMOS process” in World Applied Sciences Journal, 2012, 19(8), pp. 1140-1148.
4. Syed M. &Vikram S. “A 2-10 GHz Ultra-Wideband Common-Gate Low Noise Amplifier using Body Bias Technique”, in 2017 Devices for Integrated Circuit (DevIC), 2017, pp. 541-545.
5. Yin C.J., Murad S.A.Z., Harun A., Ramli M.M., Zulkifli T.Z.A. & Karim J. “A Low Power 2 . 4 GHz CMOS Mixer Using Forward Body Bias Technique for Wireless Sensor Network” in IOP Conference Series: Materials Science and Engineering, 2018,318(1), p.012032.
6. Kuo, J. L. & Wang, H. “A 24 GHz CMOS power amplifier using reversed body bias technique to improve linearity and power added efficiency”, in IEEE MTT-S International Microwave Symposium Digest, 2012, pp. 11–13.
7. Ugranli, H. G., Yildirim, M., & Kacar, F. “Design of low power DTMOS based FCS and its notch filter application for ECG signals”, in International Journal of Computational and Experimental Science and Engineering, 2017, 3(1), pp. 29-32.
8. Basak, M. E., & Kacar, F. “Ultra-low voltage VDBA design by using PMOS DTMOS transistors”, in Istanbul University-Journal of Electrical & Electronics Engineering, 2017, 17(2), pp. 3463-3469.
9. Teh, Y. K., Mohd-Yasin, F., Choong, F., Reaz, M. I., & Kordesch, A. V. “Design and analysis of UHF micropower CMOS DTMOST rectifiers”, in IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56(2), pp. 122-126.
10. Hou, T. C., Kamal, N., Jaafar, K., Reaz, M. I., & Sampe, J. “Design of a low power static frequency divider”, in 2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES), 2016, pp. 199-202.
11. Moradi, F., Cao, T. V., Wisland, D. T., Aunet, S., & Mahmoodi, H. “Optimal body biasing for maximizing circuit performance in 65nm CMOS technology”, in 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS), 2011, pp. 1-4.
12. Niranjan, V., Singh, A., & Kumar, A. “Dynamic threshold MOS transistor for low voltage analog circuits”, in International Journal of Scientific Research Engineering & Technology (IJSRET), 2014, 1, pp. 26-31
13. Niranjan, V., & Gupta, M. “Body Biasing-A circuit level approach to reduce leakage in Low power CMOS circuits”, in Journal of Active and Passive Electronic Devices, 2001, 6(1-2), pp. 89-99.
14. Uygur, A., & Kuntman, H. “DTMOS-based 0.4 V ultra low-voltage low-power VDTA design and its application to EEG data processing”, in Radioengineering, 2013, 22(2), pp. 458-466.

## AUTHORS PROFILE

**Noorfazila Kamal** was born in Perak, Malaysia in 1979. From 1997 to 2000, she was educated at Universiti Teknologi Malaysia (UTM), in Johor Bharu, Malaysia, where she obtained a Bachelor’s Degree in Computer Engineering with honours. In October 2002, she joined The Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia as a tutor. In 2013, she obtained her PhD in Electronic Engineering from The University of Adelaide. Currently, she is a senior lecturer at the Centre for Integrated Systems Engineering and Advanced Technologies (INTEGRA), and Program of Electrical and Electronic Engineering, Faculty of Engineering and Built Environment (FEBE), Universiti Kebangsaan Malaysia (UKM) and is currently an associate fellow of Centre for Engineering and Built Environment Education Research, FEBE, UKM. Her research interests include analog/mixed signal IC design, very large scale integration (VLSI) and engineering education. Noorfazila is the Editor of Jurnal Kejuruteraan. She had published more than forty journals and conference proceedings in both electronic engineering and engineering education fields.

**Nadhira Mohamad Fauzi** was born in Negeri Sembilan, Malaysia in1996. From 2015 to 2019 she was educated at University Kebangsaan Malaysia (UKM), in Bangi, Selangor where she obtained her Bachelor’s Degree in Electrical and Electronic Engineering with honours. In August 2018 she has completed her internship as a trainee test engineer at ON Semiconductor Sdn. Bhd. in Seremban, Negeri Sembilan. Currently, she is a junior service technician at Switch The Mines, Apple Service Centre under CG Computer Sdn. Bhd. Her research interests include MOSFET, CMOS, optimum point of PMOS and NMOS, technique of body biasing and effect of body biasing.