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Testing and Diagnosis of Delay Faults in Finfet VLSI Circuits using Non-Incremental Genetic Algorithm

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Abstract: ***FinFet transistors are used in major semiconductor organizations which play a significant role in the development of the silicon industries. Due to few embedded memories and other circuit issues the transistors have specific faults in manufacturing, designing of the circuit etc. This paper presents an advanced test algorithm to diagnose those faults. The circuit with different gates is designed to identify the places having faults. In addition, algorithms such as non-incremental algorithms is used to find critical path, path delay and PDF of Critical path delay and Genetic Algorithm for optimisation of Critical path delay for sensitive test vector and no of iterations. The transfer characteristics curve is plotted along with the delay curve which helps in finding out the simulation parameters such as noise margin, propagation delay. The results in the methodology calculate the probability density function of the critical path by estimating mean, standard deviation and variance. The advantages of the integration of the two algorithms in this paper help in analyzing the specific faults in the circuits and the error correction of the broken link in the path analysis and has enhanced performance. Furthermore, more complicated circuits are analyzed for fault detection with different approach. In this paper the research work on testing, diagnosis, estimation of Critical path and PDF of Critical path delay faults for FinFET based Combinational Circuits for 20nm and 32 nm Technologies are presented for the first time using latest Non Incremental Genetic algorithm.***

Keywords: FinFet transistors, Fault analysis, Transfer characteristics, Critical Path Delay, Non-Incremental Genetic Algorithm.

I. INTRODUCTION

The MOS transistor models are highly complex as the dimensions of devices are decreasing day by day. The model Parameters which is required for the circuit simulations needs to be extracted successfully. Alternate use of MOSFETs is the circuits involving the FinFet which is being investigated. The gate control over the channel is better when compared to MOSFETs[1].FinFETs are defined as the circuits with the shape of fins and is perpendicular to the structure of wafer which carries current. The existing fin is sandwiched in-between the front as well as back gate. In order to suppress short channel effect, the structure of FinFETs is very thin[2]. Fins are compact and sophisticated such that its size is less than the channel length. The traditional use of the planar bulk equipment of sub 25 nm with short channel behaviour, reduced leakage current and excellent fabrication process is replaced by the double gate FinFET transistors which are considered as the worst alternative. By adopting simple manufacturing process and having good compatibility with planar MOSFET, FinFET is considered as one of the most feasible multi-gate devices[3].

Numerous switching operations are performed with the 94% of the chip area. This makes the circuit to be operated in high speed and reduced power. The conventional MOSFET is used for the scaling of power which is an issue due to short channel effect[4]. As diagnosing of the fault is critical, an advanced testing model is developed for FinFET circuits. This research focuses on developing an innovative testing model and fault diagnosis method for FinFet circuits.

There are numerous types of fault models available for FinFETs[5]. There are few problems associated with the design of FinFet circuits in various applications. At various levels of abstraction, fault modelling for the planar single gate CMOS is researched extensively[6]. Considering an example of bridging, stuck-open faults and stuck at delay faults are the widely utilized fault models for CMOS. Fault modelling is defined as the method which helps in developing physical defects models which is performed at high abstraction levels. Stuck at fault model is used to detect the 80% of the faults. Testing and bridging of delay faults becomes critical by scaling of the technology. In presence of defects the behaviour of FinFET INV and NAND gates examined[7].

The statistical timing analysis is performed to analyze and predict the efficacy of the delay test in the circuits. This research develops an innovative method to identify fault in FinFET circuits. The information is derived from the data present through learning algorithms and helps in predicting new observations. These algorithms are divided such that it requires two complete passes through the input data and also iterative access to the data to complete the estimations the existing learning algorithms are referred as incremental learning algorithms which completes the computations necessary to fit the models by processing in a given time. Additional computations are required for the final result. The processing of all the tasks in each iteration is performed by the non-incremental algorithms.

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Statistical Data Miner includes a large selection of non-incremental and incremental learning algorithms; the major aim of the research is to develop an advanced test algorithm for testing and diagnosing faults in FinFet circuits. as given in proposed methodology **(Ref: Flowchart-1)**The study aims at effective testing and diagnosing of faults carried out in FinFet circuits. For this we are designing NAND, NOR & NOT gates using FinFet Library (PTM library) in LTSPICE and estimating the FinFet characteristics of NAND, NOR & NOT gates. The Next step is creating a net list for circuit diagram & importing in MATLAB. Further, Fault analysis & diagnosis using Non-incremental Genetic algorithm, Calculating Critical path delay of Mean, Variance & standard deviation values & plotting the Probability density function (Pdf) graph for Critical path delay is performed.

II. RELATED WORK &LITERATURE SURVEY

1. The specific faults in FinFet circuits with a new strategy are presented[8]. Further the fault modelling is performed and besides that, test algorithm which is novel is proposed for synthesis. The validation is performed on the other FinFET based embedded technologies. Faults specific to the FinFETS are identified. FinFET based embedded technologies is used for the validation of the proposed method. FinFETS based new faults are identified. The solution which was proposed is applied to the different types of real FinFET and the new faults are identified. The comparison is made between the FINFET based memories using the planar based memories and it is concluded that these are prone to dynamic faults and is stable towards other kinds of faults. In the future work the summarization and classification of the FinFet specific faults is done and more efficient test algorithms are developed.

2. The work is based on the FAST fault model and is proposed on behalf of the insignificant delay faults by the cross-gate defects in FinFET[9]. The test patterns are generated and selected with the help of FAST ATPG, test selection and fault simulation. The comparison is made between the FAST SDQL and FAST coverage and the pattern sets which are obtained are 29% and 4% respectively.

3. The problems associated with the fault diagnosis are overcome by an improved partial least square approach (IPLS) [10]. The IPLS helps in decomposing the process variables with the key performance indicator related part. Fault diagnosis information is obtained by the test statistics which are designed and the desired performance of the systems is presented. The proposed approach helps in diagnosing KPI faults and also provides the high fault detection rate.

4. A new approach is presented to find the internal cell delay effects using the analog simulation-based fault models[11]. By incorporating the analog simulation in the beginning of the pre-processing stage, the delay fault models are created. To ensure the precise simulation outputs, the cell aware delay diagnosis and cell internal delay suspect was simulated.

5. All the defects present in the FinFET circuits are modelled by the CMOS fault models. Mixed-mode Centaurs TCAD device is used for the simulation of the problems which are present in the circuit and shows that the faults overlap in a planar MOSFET and FINFET[12]. New faults are required to capture the behaviour of the logic gates.

6. This work proposes the direction of key statistical timing analysis problems[13] for analysing the new effective statistical timing algorithms (Non-Incremental/Incremental Computation) on behalf of advanced technology nodes. Moreover it proposes algorithms on behalf of path as well as insignificant delay fault testing applications. Additionally, Sum and Max operations are proposed with these algorithms for efficient fault simulations. The algorithms are implemented on Intel icore 7 2600K processor (32nm conventional CMOS) These models to be implemented for high technology nodes with large process variability.

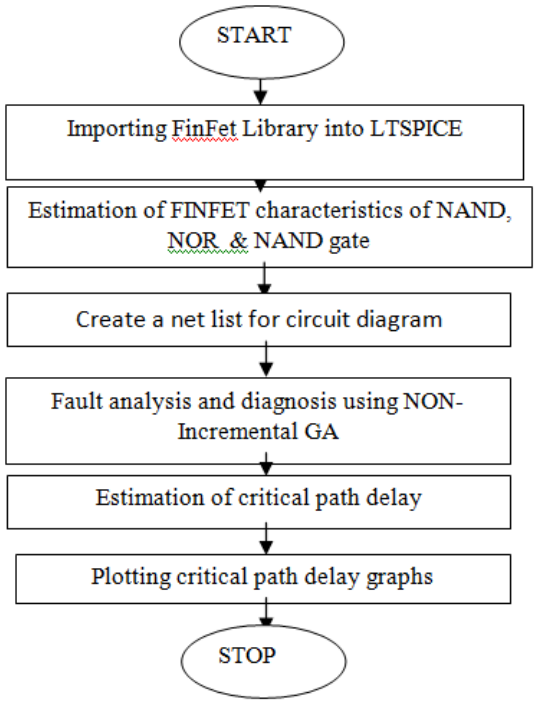
7. Identifying the group of speed limiting paths is a challenging task in designing the system-on-chip (SoC), which in turn converts into a critical situation with the passing of time in stipulated design cycle time[14]. STA analysis is useful in identifying the paths with the help of widely implemented techniques. The problem in the estimation of path delay is due to the involvement of the STA which in turn makes the identification of a realistic set of speed-limiting paths difficult. The implementation of SPICE simulations is an additional technique that accurately provides the estimation of path delay in terms of measured delay on silicon. Nevertheless, it is made unrealistic due to its extended simulation runtime in estimating the path. Compared to SPICE, a new algorithm is presented at an extract level that operates with a great speed and a path delay estimation accuracy of around 94% is maintained. Developing a reliable alert effective method wherein it identifies the timing-critical path set is the main aim in this method. Functional or structural scan is used to examine the number of paths clearly once they are produced and hence small delay defect (SDD) coverage is enhanced. Moreover, the monitoring the study of aging is done in a periodical way in an actual amount of work. In this process, there is a requirement of STA and SPICE models. Therefore, it may be impossible for signing-off the circuit database by replacing the analysis of industry standard multi corner pessimistic STA to achieve fabrication. Validating this method upon the compound industrial designs is involved in the upcoming procedures. From the above Literature it is noticed that Non Incremental Genetic algorithm is not applied for FinFet based VLSI Designs.

III. PROPOSED METHODOLOGY

The proposed method used for fault analysis is non-incremental genetic algorithm. The first step is effective testing and diagnosing of faults to be carried out in FinFet circuits. For this purpose, the designing of NAND, NOT, NOR gates(PTM Library in LT Spice)and then creating a net list for circuit diagram and later importing into MATLAB where Non Incremental Genetic Algorithms are designed (coded) and run for calculation of critical path delay of mean, variance and standard deviation values and plotting the robability density function graph for the critical path delay is performed for designed Circuits 1 and verified same with Test Circuits 2 (**Ref Fig 2).**

Flow Chart of this proposed Method Given below (Ref : Flowchart 1)and iterations in Genetic Algorithm for critical path delay values and fitness function obtained.

Flow Chart-1



3.1. NAND GATE:

The design of NAND gate using FinFET models as shown in the below **figure.1,** shows that V1, V2, V3 are considered as 1V. V1 and V2 are considered as input voltage and V3 is used as power supply to FinFET model. VTC curve and delay calculations is a plot of input vs output. The graph of the transfer curve needs to be plotted. The Vth and Vih VIL, VOH, VOL all these simulation parameters along with the noise margin high (NMH = |VOH - VIH |) and noise margins low (NML = |VIL - VOL|) are calculated and for NOR and NOT gates also results are given **(Ref.Table-1)**

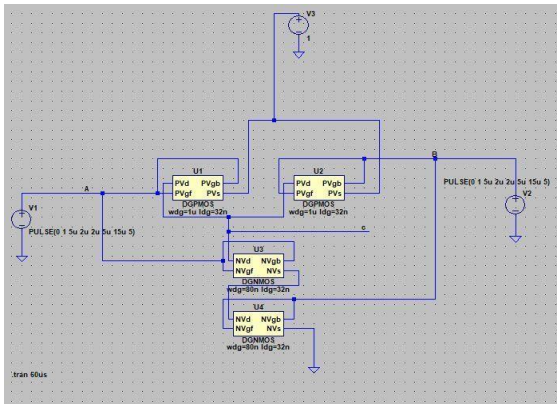


Fig: 1. NAND gate design using FinFET library

After the design of the gates these gates are constructed together to find out the fault analysis and critical path analysis.

3.2. Non-incremental Computation algorithm:

The probability in which one or more target paths are present including the path delay fault is called as target path delay fault probability. Clock cycle time Tclk is smaller than the delay of at least one target path. In spite of finding all the possible ways to calculate the delay path, the computation of the complementary event probability is effective.

$\bar{\psi}$ =P ({Θ ∈ Θ: "none of the target paths has a path delay fault"})

Where,

$\psi=1-\bar{\psi}$

Step 1: Read the initial test vector pair.

Step 2: Simulate the test vector pair to identify the sensitized path. This is attained by the following way.

The simulation of the circuit instances and the test vector pair is performed.

- The transmission towards one gate is achieved at the simulation time and assigning every single transmission at the gate's output is done at the same transition.
- After simulation the references are stored as such. It is identified by the reference of a transition if any sensitized path occurs and is carried till the circuit input is reached.
- the cross check is performed is there is reference to the transition is present for the transition at the output of the gate and identifies all the output transaction corresponding to the input transaction.
- the propagation condition of the gate and the path gets terminated is the transition violates and also if there is no any output transition

Step 3: After identifying the sensitized path by simulation the critical target paths are identified.

Step 4: The condition checks for the test vector pairs. If more test vector pairs are identified then returns to Step2. If not, the critical target path delay distribution is computed.

The process is explained as below, considering n as the amount of critical paths in which the sensitization is performed by the test vectors within a defined subset. The random vector X is given as,

X (X1……. Xn) T

Where

X1…. Xn represent the delays of the critical paths. X represents the vector with multivariate normal distribution.

Step 5: The statistical operation is performed for the dimension reduction and the procedure is continued till a user-defined threshold drops numerous random variables above it. An (n-1) dimensional normal random vector (X1…Xn-2, Y) T approximates the distribution of the random vector is given by as (X1…., Xn-2, max (Xn-1, Xn) T, with the help of a standard distribution-based MAX function application. Till the multiple variables were dropped under the value of a user defined threshold, the procedure will be continued.

Step 6: The numerical integration is carried out and the output path delay fault probability is obtained.

Let m < n denotes the remaining random variable number. Et (X1…, Xm-1, X m) T Nm (μ, Σ) defines the m-dimensional approximation of the maximum delay X.

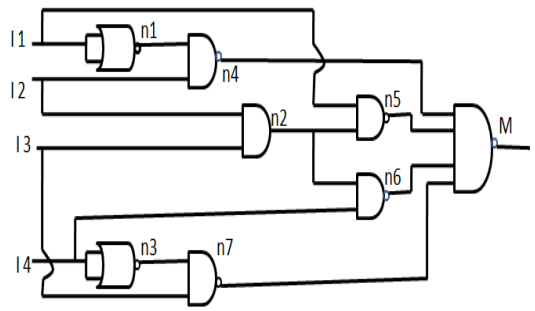
Step 7: We incorporate optimization technique for path delay fault optimization.

The optimization technique employed here will be adaptive genetic algorithm, which aids in reducing the probability of path delay fault. The optimized results are then further processed.

The non-computational genetic algorithm helps in finding the path delay by evaluating the fitness function which shows that higher fitness function means better solution. The critical path delay is the maximum delay between input and output and measured in microseconds.

Genetic Algorithm: GA(n, χ, μ)

// Initialize generation
0:K :=0;
PK: =a population of n randomly-generated individuals;
// Evaluate Pk:
compute Θ(i) for each I ε PK
do{
// Create generation k + I:
// I. Copy:
Select (l χZ) x n members Of Pk and insert into Pk+l;
// 3. Mutate:
Select μ x n members of PK; invert a randomly-selected bit in each;
//Evaluate Pk+l:
Compute 0(i) for each iε PK;
// Increment:
K: K+1;}



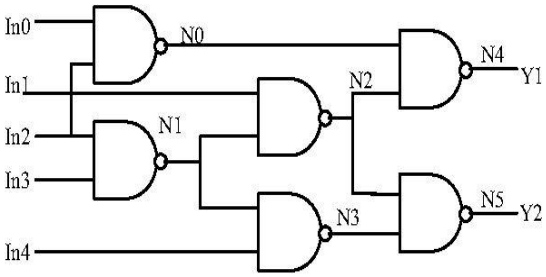


Fig 2: TEST CIRCUIT 1&2

3.2 GATE RESULTS

The simulation parameters for each gate are calculated and transfer characteristics curve is plotted.

$$VIH = \frac{2K\,(Vdd - Vtn + Vtp)}{(Kr-1)\sqrt{1+3Kr}} - \frac{Vdd - KrVtn + Vtp}{Kr-1}$$

$$VOL = \frac{(Kr+1)Vin - Vdd - KrVtn - Vtp}{2Kr}$$

$$VIL = \frac{2\sqrt{k}\,r(Vdd - Vtn + Vtp)}{(Kr-1)\sqrt{Kr+3}} - \frac{Vdd - KrVtn + Vtp}{Kr-1}$$

$$VOH = \frac{(Kr+1)Vil + Vdd - KrVtn - Vtp}{2}$$

Where,

$Kr = Kn/Kp$

The above are the general formulas and the calculations for particular gates are found accordingly

i.NAND GATE:

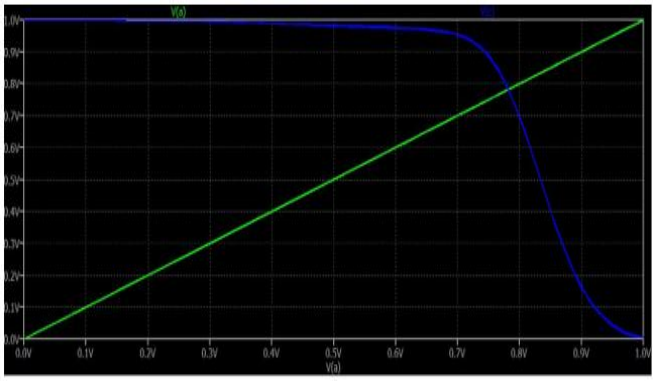


Fig 3: Transfer Characteristics curve f NAND gate.

From the above figure the parameters obtained are showed in Table-1

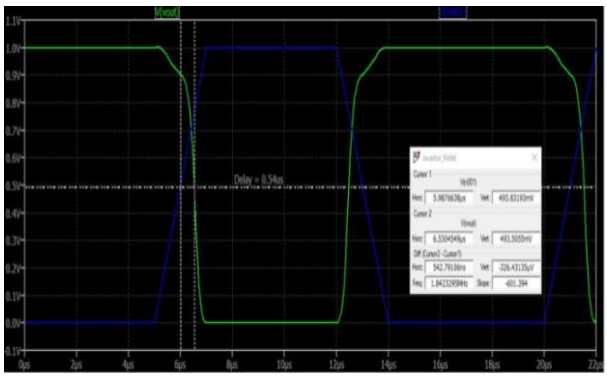


Fig 4: Delay Characteristics of NAND gate

The above fig shows the delay characteristics of the FinFET NAND gate. The steady state values obtained are, High to low propagation delay (tpHL): Time is calculated which falls from VOH to 50%, Lower to higher propagation delay (tpLH): Time is calculated which takes to rise from 50% to VOL Propagation delay is calculated as (tp)= (tpHL + tpLH)/2 =0.67μS,

GATE Results are given below(Table-1)

NAND	NOR	NOT
V_{OH}= 0.9 V	V_{OH}= 0.97 V	V_{OH}= 0.8V
V_{OL}= 1 V	V_{OL}= 0.07 V	V_{OL}= 0.66V
NMH=|VOH - VIH| = 0.02 V	NMH=|VOH - VIH| = 0.25 V	NMH=|VOH - VIH| = 0.07 V
NML = |VIL - VOL| = 0.64 V	NML=|VIL - VOL| = 0.513V	NML = |VIL - VOL| = 0.56 V
Propagation Delay (tp): (tpHL + tpLH)/2 = 0.67 ***μ***s.	Propagation Delay (tp): (tpHL + tpLH)/2 = 0.04 ***μ***s.	Propagation Delay (tp):(tpHL + tpLH)/2 = 0.54 ***μ***s.

IV. RESULTS AND DISCUSSION

4.1. (For Genetic Algorithm)

The results obtained by using genetic computation and the elapsed time is 0.183970 seconds

And the best solution is for the inputs

1111 Fitness value is 0.7400

Total iterations are 101

The graph is drawn for genetic algorithm,**(Ref:CFig 5)**

Results:

GA:

```
Elapsed time is 0.183970 seconds.
Best solution/chromosome
     1     1     1     1

Fitness value
    0.7400

Total iterations:
   101
```

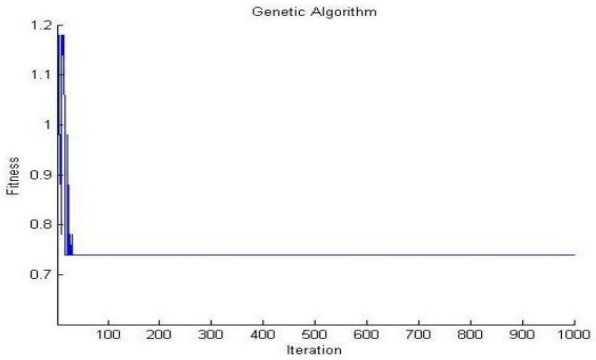


Fig 5. Graph for finding the fitness value in genetic algorithm

4.2 CRITICAL PATH DELAY CCALCULATIONS

The critical path is shown in the below **figure.6** The path is highlighted in red colour **(Circuit 1)**

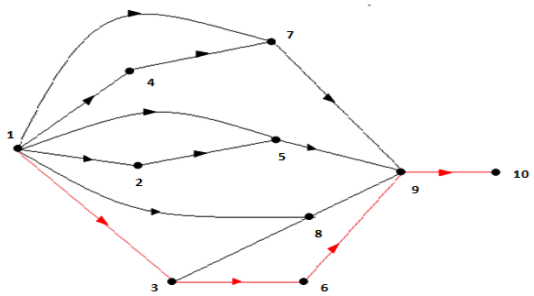


Fig 6: Critical path selected

Example: 1-3-6-9 = 2.68 microseconds. The traverse of 1 to 3 is AND which is 1.34 microseconds and from 3 to 6 NAND gate it is 0.67 microseconds and from 6 to 9 is the path of NAND it is 0.67 microseconds. So, the total of this path is 2.68 microseconds.

Now calculating of the flow of input in every possible path the critical path flow is 1-3-6-9 and 1-3-8-9 which is 2.68 microseconds and that is the critical path value.

Weighted graph for Critical path is displayed in the below

figure 7

```
The critical Path
     1     3     6     9    10

The critical path dealy in micro second
    2.6800
```

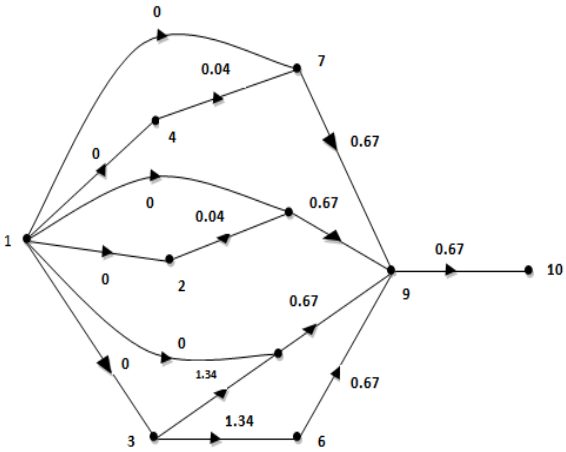


Fig 7: Weighted graph for Critical path

V. PDF OF CRITICAL PATH:

Mean: The mean is calculated by the critical path consideration for 1-3-6-9 so the mean values are added and the total mean is 2.68 microseconds

Standard deviation: consider 99.7% delay covers within the range of o to 2 microseconds. To cover 99.7% the standard deviation is

$\sigma t = \sigma 1 + \sigma 2 + \sigma 3 = 0.33$ micro

Total σt 0.33+0.33+0.33+0.33=1μS

Thus, the above values which are calculated is plotted in the below graph **(Fig 8)**

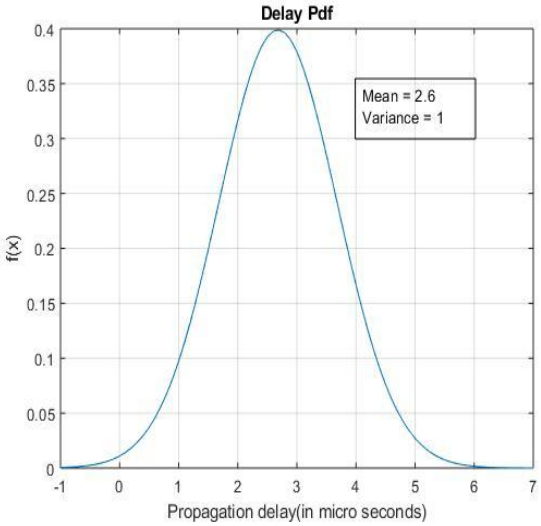


Fig 8. PDF Graph of time delay

Similar to the above process, we have measured for **Test circuit 2** for different outputs and the corresponding results are displayed in the below sections,

The critical path for test circuit 2 for output 8 is shown in the below **figure.9** The path is highlighted in red colour.

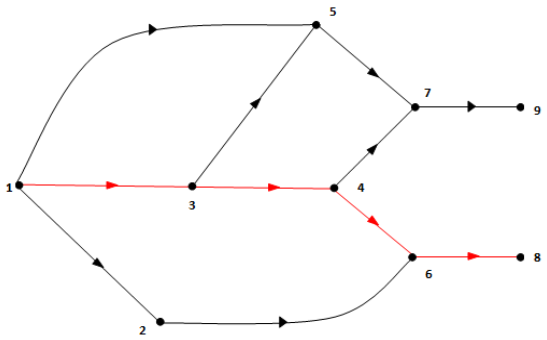


Fig 9: CRITICAL PATH Selected

The critical path for test circuit 2 for output 9 is shown in the below figure. The path is highlighted in red colour (1-3-4-9 and Critical path delay is 2.01μ secs)

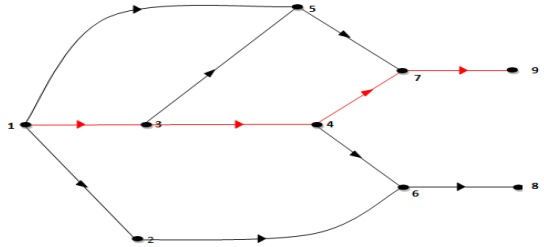


Fig 10: CRITICAL PATH Selected

Weighted graph for the critical path is displayed in the below **figure 11 (Circuit 2)**

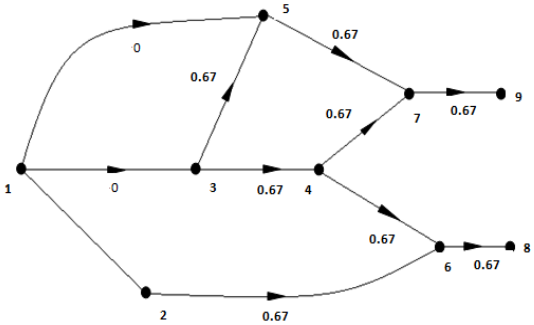


Fig 11: Weighted graph for test circuit 2

VI. CONCLUSION

In this paper, designing of NAND, NOR and NOT gates are done using FinFet model & each gate with logic outputs are verified as shown in graphs. The simulation results show that for each gate VTC curves has been plotted and delays, noise margin values (VTh, VIH, VIL, VOH, VOL, NMH, NML) are obtained. The circuit diagram is designed and faults are analyzed. Using Non-incremental genetic algorithm, best vector selection is found. Furthermore, calculating critical path delay , PDF of Critical Path Delay and Fitness value for path delay iterations are plotted.(i.e., max delay between input & output) using different input parameters. From critical path analysis, the values of Mean, Variance, and standard deviation are calculated & critical path is plotted in graph. Genetic Algorithm iterations for convergence of path delay values obtained. Thus, the FinFet circuits are having better test performance by integrating the two algorithms, thereby for reducing the faults. Further, the FinFet based applications are considered and the device performance is calculated and helps in reducing power consumption, delay etc.

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Second Author profile which contains their education details, their publications, research work, membership, achievements, with photo that will be maximum 200-400 words.

Dr.Sriharirao Patri is working as Assoc Prof at NITWarangal in the dept.of ECE. His Research intrests include RFIC Design, VLSI Testing, Fault Diagnosis Analog/digital IC design, DSP Architecture, Analog LDO's. He has published 10 technical papers in Reputed international journals/Presented in Conferences. He has conducted various cour in VLSI area and guided 5PhD Students.