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Performance of Efficient CMOS Power Amplifier for ISM Band Applications

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Abstract: ***Power amplifiers are one of the most important functional blocks in the Radio Frequency (RF) frontend for reliable wireless communications. The power amplifiers amplify and boost the input signal to needed output power. The signal is amplified to create it sufficiently high for the transmitter to propagate the needed distance to the receiver. Such as power amplifiers are expected to need low-power communication while producing a relatively high output power with more efficiency. The trans-receiver has various blocks such as filters, Voltage Control Oscillator (VCO), Low Noise Amplifier (LNA) and power amplifier. Among these, the most power hungry device is a power amplifier. The efficiency of the power amplifier can be 100%, but practically it is just 55%. So, the scope of improvement in efficiency in a power amplifier will be an interesting and most challenging task. As well defined architecture, including linear functional block synthesis, which is complex in designing CMOS power amplifier for different applications. This article describes the different state-of-the-art design biasing class and advanced RF CMOS power amplifier for Industrial, Scientific, and Medical (ISM) band applications.***

Keywords: ***complementary metal–oxide semiconductor, radio frequency, power amplifiers, and reliable wireless communication.***

I. INTRODUCTION

Generally, the power amplifier is the last block of a Transmitter Systems (TSs). It amplifies a weak signal to a power level required to transmit a signal, which is called a large signal amplifies. Due to the fact that in order to get a large signal power at the output, the voltage of the input signal should be very large. The PA has a wide application area such as Bluetooth, radar system, Wireless Lane Area Network (WLAN), mobile communication, and also medical, military applications [1],[2]. Based on applications power amplifiers can be categorized into two types such as Audio Power Amplifiers (APA) [3], [4] and Radio Frequency Power Amplifiers (RFLPs) [5], [6]. In RFPA, RF signals amplifying a specific band of frequency and avoiding the unwanted frequency components. The APAs perform with the audio frequency range, for example driving a loudspeaker.

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The demand for a low cost and system on a chip for mobile terminals has led to the development of a highly integrated, a low distortion and high power efficiency CMOS power amplifier for wide baseband applications like Long Term Evolution (LTE) [7].

Traditional CMOS power amplifier is a double stage differential source-grounded amplifier with inductive load [8], [9], linearization methods have been utilized to enhance distribution and power efficiency [10], [11]. In the past decades, many power amplifiers has been proposed to enhance both power amplifier Power Back-off (PBO) efficiency and linearity. Dynamically adapting the power amplifier biasing current to the envelope signal can enhance the AM-AM linearity but may not address the AM-PM linearity [12], envelope elimination and restoration power amplifier [7], polar power amplifier scheme [13], poses a stringent trade off on supply modulator for its efficiency, dynamic range and bandwidth [14], frequently compromising the performance in practice. In envelope tracking power amplifier [15], the supply modular requirements are relaxed, minimized the peak efficiency because of utilizing of a linear power amplifier as opposed to switching power amplifier in envelope elimination and restoration systems and increases the complexity for pre-distortion. The Direct Digital Amplitude Modulation (DDAM) is another polar power amplifier. Although, generally single branch DDAM power amplifiers are achieved class-B PBO efficiency performance only [16]. In this paper, different types of the power amplifier are reviewed. This review based on a fully integrated power amplifier utilizing CMOS technology. The most of amplifiers presented in this paper are performing at various frequency bands and aiming at applications for wireless services such as 5G, satellite communication and so on. Finally, the performance of existing power amplifier methods is analyzed in terms of linearity, output power, power consumption, power gain and power added efficiency, which is tabulated.

II. POWER AMPLIFIER

Design of power amplifier is one of the challenging tasks in the Very large scale integrated (VLSI). Earlier Bipolar Junction Transistor (BJT) were utilized for fabricating amplifiers. However, with the start of CMOS technology, the Metal Oxide Semiconductor Field Effect Transistors (MOSFET) have found huge applications in the fabrication of analog as well as digital circuits. Otherwise, employing MOSFET has its consequences.

This paper compares the designs of different power amplifiers utilizing CMOS technology. Because of the basic idea behind utilizing CMOS technology is a reduction in cost and size and at the same time requirement of low power [17]. Several various topologies and design strategies exist that help with designing of these amplifiers. Block diagram of the CMOS power amplifier is shown in figure .1. It is consists of two stages such as driver stage and power stage. These both stages are biased with individual bias voltages. Various configurations are applied to the driver stage and the power stage to operate properly [18].

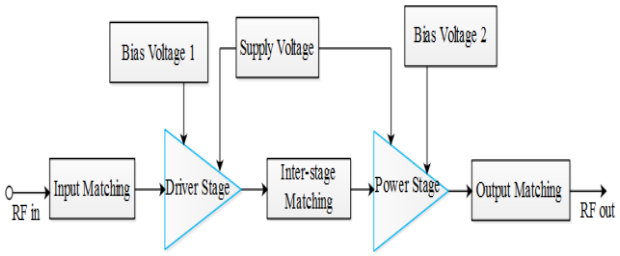
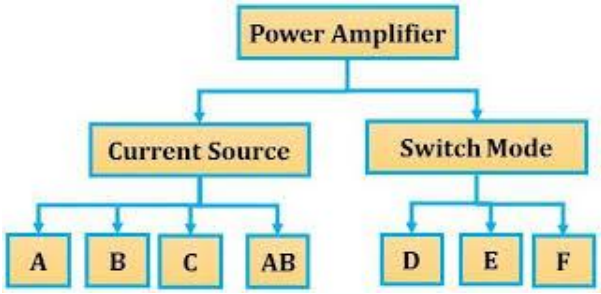


Fig. 1 Block diagram of the CMOS power amplifier

Input and output matching networks are utilized to minimize the return losses to achieve a high gain and output power. Although inter-stage matching is also needed between power and driver stages. In the last decade, various PA design architectures (general cascade, self-biased cascade, differential cascade, power combining) have been introduced to achieve the desired performances. These architectures are suffered by non-linearity, high power consumption, low output power, low gain and low power added efficiency [19]. Hence, a high-performance power amplifier must urgently be modeled to satisfy the rising demands for industrial, scientific and medical (ISM) band applications. This paper is aimed to analyze the different aspects of the design and performance of a power amplifier for ISM band applications.

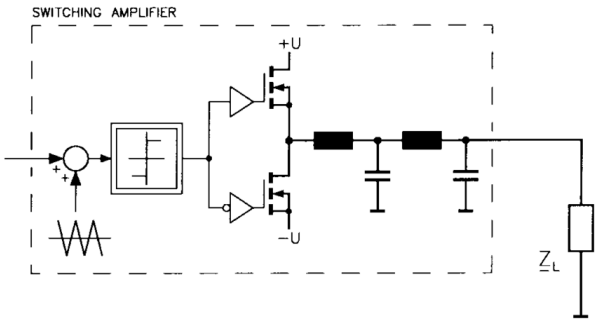
Taxonomy of power amplifier

The power amplifier can be classified based on power classes A, B, C, D, E, F, AB and so on. The power classes are categorized based on the types of bias applied to the RF transistors. The classes A, B, an AB are represented as linear amplifiers, and classes C, D, E, and F are labeled as non-linear amplifiers.



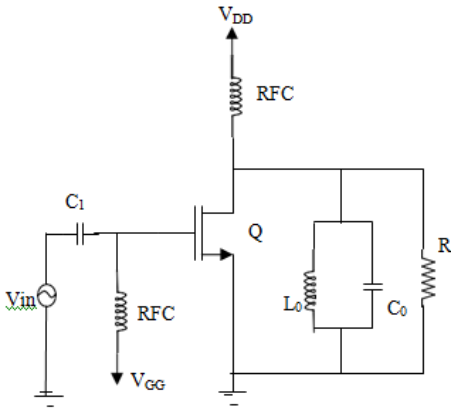
Linear based power amplifier

The class-A amplifier is biased such that the output device of amplifier conducts 360◦ throughputs the full cycle and as a consequence, the power loss is increased in which turn leads to having low efficiency. By differently, the class-B amplifier is operated similarly to class - A amplifier, but its output device conducts only a half of the sinusoidal cycle. Hence, the power loss is reduced and efficiency is improved compared to class A-amplifiers. Finally, the class AB amplifier is a combination of class-A and class-B amplifiers, in that both amplifiers can be on at the same time for a short period and hence enhances the efficiency [20]. The limitation of power dissipation more in this amplifier that utilized in the restricted area of low-frequency range. Further, these 4- types of amplifiers used in the restricted area of a low-frequency range. In these four types of the amplifier, further classified according to their biasing conditions and conduction angles.



Non-linear power amplifier

The class-C amplifier, conducts less than half cycle, experiences higher distortions and noise effects [21]. However, the efficiency of the class C power amplifier is better, which suffers from poor dynamic range. The class D amplifiers also known as the switching amplifier, it has a low power loss because the active devices are kept either fully on or fully off. Class E amplifier is preferred for the design of RF power amplifiers because class E has a higher theoretical efficiency than classes D and F. Class F amplifier operates in a unique manner by implementing the output network such that drain voltage and drain current do not overlap with each other. The non-linear characteristics but has better efficiency and again. Here, with the help of some linearization methods are used to working in a power amplifier for a given frequency range. It is expressed in Eq. (1.1)



Power dissipation = $\int_0^{2\pi} Vm \times Im \sin(\emptyset - \pi) d\emptyset$ (1.1)

Hybrid class amplifier

The hybrid class power amplifier has its benefits and limitations respectively of combination if two- various classes. To solve these drawbacks and further developments will be dome with many classes such as classes BD power amplifier, class EF power amplifier are the particular classes of interest. To design this power amplifier the use of class EF will give special attention to get better performance with low voltage supply. This operating class has the benefit of getting high bandwidth with frequency range is a form of 1.5 to 3 GHz.

III. PERFORMANCE PARAMETER

The performance of the CMOS power amplifier has evaluated in terms of several parameters. Most significant aspects of a power amplifier design are output power, power gain, power consumption, PAE, etc. An inevitable trade-off exists among these factors and these trade-off creates power amplifier design challenging at CMOS downscaling. These key factors used for assessing transmitter performance has described as follows.

Power consumption

Total power consumption of a power amplifier is the sum of dynamic and static power consumption. It is defined as equation (1.2).

$$P_{total} = P_S + P_D \quad (1.2)$$

Where P_S is static power consumption and P_D is dynamic power consumption.

Output power

The output power refers to the quantity of power that must be delivered to the load and it is considered the most significant aspect of a power amplifier design. The power gain and efficiency have a trade-off with output power. Output power is denoted by dB and expressed as Eq. (1.3).

$$P_{dBm} = 10lg\frac{P_{out}}{10^{-3}} \quad (1.3)$$

Where P_{out} represented real output power with Watt as its unit.

Efficiency

The efficiency of the power amplifier can be categorized into two types: Drain efficiency and PAE. Drain efficiency is the ratio of the RF output power to Direct Current (DC) power dissipation, which is defined as in equation (1.4). The PAE is defined as the output power gained subtracted by the input power and then divided by the DC power dissipation, as shown in equation (1.5).

$$Drain\ efficiency = {P_{out}}/{P_{(DC,drain)}} \quad (1.4)$$

$$PAE = {(P_{out} - P_{in})}/{P_{(DC,drain)}} \quad (1.5)$$

Where P_{in} is input power.

Linearity

Linearity is defined as the scenario in which the output of the device varies linearly with respect to the variations of the input. Linearity has become increasingly significant in current RF communication structures. High linearity means that the P_{out} gained is linear to the input power.

Power gain

Generally, power amplifiers have one to three stages and the drive stage can only output a few milli watts (MW). Thus, the power gain requires to be taken into account. It is expressed as in equation (1.6).

$$power\ gain = \frac{P_{out}}{P_{in}} \quad (1.6)$$

Hence, to satisfy the current demand, the power amplifiers should be designed to have less power consumption, high output power & power gain, high PAE and linearity.

IV. EFFICIENT RF POWER AMPLIFIER ARCHITECTURE

Power amplifier design has developed rapidly and has become more advanced. The rapid growth of ISM band devices demands a low cost and low power consumption solution. However, considerable achievements have been attained in CMOS, and analyzing this goal remains challenging for System-on-Chip (SOC) designers. This section provides a description of every advanced RF power amplifier that has been potential to be implemented.

Envelop Tracking RF power amplifier

This architecture is significant improvement technique depends on the order envelop EER architecture, incorporating a modulator for shaping the PA power supply according to low-frequency envelope. The efficiency of the envelop tracking power amplifier is roughly the product of envelope amplifier, significantly and RF power amplifier drain efficiency. It can be expressed in (1.7).

$$\eta_{overall} = \eta_{Envelop\ amp}.\eta\ RF\ power\ amplifier \quad (1.7)$$

Hence the model of high-efficiency envelope amplifier is complex to the overall efficiency of envelope tracking power amplifier system.

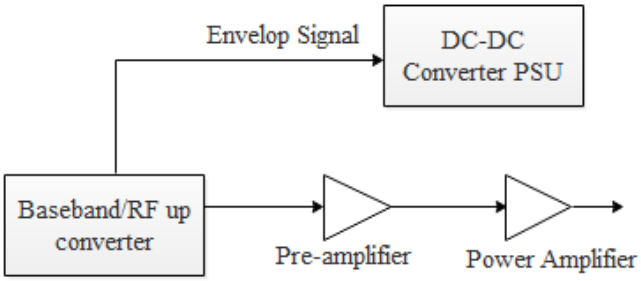


Fig. 2 Block diagram of envelop tracking RF power amplifier

Figure .2 shows the block diagram of envelop tracking RF power amplifier. Envelop tracking block depicts that the DC-DC converter has been replaced by Envelop Racking Supply (ETS). This takes in information about the envelope to ensure that it provides the correct voltage output to the RF power amplifier, so that it runs in its linear portion but dissipating the minimum heat.

The architecture requires high power regulators with precise control, which is the major drawback of envelope tracking RF power amplifier.

Doherty RF power amplifier

Doherty power amplifier is based on Active Load Concept (ALC), which is suitable decrease the impedance transmission of Active Amplifying Device (AAD), hence forcing the latter to operate its high-efficiency conditions for a pre-determined range of input and output power levels. The active load concept highly depends on output impedance inverter therefore latter receivers several researcher attention.

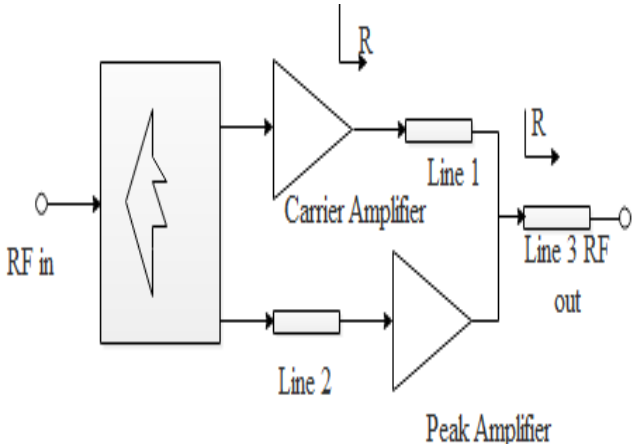


Fig. 3 Block diagram of Doherty RF power amplifier

Figure.3 shows the block diagram of Doherty RF power amplifier. It is consist of splitter, carrier amplifier, peak amplifier and three Quarter Wave Transmission (QWT) lines. The carrier amplifier is realized by Linear Power Amplifier (LPA) to satisfy the linear requirements of the RF output signal. In order to improve the efficiency of carrier amplifier at power back off region, and peak amplifier, it is realized by a Non LPA because of its high efficiency, and line 1areused to modulate the load resistance of carrier amplifier by using Active Load Pull (ALP) method. Since line one introduce 90° phase shift to RF output signal from the carrier amplifier, line 2 is added to RF path of peak amplifier to balance the phase shift. The third line is added to find impedance transformation because the output impedance of a typical RF system is 50 Ohm. The RF input signal is divide into 2 categorizes by using splitter. When the input power range is very low at the time only the carrier amplifier performs and peak amplifier is shut down. In Doherty power amplifier, power added efficiency can be defined utilizing the following equation (1.8).

$$\eta PAE = \frac{P_{out} - P_{in}}{\sum_{n=1}^{m} V_{DDn} I_{DQn}} \quad (1.8)$$

Here V_{DDn} represents power supply of n^{th} power amplifier in Doherty power amplifier configuration, I_{DQn} represents quiescent current consumed by power amplifier and m is total parallel power amplifier branches. The Doherty power amplifier is very simple and less complex circuitry reacting to the input signal required compared to envelope tracking architecture.

Out phasing RF power amplifier

The out phasing modulation scheme is used to improve both linearity and efficiency of AM broadcast transmitter. Considerably, its applications are extended up to microwave frequency under the Linear Amplification and Nonlinear Component (LINC).

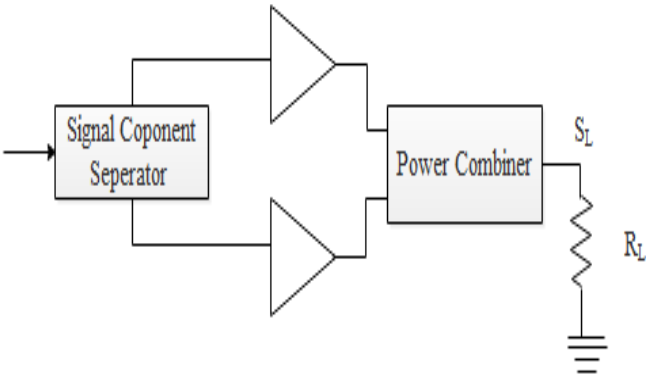


Fig. 4 Diagram of out phasing RF amplifier

Figure.4 shows the diagram of Out phasing RF amplifier. The out phasing as a linear power amplifier system for Amplitude Modulated Signal (AMS) having linear transfer function over a wide range of the signal levels of input by combining outputs of 2-nonlinear power amplifier, which are driven with signals of Constant Amplitude (CA) but various time-varying phase corresponding to envelop of the input signal. Theoretical out phasing power amplifier efficiency comes close to 100% where the practical power amplifier compensation can be defined in equation (1.9).

$$\eta_{outphasing\ power\ amplifier} = \frac{2cos^2\phi}{\sqrt{(2cos^2\phi)^2 + (sin2\phi - \sin 2\phi_{comp})^2}} \quad (1.9)$$

Here, ϕ is outphasing angle, ϕ_{comp} is compensation angle. For outphasing power amplifier, particular power combiner needed. General power combiner do not provide sufficient performance, hence particular phase compensated ones are needed. Furthermore, power combiner also one of the major issue.

V. LITERATURE SURVEY

This literature review shows that few efficient techniques are available for power amplifier designs. The development of CMOS power amplifiers is operating at a different frequency that is explained in this study in terms of power amplifier techniques and performance point of view. Researchers suggested many optimization techniques to improving linearization and bandwidth of power amplifier. In this section, a brief evaluation of some significant contribution to the existing methods is presented about power amplifiers. In Table.1, shows the advantage, disadvantage and performance measure are described for existing power amplifier designs.

Table. 1 Performances comparison of the CMOS power amplifiers

Authors	CMOS technology	Supply Voltage	Performance Measure
Oishi et al. [8]	90 nm CMOS	0.9 V	PAE – 39 % and Adjacent channel leakage ratio is -41 dB.
Kaymaksut et al. [10]	40 nm CMOS	1.5 V	Frequency of 1.9 GHz. Output power 23.4 dB. Gain 21.3 dB.
Haghighat et al. [21]	180 nm CMOS	3.3 V	Center frequency 2.6GHz, PAE is 31.25 in maximum linearity point. 12.3% improvement at power level. Output power 20.2 dB.
Solar et al. [22]	180 nm CMOS	3.3 V	The power gain of 21.1 Db. PAE is 29%.
Kaymaksut et al. [23]	40 nm CMOS	1.5 V	Peak PAE of the amplifier is 34 %, BOLs are still as high as 25.5% and 19.7%. The amplifier achieves 18.4% PAE.
Ryu et al. [24]	130 nm CMOS	3.3 V	1-dB compression point (p1) of 31.9 dBm. PAE at p1 dB of 51%. Output power 22.8 dBm and of 30.1 % were obtained.
Santos, E. L et al. [26]	130 nm CMOS	1.8 V	Power gain 26.5 dB and 35.9 dB and a peak PAE of 38 % with a 1.8 V power supply. The power consumption of the PA is minimized from 225 mW in the highest-gain mode to 179 mW for the lowest gain.
Kang et al. [27]	180 nm CMOS	2.8 V and 3.5 V	A PAE of 34%, an Error Vector Magnitude (EVR) of 3.2%, and an Adjacent Channel Leakage Ratio (ACLR) of -32.5 dB at an average output power of 26 dBm.
dos Santos et al. [28]	130 nm CMOS	Stable DC power supply	Gain from 22.4 dB to 31 dB, with power consumption ranging from 171 mW to 196.2 Mw.

VI. CONCLUSION

This paper comprehensively discussed the class of power amplifier and different advanced RF power amplifier architectures of CMOS power amplifier design. Many researches have been developed by various researchers to enhance the performance RF power amplifiers in CMOS technology with different nm technology. Several researchers have tried to maximize the output power, improve linearization, bandwidth, and several others have worked to minimize the power consumption to achieve ultra-low power. From this review, a few studies have enhanced the power gain. Performance requirement of the specific parameter must be identified and focused on designing CMOS power amplifier. Linearization, output power, power efficiency, and consumption are the major performance parameters of PA that are must be considered. The comparison table showed that the Doherty RF power amplifier IS highly suitable for designing an efficient CMOS power amplifier and that can analyze the demand for PAE, output power and high power gain by ISM band communications. Finally, the class biasing for PA would be class AB if high efficiency is highly demanded desired power amplifiers.

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