

Issues on High Speed Relaying in High Voltage Transmission lines using Full Cycle Discrete Fourier Transform and Phaselet Transform



M Naga Chaitanya, G V Siva Krishna Rao

Abstract: *Now-a-days Phaselet Transform based distance relaying scheme is being proposed in the literature for high speed relaying in high voltage lines to obtain response times less than one quarter cycle. Phaselets are gaining importance due to their better transient response compared to Full Cycle Discrete Fourier Transform (FCDFT) during dynamic situations. But there are few operational issues with phaselets that have to be observed closely. In this paper, a single end feed test system with phaselet/FCDFT was simulated in MATLAB platform with various test cases. Then the performance of phaselet based distance relaying scheme is compared with the conventional Full Cycle Discrete Fourier Transform. Results are reported in this paper.*

Keywords : *High Voltage lines, High speed relaying, Phaselet Transform, Full Cycle Discrete Fourier Transform.*

I. INTRODUCTION

In electric power systems, HV and EHV transmission lines are basically tie lines between two grids or power stations. Selectivity and Speed of relaying are extremely important as the voltage level increases. This is to maintain transient stability between sources, protect the equipments from high faults currents and also to eliminate wider dislocation of loads. Hence considering the above factors, fast acting distance relays are commonly used in high voltage lines.

According to the synchrophasor initiative in India[1], several PMUs are installed by RLDCs/NLDCs at major transmission interconnections, interfaces and major 400 kV/220 kV/132 kV substations. PMUs are the devices capable of measuring frequency, voltage, current waveforms along with phase angles at high sampling rates. Phasor is representation of a sinusoid using its magnitude and phase angle. Many analog and digital distance relays use phasors as the operating signals in distance protection functions. In order to estimate these phasors, many digital algorithms were available.

Discrete Fourier Transform (DFT) is one which is widely used in digital distance relays. DFT can be computed by taking any size of data window, but conventionally they consider either the full cycle window or half cycle window. The advantage of Half Cycle Fourier is that, it requires half the samples than Full Cycle Fourier to compute the fundamental phasor i.e., the fundamental phasor is computed in half the cycle i.e., 10ms for a 50 Hz system. But if we observe their filtering abilities, Full Cycle Fourier is immune to harmonics but effected by decaying DC offsets and Half Cycle Fourier is effected by both even harmonics and decaying DC offsets[2]. Noticeable efforts are also made to improve the performance of Full Cycle DFT and Half Cycle DFT in presence of decaying DC offsets and harmonics[3]–[9]. Attempts are also made to estimate the phasor with different basis functions also. A way to compute the fundamental phasor faster than FCDFT by wavelets is given in [10]. But it also suffers from the inaccuracies due to decaying DC offsets and harmonics. In [11], Phasorlet based estimation considers only fraction of sampled data to compute the phasor. It is faster than others only if the signal is pure sinusoidal. This concludes that most of the phasor estimation techniques fail to converge at a faster rate if the signal is not pure sinusoid.

In [12],[13], a new approach for computation of Fourier transform using phaselets has been introduced and applied in transmission line differential relay. This improved the operating time of the relay. But phaselets are initiated only after the fault has been triggered. The fault has to be sensed by the relay or by some fault sensing algorithms in order to initiate the phaselet. This sensing time should also be considered while evaluating the performance of this new approach.

In [14], authors has implemented high speed distance relaying scheme on FPGA and shown fast and secured tripping decision by mho relay. Application of phaselets for detection of voltage flickers due to distributed generators is presented in [15]. Distance relays are prone to maloperation due to power swings initiated after fault clearance in a heavily stressed line. A method utilizing phaselets for power swing identification and blocked is reported in [16].

In this paper, performance of Phaselet over FCDFT based distance relay is compared. The effect of relay fault sensing time on these algorithms is also studied. This is to show that FCDFT is still a better relaying algorithm under dynamic conditions. Session II and III introduces basic mathematical relations of FCDFT and Phaselet for phasor estimation.

Revised Manuscript Received on December 30, 2019.

* Correspondence Author

M Naga Chaitanya*, Department of Electrical and Electronics Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, A.P, India

G V Siva Krishna Rao, Department of Electrical and Electronics Engineering, Andhra University College of Engineering (A), Andhra University, Visakhapatnam, A.P, India.

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an [open access](http://creativecommons.org/licenses/by-nc-nd/4.0/) article under the CC-BY-NC-ND license <http://creativecommons.org/licenses/by-nc-nd/4.0/>



Results showing the performance of the two relaying algorithms, when different parameters of the test system are varied are discussed in session IV. Finally Section V concludes up with the key issues observed in this research work.

II. DISCRETE FOURIER TRANSFORM BASED PHASOR ESTIMATION

Full Cycle DFT for estimating the fundamental frequency phasors of a sampled system signal $\{x(n)\}$ is given by the following equations:

$$\bar{C} = \frac{2}{N} \cdot \sum_{k=0}^{N-1} x(k) \cdot \cos \frac{2\pi k}{N} \quad 2.a$$

$$\bar{S} = \frac{2}{N} \cdot \sum_{k=0}^{N-1} x(k) \cdot \sin \frac{2\pi k}{N} \quad 2.b$$

$$\bar{X} = \bar{C} - j\bar{S} \quad 2.c$$

$$|\bar{X}| = \sqrt{\bar{C}^2 + \bar{S}^2} \quad 2.d$$

$$\angle \bar{X} = \tan^{-1} \frac{-\bar{S}}{\bar{C}} \quad 2.e$$

Where N denotes number of samples/cycle.

For a window length of integral multiples of half cycle, sine and cosine components are orthogonal to each other. Hence, projection of the signal onto these orthogonal basis, gives us accurate phasor estimation. But on the other hand, if it is required to estimate the phasor with a window less than integral multiples of half cycle, cosine and sine components of DFT form an oblique basis and are no longer orthogonal. So the projection of the signal onto these oblique basis, does not give an accurate result. Now for such shorter windows, a correction matrix is required to compute fundamental phasor.

In real time operation, signal samples keep on streaming into the digital device at every sampling instant. Hence at every sampling instant a new phasor has to be computed considering this new sample or old phasor has to be updated. Considerable amount of computation time can be saved by relating the DFT computed in one data window to the new data window. A new data window is formed by considering the newest sample and removing the oldest sample from the old data window. As the window moves over one sample at a time, the new i^{th} phasor is computed from $(i-1)^{\text{th}}$ phasor by the following equations, where \bar{X} is a phasor and N is the full cycle sample size [17],

$$\bar{X}^{(i)} = \left\{ \bar{X}^{(i-1)} + j \frac{\sqrt{2}}{N} (x_{N+i} - x_i) e^{-j \frac{2\pi(i-1)}{N}} \right\} \quad 2.f$$

Under normal operation of the power system i.e., the DFT window keeps on moving and estimates the phasor. During a fault for one cycle of fault inception, the window consists of both the pre-fault samples and post-fault samples. This contamination of window introduces transient error during the one cycle time after the fault has occurred.

III. PHASELET BASED PHASOR ESTIMATION

Phaselets are partials sums of product of the signal samples and their corresponding sine and cosine scaling factors. Such phaselets are accumulated over the adaptive window sizes and phasor is computed. The window size in phaselet computation is not restricted to integer multiple of a half cycle at the power system frequency. The phaselets are calculated according to:

$$C_{\text{phaselet}}(p) = \sum_{k=p \cdot P}^{p \cdot P + P-1} x(k) \cdot \cos \frac{2\pi k}{N} \quad 3.a$$

$$S_{\text{phaselet}}(p) = \sum_{k=p \cdot P}^{p \cdot P + P-1} x(k) \cdot \sin \frac{2\pi k}{N} \quad 3.b$$

Where p is the phaselet index and $C_{\text{phaselet}}(p)$ is the cosine part of the p^{th} phaselet and $S_{\text{phaselet}}(p)$ is the sine part. Constants N, P are the number of samples per cycle and number of samples per phaselet. There will be N/P number of phaselets per cycle and should be an integer. As the window size of the phaselet increases, it encloses the previous phaselet samples and the combined cosine and sine components are given by:

$$C_{\Sigma \text{phaselet}}(n) = \sum_{p=n \cdot \frac{W}{P} + 1}^n C_{\text{phaselet}}(p) \quad 3.c$$

$$S_{\Sigma \text{phaselet}}(n) = \sum_{p=n \cdot \frac{W}{P} + 1}^n S_{\text{phaselet}}(p) \quad 3.d$$

Where n is the phasor index and W is window size in samples. The window size is adaptive, which increases in a linear fashion. $C_{\Sigma \text{phaselet}}(n), S_{\Sigma \text{phaselet}}(n)$ are the cosine and sine part of the sum of all phaselets inside the specified window, which is a function of phasor index (n). Here, it is required to note that the window size starts with the first p samples and then increases to $p+1$ samples and goes on till the full cycle samples are reached. Hence, cosine and sine parts computed for the phaselets are no longer orthogonal till full cycle is reached. Hence for such shorter windows a correction matrix is required and the computations of actual phasor components are as given below [18]:

$$\begin{bmatrix} \bar{C}_n \\ \bar{S}_n \end{bmatrix} = \begin{bmatrix} T11(n, W) & T12(n, W) \\ T21(n, W) & T22(n, W) \end{bmatrix} \cdot \begin{bmatrix} C_{\Sigma \text{phaselet}}(n) \\ S_{\Sigma \text{phaselet}}(n) \end{bmatrix} \quad 3.e$$

Finally the phasor magnitude and angle will be obtained according to the Equations (2.d, 2.e).

Under normal conditions, the phaselet window is fixed to N and phasor computation is same as FCDFT and slides over the samples. But once a disturbance is detected, the window is initialized to P and contains only fault samples. The pre-fault samples are not considered in the window. Then the window size increases until it reaches on full cycle N . After one cycle after a fault, the window is fixed to N and the phaselet computed is same as that of FCDFT. If there is any disturbance in the system, the phaselet procedure is again initiated. This makes phaselets to show a better transient response over the FCDFT by using partial sums of cosine and sine components over adaptive window.

IV. SIMULATION RESULTS AND DISCUSSIONS

The effect of variation of fault inception angle, load, source impedance, and fault resistance on Phaselet and FCDFT based distance relays have been studied on test system shown in the Fig. 1. Test system is modeled in MATLAB SIMULINK [19]. Phaselet and Sliding mode DFT algorithms are programmed on the same platform in Intel(R) Core(TM) i3-2310M CPU @ 2.10 Hz personal computer.

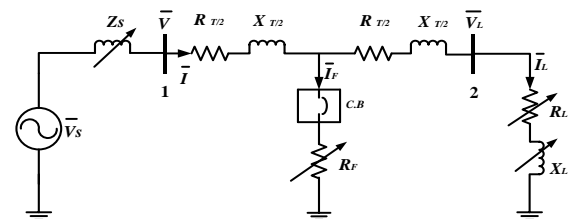


Figure 1. Schematic diagram of single end feed test system

1000MVA and 765 kV are considered as the base values for the test system. The signals are sampled at 80 samples/cycles (4000 Hz). The number of samples/phaselet are 4. In this system, fault inception angle, source impedance, load, fault resistance are varied over a range. In every test case, it is considered that fault takes place at half the length of the transmission line. Transmission line impedance is fixed at $(0.02+j0.2)$ pu.

In order to compare the performance of FCDFT and Phaselet as relaying algorithms in distance relays, four different cases are considered. In each case, Z_{est} indicates fault impedance estimated by the relay, $t_{o_phaselet}$ denotes the operating time of Phaselet based relay and t_{o_DFT} denotes the operating time of FCDFT based relay. It is to emphasize that the two times defined above does not include the relay fault sensing time. It is to be observed that, sliding mode FCDFT does not require any additional fault sensing time. In Phaselet based relaying scheme, phaselets are triggered only when the fault is sensed. Typically fault sensing time for a static relay is in the order of one T_{cycle} , where it denotes one cycle time at power system frequency. Hence, taking fault sensing time also into account $t'_{o_phaselet}$ denotes the total operating time of Phaselet based relay. The difference between the operating times between the two relays is denoted by t_{diff} . Relays trip setting is kept at 0.8 times the transmission line impedance. The fault was initiated at 0.4ms by closing the circuit breaker.

Case A: Effect of variation of fault inception angle:

In this case (the fault in zone-1), fault inception angle is varied from 0^0 to 180^0 . Fault impedance estimated by the FCDFT based distance relay and Phaselet based distance relay is shown in Fig.2. The details of the test results are given in Table I.

TABLE I
DETAILS OF TEST CASE-A

System Parameters: 1000 MVA, 765 kV, $Z_s=0.1$ pu, $R_F=0.01$ pu, $Z_L=0.5$ pu, $R_{T/2}=0.01$ pu, $X_{T/2}=0.1$ pu.

Φ^0	$t_{o_phaselet}(ms)$	$t_{o_DFT}(ms)$	$t'_{o_phaselet}(ms) = t_{o_phaselet} + T_{cycle}$	$t_{diff}(ms)$
0^0	0.035	15.75	20.35	15.4
30^0	1.45	14.35	21.45	12.9
60^0	2.35	14.15	22.35	11.8
90^0	3.25	15.05	23.25	11.8
120^0	10.95	16.75	30.95	5.8
150^0	8.35	17.15	28.35	8.8
180^0	0.35	15.75	20.35	15.4
			Average(t_{diff})	11.7

From Fig.2 (a), it is observed that at maximum DC offset i.e., at 0^0 & 180^0 inception angles, impedance estimated by FCDFT did not change instantaneously after the fault initiation. It showed inherent delay in its response. But Phaselets starts accumulating after a time delay of four samples, as the first phaselet accommodates four samples. From Fig.2 (b), phaselet based relaying shows undershoot at lower values of inception angles and overshoots at higher inception angles. Although overshoot does not create any problem to the tripping but undershoot may create false tripping. If the relay trip setting was decreased, the impedance estimated may be greater than this value but due to the undershoot behaviour exhibited, the relay may operate. There are no such problems with FCDFT based relay.

Now from Table I, it can be observed that the tripping time of Phaselet based relay is less than FCDFT relay. But considering the actual operating time i.e., including fault sensing time, FCDFT relay is faster than Phaselet based relay. In this case, for Phaselet based relay to operate faster, the relay fault sensing time should be less than the average t_{diff} .

Case B: Effect of variation of load impedance:

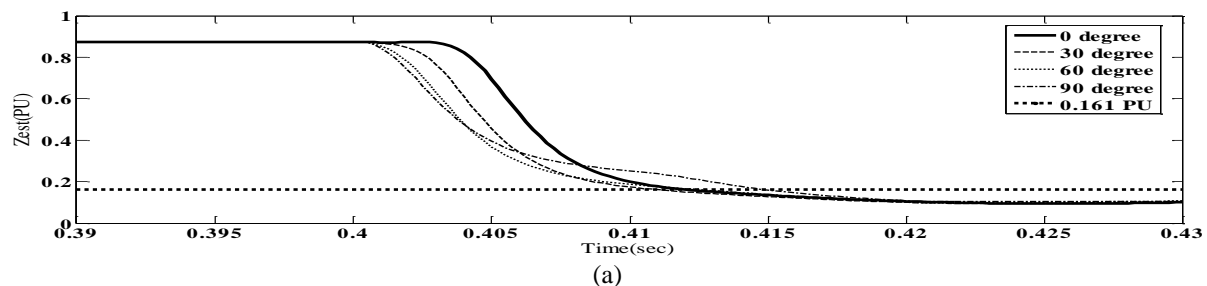
In this case, load impedance is varied from 0.1 pu to 2.0 pu. Fault impedance estimated by the FCDFT based distance relay and Phaselet based distance relay is shown in Fig.3. The details of the test results are given in Table II.

TABLE II
DETAILS OF TEST CASE-B

System Parameters: 1000 MVA, 765 kV, $Z_s=0.1$ pu, $R_F=0.01$ pu, $\Phi^0=0^0$, $R_{T/2}=0.01$ pu, $X_{T/2}=0.1$ pu.

$Z_L(pu)$	$t_{o_phaselet}(ms)$	$t_{o_DFT}(ms)$	$t'_{o_phaselet}(ms) = t_{o_phaselet} + T_{cycle}$	$t_{diff}(ms)$
0.1	0.05	9.85	20.05	9.8
0.5	0.35	11.35	20.35	11
1.0	0.45	11.85	20.45	11.4
1.5	0.45	11.95	20.45	11.5
2.0	0.45	12.05	20.45	11.6
			Average(t_{diff})	11.06

In this case, from Fig.3 (a), it is observed that the estimated impedance after the fault, at first increased and then decreased to the actual value. This hump became predominant at higher load impedances. Although this hump did not effect the estimation process but effected the operating time. Here also from Table II, the actual operating time of Phaselet based relay is higher than FCDFT based relay.



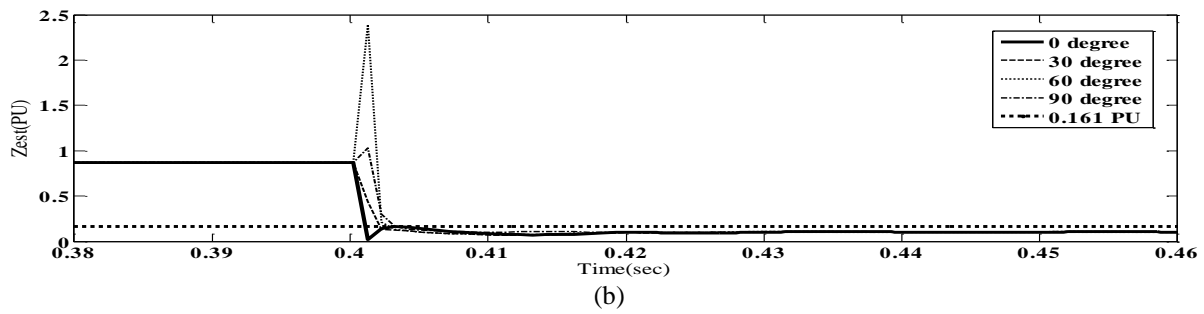


Figure 2. Effect of variation of fault inception angle: Fault impedance estimated at bus 1 by

(a): FCDFT based distance relay (b):Phaselet based distance relay

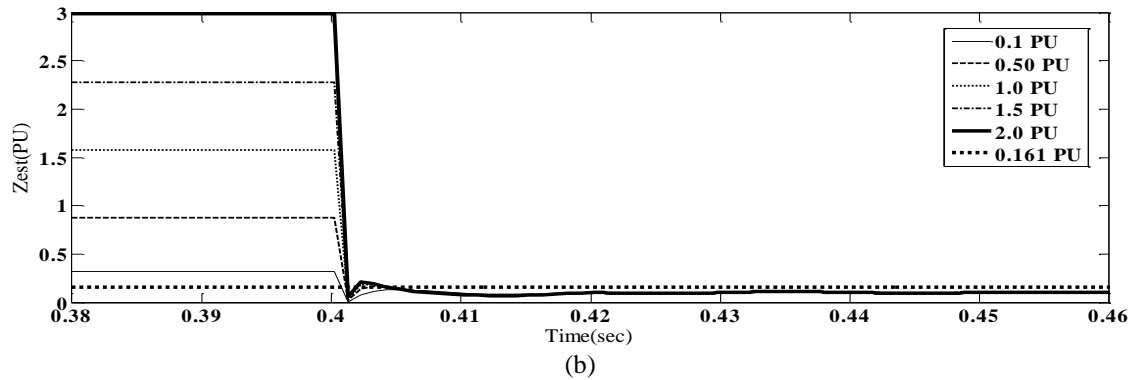
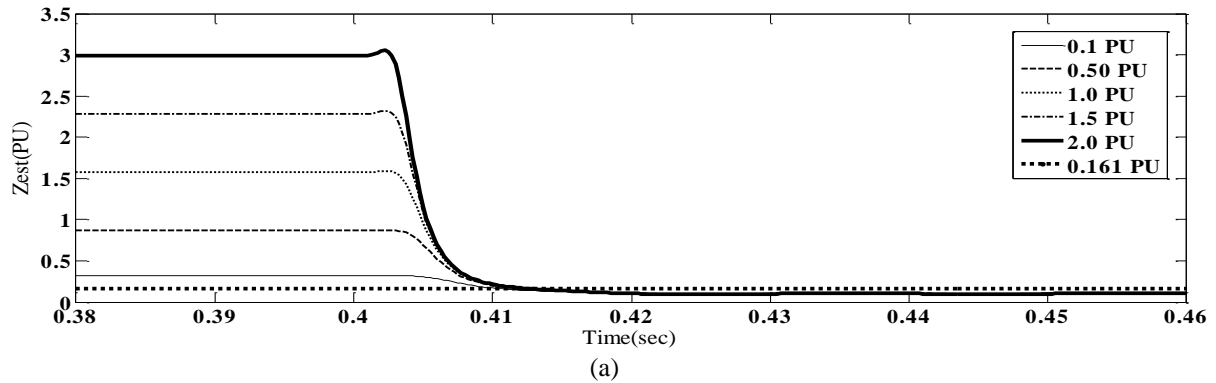
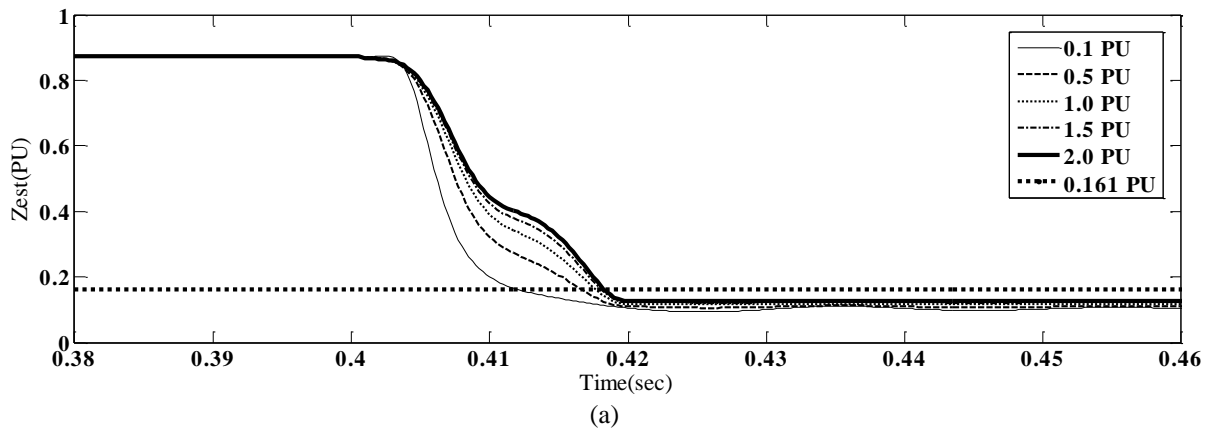


Figure 3. Effect of variation of load impedance: Fault impedance estimated at bus 1 by

(a): FCDFT based distance relay (b):Phaselet based distance relay



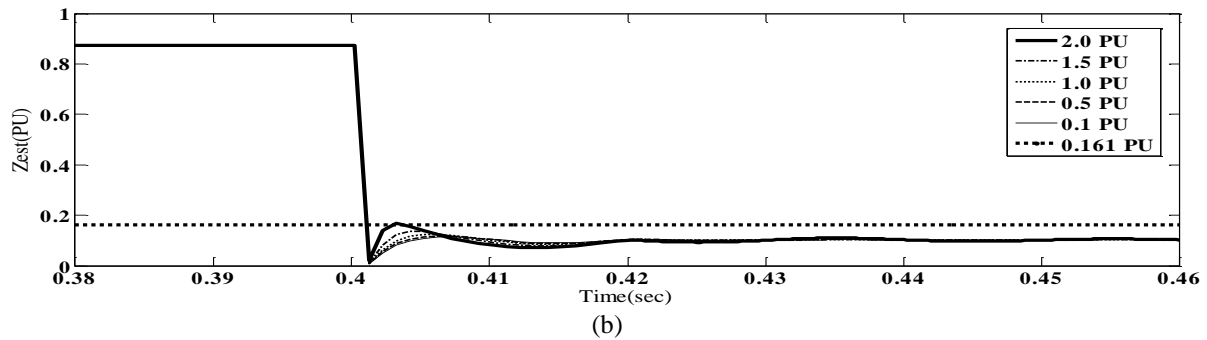


Figure 4. Effect of variation of source impedance: Fault impedance estimated at bus 1 by
(a): FCDFT based distance relay (b):Phaselet based distance relay

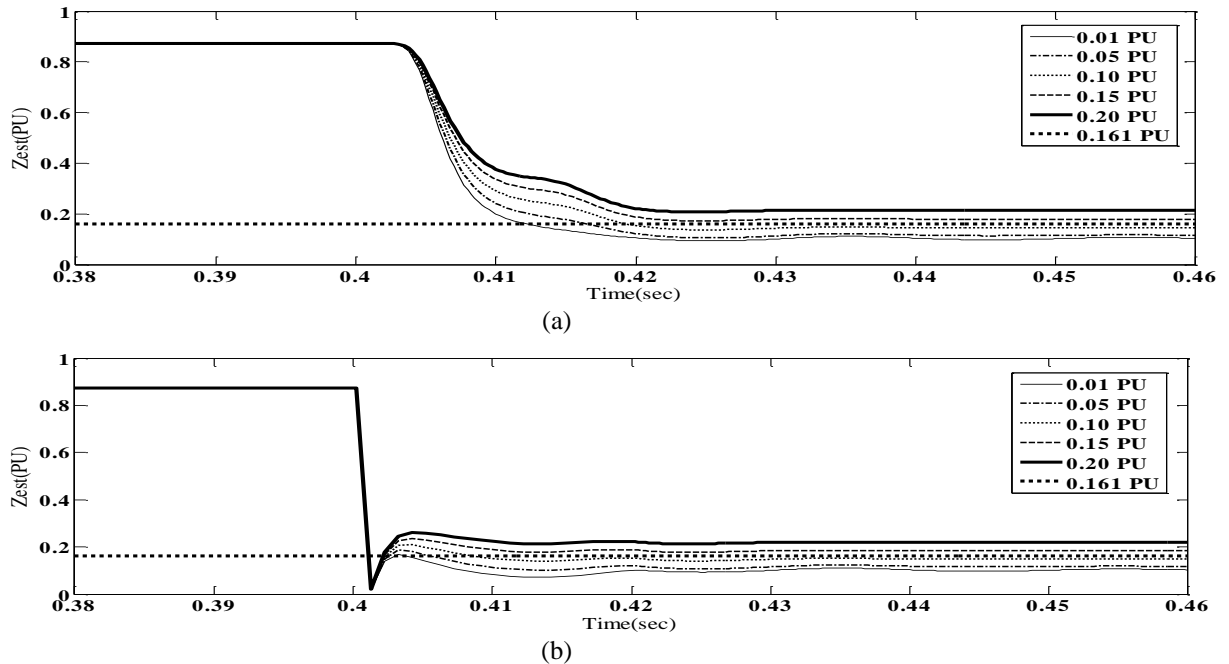


Figure 5. Effect of variation of fault resistance: Fault impedance estimated at bus 1 by
(a): FCDFT based distance relay (b):Phaselet based distance relay

Case C: Effect of variation of source impedance:

In this case, source impedance is varied from 0.1 pu to 2.0 pu. Fault impedance estimated by the FCDFT based distance relay and Phaselet based distance relay is shown in Fig.4. The details of the test results are given in Table III.

TABLE III
DETAILS OF TEST CASE-C

System Parameters: 1000 MVA, 765 kV, $Z_L=0.5$ pu, $R_F=0.01$ pu, $\Phi^0=0^0$, $R_{T/2}=0.01$ pu, $X_{T/2}=0.1$ pu.

Z_s (PU)	$t_{o_phaselet}$ (ms)	t_{o_DFT} (ms)	$t'_{o_phaselet}$ (ms)= $t_{o_phaselet}+T_{cycle}$	t_{diff} (ms)
0.1	0.35	11.35	20.35	11
0.5	0.35	15.95	20.35	15.6
1.0	0.35	16.95	20.35	16.6
1.5	0.35	17.35	20.35	17
2.0	0.35	17.55	20.35	17.2
			Average(t_{diff})	15.48

In this case also, the problems discussed in the above cases persisted. From Table III, it can be observed that the operating time of the Phaselet based relay is same irrespective of the source impedance. But, with FCDFT relay the operating time increases as the source impedance is increased.

Case D: Effect of variation of fault resistance:

In this case, fault resistance is varied from 0.1 pu to 2.0 pu. Fault impedance estimated by the FCDFT based distance relay and Phaselet based distance relay is shown in Fig.5. The details of the test results are given in Table IV.

TABLE IV
DETAILS OF TEST CASE-D

SYSTEM PARAMETERS: 1000 MVA, 765 kV, $Z_s=0.1$ PU, $Z_L=0.5$ PU, $\Phi^0=0^0$, $R_{T/2}=0.01$ PU, $X_{T/2}=0.1$ PU.

R_F (PU)	$t_{o_phaselet}$ (ms)	t_{o_DFT} (ms)	$t'_{o_phaselet}$ (ms)= $t_{o_phaselet}+T_{cycle}$	t_{diff} (ms)
0.01	0.35	11.35	20.35	11
0.05	0.35	11.35	20.35	11
0.1	0.35	18.53	20.35	18.18
0.15	0.35	No Trip		
0.2	0.35	No Trip		
			Average(t_{diff})	13.39

In this case, Phaselet based relay response is same as that in Case-C. The interesting point to note here that, at higher fault resistance, FCDFT fails to detect the fault, where as Phaselet based relay can. The operating time of the relays is same as the above all cases.

V. CONCLUSIONS

In this paper, different parameters of a single end feed test system such as fault inception angle, load impedance, source impedance and fault resistance were varied over a range. Then the performance of Full Cycle Discrete Fourier Transform (FCDFT) and Phaselet based distance relays under such scenarios is observed.

The key issues observed from the simulation studies are enumerated below:

- The rate of change of estimated impedance by a distance relay after a fault is higher by using Phaselets rather than FCDFT. This is because phaselet window does not contain pre-fault samples.
- Fault sensing time is important when considering the operating time of a phaselet based distance relay. But FCDFT based distance relay does not require any additional fault sensing time. From the details obtained in different simulated cases, fault sensing time of a phaselet based relay should atleast lower than the average t_{diff} to operate faster than FCDFT based relay.
- In a phaselet based relay, after the fault inception, first fault sensing algorithm has to sense it and initiate phaselets. Although phaselet is initiated, we obtain the initial impedance estimate only after first phaselet. In the simulated cases, it is after 1 ms.
- Under some simulated cases, phaselet based relay is showing undershoot in its impedance estimation. This would sometimes give a false trip signal to the circuit breaker. There are no such problems observed in FCDFT based relay.

From the above key issues, FCDFT remains to be prominent over the phaselets for high speed relaying in High voltage lines. If there are any advancement in faster fault detection techniques, parallel processing techniques and solid state relays, Phaselet based relaying may gain importance over other techniques.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the suggestions given by Dr. M. Ramamoorthy (Retired Director General, Central Power Research Institute, Bangalore, India) has been a great help in the carrying out this research work.

REFERENCES

1. "Synchrophasors Initiative in India," *Power System Operation Corporation*, Dec-13, 2013.
2. C. Yu, Y. Huang, J. Jiang, "A Full- and Half-Cycle DFT-based Technique for Fault Current Filtering," *IEEE Int. Conf. Ind. Technol.*, pp. 859–864, 2010.
3. H. Xue, D. Song, and R. Yang, "Consecutive DFT Method for Instantaneous Oscillating Phasor Measurement," *IEEE Trans. Power Syst.*, vol. 28, no. 4, pp. 4634–4644, 2013.
4. C. Yu, "A Discrete Fourier Transform-Based Adaptive Mimic Phasor Estimator for Distance Relaying Applications," *IEEE Trans. Power Deliv.*, vol. 21, no. 4, pp. 1836–1846, 2006.
5. D. Lee, S. Member, S. Kang, and S. Nam, "New Modified Fourier Algorithm to Eliminate the Effect of the DC offset on Phasor Estimation Using DFT," in *IEEE/PES Transmission and Distribution Conference and Exposition*, 2008, pp. 1–6.
6. S. Yu and J. Gu, "Removal of Decaying DC in Current and Voltage Signals Using a Modified Fourier Filter Algorithm," *IEEE Trans. Power Deliv.*, vol. 16, no. 3, pp. 372–379, 2001.
7. C. Chen, C. Liu, S. Member, and J. Jiang, "Application of Combined Adaptive Fourier Filtering Technique and Fault Detector to Fast Distance Protection," *IEEE Trans. Power Deliv.*, vol. 21, no. 2, pp. 619–626, 2006.
8. H. A. Darwish and M. Fikri, "Practical Considerations for Recursive DFT Implementation in Numerical Relays," *IEEE Trans. Power Deliv.*, vol. 22, no. 1, pp. 42–49, 2007.
9. C. M. Smith, A. D. Fourier, and T. Dft, "Comparing Discrete Wavelet Transform (DWT) with Discrete Fourier Transform (DFT) implemented for Digital Relays," in *Australasian Universities Power Engineering Conference*, no. 1.
10. A. H. Osman, S. Member, O. P. Malik, and L. Fellow, "Transmission Line Distance Protection Based on Wavelet Transform," *IEEE Trans. Power Deliv.*, vol. 19, no. 2, pp. 515–523, 2004.
11. J. A. De la O Serna, "Phasor estimation from phasorlets," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 1, pp. 134–143, 2005.
12. R. A. Gopinath and S. Member, "The Phaselet Transform — An Integral Redundancy Nearly Shift-Invariant Wavelet Transform," *IEEE Trans. Signal Process.*, vol. 51, no. 7, pp. 1792–1805, 2003.
13. M. Adamiak, G. Alexander, and W. Premierani, "Advancements in adaptive algorithms for secure high speed distance protection," *Twenty Third Annu. West. Prot. ...*, 1996.
14. Jin, X., Gokaraju, R., Wierckx, R. and Nayak, O., "High speed digital distance relaying scheme using FPGA and IEC 61850," *IEEE Transactions on Smart Grid*, vol. 9, no.5, pp.4383-4393, 2017.
15. Saleh, S.A., "Phaselet Transform Based Approach for Detecting Voltage Flickers Due to Distributed Generation Units," *IEEE Transactions on Industry Applications*, vol. 54, no.5, pp.5278-5292, 2017.
16. Ghalesefidi, M.M. and Ghaffarzadeh, N., "A new phaselet-based method for detecting the power swing in order to prevent the malfunction of distance relays in transmission lines," *Energy Systems*, pp.1-25, 2019
17. A. G. Phadke, J.S. Thorp, and M.G. Adamiak, "A new measurement technique for tracking voltage phasors, local system frequency and rate of change of frequency," *IEEE Trans. Power systems and App.*, Vol. PAS-102, pp. 1025-1038, 1983.
18. A. G. Phadke and J. S. Thorp, *Computer Relaying for Power Systems*. 2009.
19. Sim Power Systems 4 – Reference Manual. Natick, MA, The Math-Works, Inc., 2007.