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Stability Prediction of Soft Switched Isolated DC-DC Converter

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Abstract*: Mathematical analysis and stability prediction of soft switched isolated dc-dc converter is presented in this paper. Half bridge dc-dc converter is an attractive topology for low voltage applications due to its simplicity, lower cost, improved reliability and enhanced dynamic performance. Both power semiconductor switches of the proposed isolated converter operate asymmetrically under Zero Voltage Switching (ZVS) to achieve high efficiency and low voltage stress. Furthermore, the ringing resulted from the oscillation between the transformer leakage inductance and the junction capacitance of two switches is eliminated. Conversion efficiency is also improved by providing synchronous rectifier with very small output filter. The operating principle, state space analysis and control strategy of proposed converter is explained with small signal model. Experimental results are presented to explain the zero voltage switching capability and stability features of proposed converter.

Keywords*: Half bridge converter, State space modelling, Pulse Width Modulation (PWM), Small signal model, Zero Voltage Switching (ZVS).

I. INTRODUCTION

Portable products such as personal communicators, com-links, displays and digital assistants has demanded continuous improvements in dc-dc converter topology for providing constant dc voltage in order to increase their battery life time and enable compact systems. Soft switching is easily obtained in half bridge circuits and it reduces the switching loss. Soft switching techniques reduce the electromagnetic interference and achieve higher power conversion density of converter circuits.

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Condition of stability using different methods is presented in [1] and it reveals the results in terms of error and peak overshoot values. Converter performance under various modes of operation during disturbances is presented in [2].

Power electronic converter controlled using digital techniques and its modes of operation under various disturbances and its modeling is explained in [3]. Low power converters performance analysis is presented in [4] with different types of controllers for various types of disturbances. Importance of clamp circuits in stability part of power converter with zero losses during switching operation is explained in [5]. Importance of segmentation for converter stability optimization with increased performance is shown in [6, 7]. Concept based on/off control with ideal characteristics is proved in [8]. Intelligent controllers for prediction of stability is explained in [9-11] with its rapid accelerating characteristics. In this proposed converter all the above said features are analyzed using state space model and the converters stability is predicted using frequency response plots.

II. PROPOSED CONVERTER CIRCUIT

The drawback of conventional converter circuit includes restricted frequency range and more stress on operating switches. It affects the operating condition and the stability of power converter. To overcome the above said drawbacks of the conventional converter circuit soft switched asymmetric converter is proposed in this paper and it is shown in Figure 1.

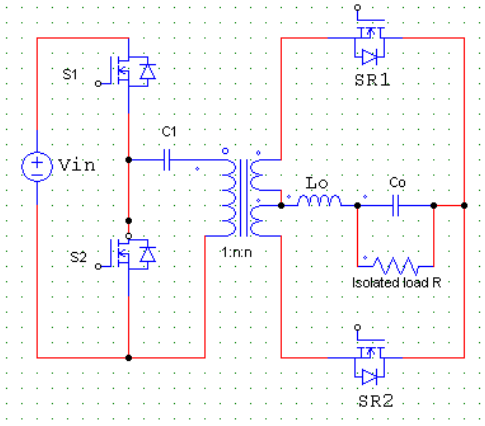

Figure 1 Proposed converter circuit

In the converter circuit the switches are turn on/off asymmetrically to create zero voltage between the transitions. The capacitor is introduced to reduce the voltage ripples. MOSFET is preferred for this because its a good switching device due to its low capacitance and increased transconductance. Driving signals are generated according to its voltage polarity.

The converter ensures soft switching in all the power switches. The derivation of small signal model is derived as follows.

By considering the magnetic inductance and duty cycles the capacitor voltage is derived as

$V_{C1} = d_1 V_{in}$ (1)

The above equation is based on L_m as

$(V_{in} – V_{C1}) (L_m / (L_m + L_r)) d_1 T_s – V_{C1} (d_2) T_s = 0$ (2)

Voltage transfer ratio can be obtained from equation (1) as

$((L_m (d_2) V_d) / (L_m + L_r)) d_1 T_s = ((1 / n) V_o d_1 T_s) + ((L_m d_1 V_{in}) / (L_m + L_r) d_2 T_s)$ (3)

Relation between the duty cycles are $d_1 = 1 - d_2$ (4)

Using Equation 1-4 voltage transfer function is derived as

$V_o / V_{in} = (L_m / (L_m + L_r)) n d_1 \cong n d_1$ (5)

From the derived transfer function equation 5, the small signal model is derived in the next section.

III SMALL SIGNAL MODELLING

The step by step procedure for obtaining small signal model is explained as follows.

Step 1: The modes of converter operation is identified.

Step 2: Select the state variables of the switching converter. Normally current through the inductor and voltage across capacitor is selected as state variables.

Step 3: Write the state equations for switched converter modes using Kirchhoff's current and voltage laws.

Step 4: Perform state space averaging using the duty cycle as a weighting factor and identify the state matrices. Combine the state matrices in to a single averaged matrix using the following equation,

$\dot{x} = [A_1 d + A_2 (1 – d)] x + [B_1 d + B_2 (1 – d)]u$ (6)

The above equation results in a matrix A and B.

Step 5: Substitute the component values in the matrix and the transfer function is obtained using the matrices A and B with the help of the MATLAB. From the obtained transfer function the frequency response plots i.e. bode plot and root locus plot are drawn using MATLAB to identify the converter stability.

For state variables identified for the proposed converters are C_1, L_m, L_o and C_o

Condition 1: In this mode, S_1 and SR_2 is ON. The derived state equations for the identified four state variables are

$$
\begin{aligned}
C_1 \, dV_{C1} / dt &= (- V_{C1} / R) + i_{Lm} - n i_{Lo} \\
L_m \, di_{Lm} / dt &= - V_{C1} + V_{in} \, d_1 \\
L_o \, di_{Lo} / dt &= n V_{C1} - V_o + n V_{in} \, d_1 \\
C_o \, dV_o / dt &= i_{Lo} - (V_o / R)
\end{aligned}
\quad (7)
$$

Equation (7) can be rearranged as

$$
\begin{aligned}
dV_{C1} / dt &= (- V_{C1} / R \, C_1) + (i_{Lm} / C_1) - (n i_{Lo} / C_1) \\
di_{Lm} / dt &= (- V_{C1} / L_m) + (V_{in} \, d_1 / L_m) \\
di_{Lo} / dt &= (n V_{C1} / L_o) - (V_o / L_o) + (n V_{in} \, d_1 / L_o) \\
dV_o / dt &= (i_{Lo} / C_o) - (V_o / R \, C_o)
\end{aligned}
\quad (8)
$$

The state space model takes the following form:

$dx / dt = AX + BU$ (9)

where X is a matrix containing the state variables V_{C1} , i_{Lm} , i_{Lo} , and V_o , U contains control inputs.

A_1 and B_1 values are obtained after rearranging equation (9).

$$
A_1 = \begin{pmatrix} \frac{-1}{R_{C1}} & \frac{1}{C_1} & \frac{-n}{C_1} & 0 \\ \frac{-1}{L_m} & 0 & 0 & 0 \\ \frac{n}{L_0} & 0 & 0 & \frac{-1}{L_0} \\ 0 & 0 & \frac{1}{C_0} & \frac{-1}{R_{C0}} \end{pmatrix} \qquad X = \begin{pmatrix} V_{c1} \\ i_{lm} \\ i_{lo} \\ V_0 \end{pmatrix}
$$

$$
B_1 = \begin{pmatrix} 0 & 0 \\ \frac{V_{in}}{L_m} & 0 \\ \frac{n V_{in}}{L_0} & 0 \\ 0 & 0 \end{pmatrix} \quad U = \begin{pmatrix} d_1 \\ d_2 \end{pmatrix} \qquad (10)
$$

Condition 2: In this mode, S_2 and SR_1 is gated ON. The transformer is energized through the input voltage and the inductor connected in load side charging at varying rates. For this condition the obtained state equations are

$$
\begin{aligned}
C_1 \, dV_{C1} / dt &= (- V_{C1} / R) + i_{Lm} + n i_{Lo} \\
L_m \, di_{Lm} / dt &= V_{in} \, d_2 - V_{C1} \\
L_o \, di_{Lo} / dt &= n V_{C1} - V_o + n V_{in} d_2 \\
C_o \, dV_o / dt &= i_{Lo} - (V_o / R)
\end{aligned}
\quad (11)
$$

Equation (11) can be rearranged as

$$
\begin{aligned}
dV_{C1} / dt &= (- V_{C1} / R \, C_1) + (i_{Lm} / C_1) + (n i_{Lo} / C_1) \\
di_{Lm} / dt &= (V_{in} \, d_2 / L_m) - (V_{C1} / L_m) \\
di_{Lo} / dt &= (n V_{C1} / L_o) - (V_o / L_o) + (n V_{in} d_2 / L_o) \\
dV_o / dt &= (i_{Lo} / C_o) - (V_o / R \, C_o)
\end{aligned}
\quad (12)
$$

Matrices A_2 and B_2 are obtained from the equation (12).

$$
A_2 = \begin{pmatrix} \frac{-1}{R_{C1}} & \frac{1}{C_1} & \frac{+n}{C_1} & 0 \\ \frac{-1}{L_m} & 0 & 0 & 0 \\ \frac{n}{L_0} & 0 & 0 & \frac{-1}{L_0} \\ 0 & 0 & \frac{1}{C_0} & \frac{-1}{R_{C0}} \end{pmatrix} \qquad X = \begin{pmatrix} V_{c1} \\ i_{lm} \\ i_{lo} \\ V_0 \end{pmatrix}
$$

$$
B_2 = \begin{pmatrix} 0 & 0 \\ 0 & \frac{V_{in}}{L_m} \\ 0 & \frac{n V_{in}}{L_0} \\ 0 & 0 \end{pmatrix}
$$

$$U = \begin{pmatrix} d_1 \\ d_2 \end{pmatrix} \quad (13)$$

Averaged single matrix is obtained using the following equation (14).

$$\dot{x} = [\, A_1 d + A_2 (1 - d)\,] x + [\, B_1 d + B_2 (1 - d)\,]u \quad (14)$$

The feedback control loops of output voltage regulation and input voltage regulation. In this paper two control loops are used for converter called Input and output Voltage Regulation as shown in figure 2. Input voltage regulation sets the reference value based on optimized voltage value and Output regulation is a voltage control loop and the control input is d_1. A, B, X and U matrices are obtained from the equation (14).

$$A = \begin{pmatrix} \frac{-1}{R_{C1}} & \frac{1}{C_1} & \frac{-n}{C_1} & 0 \\ \frac{-1}{L_m} & 0 & 0 & 0 \\ \frac{n}{L_0} & 0 & 0 & \frac{-1}{L_0} \\ 0 & 0 & \frac{1}{C_0} & \frac{-1}{R_{C0}} \end{pmatrix} \qquad X = \begin{pmatrix} V_{c1} \\ i_{lm} \\ i_{lo} \\ V_0 \end{pmatrix}$$

$$B = \begin{pmatrix} 0 & 0 \\ \frac{V_{in}}{L_m} & \frac{V_{in}}{L_m} \\ \frac{nV_{in}}{L_0} & \frac{nV_{in}}{L_0} \\ 0 & 0 \end{pmatrix} \quad U = \begin{pmatrix} d_1 \\ d_2 \end{pmatrix} \quad (15)$$

Pulse Width Modulator generates the duty cycle d_1 is for the switches S_1, SR_2 and duty cycle d_2 is for S_2 and SR_1. Because of the existence of interacting control loops the model is designed as shown in figure 2 for the proposed converter.

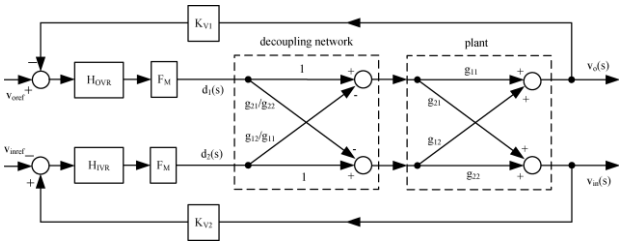

Figure 2 Converters Model

In the model G(s) (4, 2) represents the fourth state variable V_o and the second control variable d_2, which equals to transfer function of V_o / d_2.

$G(s) = (sI - A)^{-1} B$

$V_o / d_1 = g_{11} = G(s)\ (4,1)$ $V_{in} / d_1 = g_{21} = G(s)\ (1,1)$

$V_o / d_2 = g_{12} = G(s)\ (4,2)$ $V_{in} / d_2 = g_{22} = G(s)\ (1,2)$ (16)

Pulse Width Modulator gain F_M is calculated using the following equation,

$$F_M = \frac{2^M f_s}{f_{PWMClock}} \quad (17)$$

Where, $f_{PWMClock}$ is the clock frequency of the Pulse Width Modulator i.e. the rate at which the pulses are generated. The K_{V1} and K_{V2} are the feedback path gains. The G^* decoupling network is described as

$$G^* = \begin{pmatrix} 1 & -\frac{g_{12}}{g_{11}} \\ -\frac{g_{21}}{g_{22}} & 1 \end{pmatrix} \quad (18)$$

The Output voltage regulation is designed using the following transfer function

$V_o(s) / d_2(s) = g_{11} - g_{12} \times g_{21} / g_{22}$. (19)

While substituting the component values of the proposed converter in the derived small signal matrices, $g_{11}, g_{12}, g_{21}, g_{22}$ are obtained and from equation (15) and the output voltage regulation mode transfer function H_{OVR} is

$H_{OVR} = 89(s/2\pi\times300+1)$
$(s/2\pi\times600+1)/(s\times(s/2\pi\times4280+1)\times(s/2\pi\times4280+1))$ (20)

The Input Voltage Regulation (IVR) loop design utilizes the following loop equation from the derived small signal model

$v_{in}(s) / d_1(s) = g_{22} - g_{12} \times g_{21} / g_{11}$ (21)

The compensator of H_{IVR} used is as follows:

$H_{IVR} = 0.7(s/2\pi\times941+1)(s/2\pi\times941+1)/(s\times(s/2\pi\times199+1)$
$/(s/2\pi\times300+1))$ (22)

IV. EXPERIMENTAL RESULTS

A 100 W asymmetric half bridge converter is tested to verify the small signal model. There is a small time delay between S_1 and S_2 is created to solve the problem of cross conduction. Figures 3 and 4 show the experimental waveforms of the voltage between drain and source of MSOFET (in green line) and the gate pulses are shown in blue line. In figure 3 and 4 the green line that is the voltage across switch reaches zero before the gate pulses represented in blue line) are applied to the switches to turn on. Hence, soft switching is achieved and the losses are reduced.

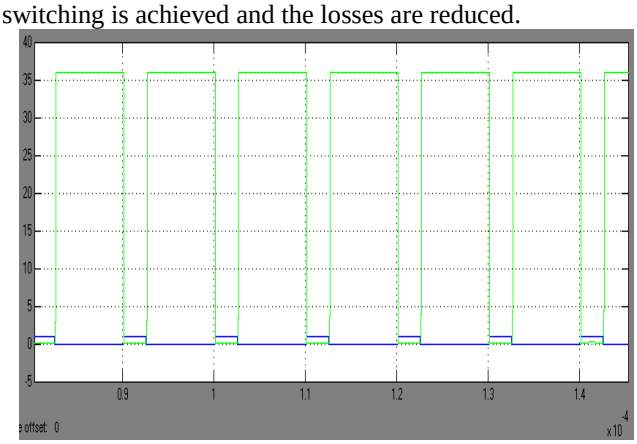

Figure 3 ZVS achievement in S_1 (Green line represents voltage across drain-source terminals of S_1 and blue line represents gate pulses to turn on S_1)

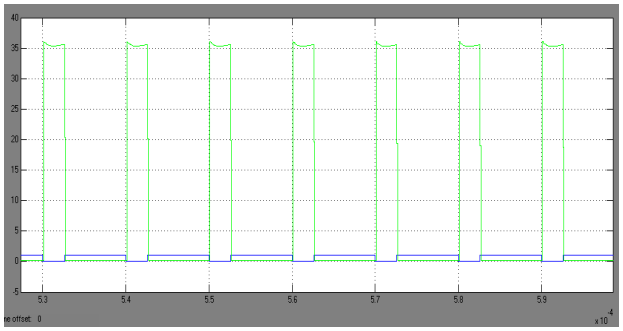

Figure 4 ZVS condition for the switch S_2 (Green line represents voltage across drain-source terminals of S_2 and blue line represents gate pulses to turn on S_2)

The Bode plot and Root locus plot for input voltage regulation mode and output voltage regulation mode was plotted to identify the stability of the system and is shown in figures 5 - 8.

The frequency domain specifications; phase margin and gain margin is obtained from the bode plot of input voltage and output voltage regulation modes. According to the stability criteria the stable system should have positive values of phase and gain margins. The obtained margin values from bode plots of input and output voltage regulations are positive thereby it satisfies the stability criteria. Then the next frequency response plot called root locus is drawn for confirming the stability of the proposed system. For stable system all the poles should lie inside the unit circle. In the obtained root locus plot all the closed loop poles lie within the unit circle for input and output voltage regulation. So the designed system satisfies the stability criteria of root locus also.

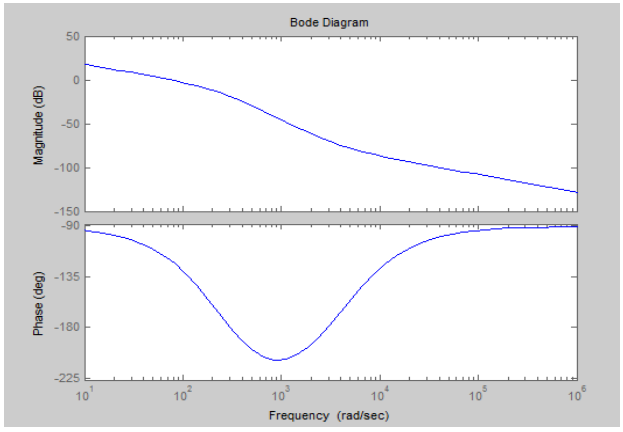

Figure 5 Bode plot for input voltage regulation (phase margin = 45.21 degrees, gain margin = 89.96 dB)

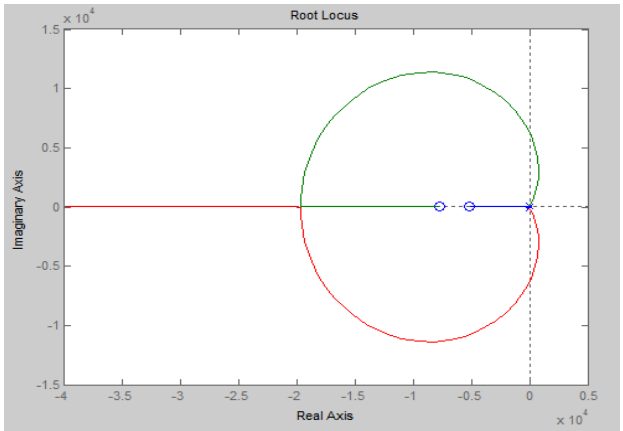

Figure 6 Root locus plot for input voltage regulation

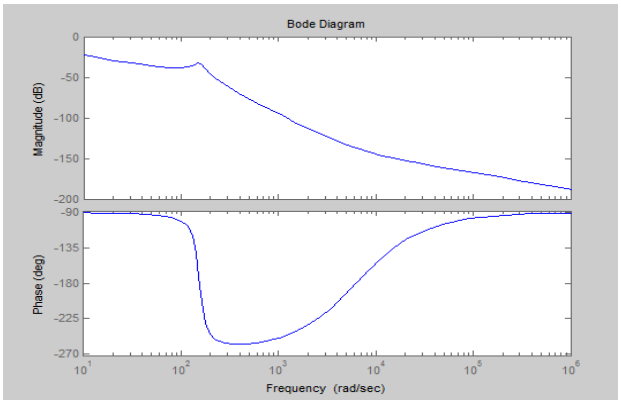

Figure 7 Bode plot for input voltage regulation (phase margin = 9.14 degrees, gain margin = 59.89 dB)

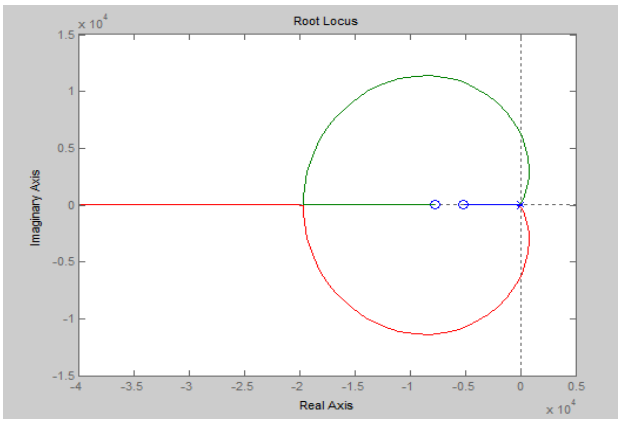

Figure 8 Root locus plot for output voltage regulation

Proposed converters output voltage and current waveforms are shown in figure 9. From figure 9 it is seen that within a short time voltage and current reaches its steady state condition. So the converter has improved dynamic response. The efficiency is calculated by dividing the output power of the converter to input power under different load conditions. The measured efficiency is presented in Table-1. Table-1shows proposed converters efficiency is high, because of its low forward voltage drop. All the switches are operated in ZVS condition, hence the efficiency is increased.

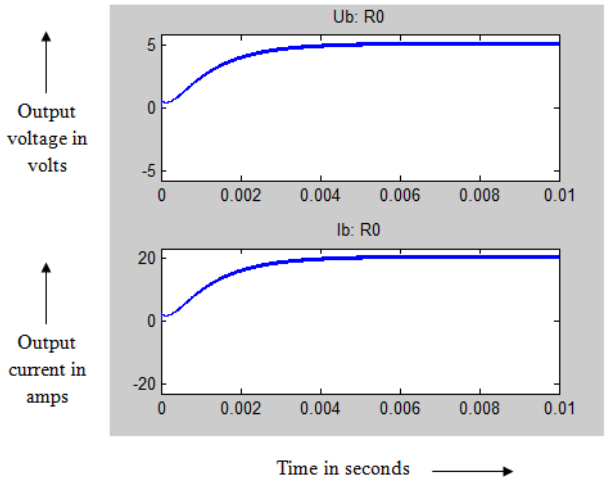

Figure 9 Output voltage and current waveforms

Table 1: Comparison between percentage efficiency of converters

Output power in watts	Conventional converter efficiency (%)	Proposed converter with synchronous rectifier efficiency (%)
3	79	80
10	81	86
20	83	87
30	85	88
40	86	88
50	86	89
60	87	90
70	88	90
80	89	91
90	90	92
100	90	92

V. CONCLUSION

The mathematical analysis and stability identification of the DC-DC converter is implemented for low voltage applications. The small signal model of the converter is obtained from its switching modes. Decoupling network is designed to resolve the interdependence problem. The converter is decoupled and analyzed for each operating modes separately. Control loops transfer functions are derived. The converters stability is proved through Frequency response plots with soft switching. So the converter has reduced losses and improved efficiency. Experimental results reveal that the designed converter will be suitable for low voltage compact applications even during the operating conditions having high disturbances.

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