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# Noise Performance Improvement In Future IC Integration using Perylene-N As Dielectric Material

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*Abstract*: ***Ever-growing consumer demand for smaller and faster devices opens up to think the semiconductor industries about another direction of improvement during IC integration as long run metal wires not only reduces the form factor of the system but also decreases the system performance by creating RC delay which in turn reduces the bandwidth during communication. In order to improve the system performance the devices must be interconnected vertically known as 3D IC integration. In this emerging technique, different modules are mounted on different layers with Si substrate and these layers are placed one on other. TSV's (Through Silicon Via or Through Substrate Via) are the basic building blocks of the 3D ICs which are playing an important role to create high performance electrical path between thin IC chips. TSV's carries the entire electrical signal between the layers of 3D structure. Major drawback is poor electrical signaling due to the noise coupling between signal carrying TSV's(aggressive TSV's) and ground TSV's(victim TSV's).Therefore there is a strong need of isolation between Si substrate and TSV's with proper liner materials and structures. Perylene-N is one of the most promising dielectric material for less area consumption and less power consumption. In this paper, we compared the results for Perylene-N and conventional SiO2 liner for ETSV's. The performance of this structure is analyzed and verified under different parameters to reduce the noise coupling. In this structure dielectric-metal-dielectric are arranged around the Copper TSV. The achieved result shows that more noise coupling is reduced by using Perylene-N as dielectric material as compared with conventional SiO2. Furthermore, Perylene-N shows 33 dB improvements in noise coupling performance at THz frequencies which is verified and validated as well in this work.***

*Keywords* : ***3D IC, ETSV, Perylene-N, Noise Coupling.***

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## I. INTRODUCTION

Three Dimensional IC (3D IC) is an emerging technology which can be successfully overcome the challenges faced by 2D IC integration. 3D IC integration can be achieved by several thin IC chips are electrically interconnected using vertical bonding [1] –

[5] and TSV's. Now-a-days TSV's plays a major role in many semiconductor industries for the integration of 3D IC. TSV's are classified into two major types i.e., ETSV (Electrical TSV) which carries electric signal and TTSV (Thermal mitigation TSV) which carries thermal signal. In spite of several advantages of 3D IC with TSV's noise coupling is one of the most significant consideration for the critical design circuitry. The major obstruction of TSV's are electrical signal is poor due to the noise coupling between signal carrying TSV's (aggressive TSV) and ground TSV's (victim TSV) through Si substrate [6]. Some of the researchers have reported few improvements in noise coupling using guard ring structure around the TSVs, and trench shaped TSVs [7] – [9]. Guard ring structure is quiet impressive but additional structure require for improvement in noise coupling. Also, some of the researchers have employed stacked liner structure and different liner materials in order to improve the noise coupling [10], [11].

In our present work, we have introduced Perylene-N as a better choice of dielectric material through ETSV. As Perylene-N is having highest penetrating ability then Perylene-C and Perylene-D and also it is thermally stable up to 400 degree C. The major properties of Perylene-N are low dielectric constant and it is independent of frequency, high dielectric strength, high mechanical durability and excellent electrical insulation. We analyzed the performance of noise coupling using two different liners structures, one is single liner structure the liner is totally filled with different dielectric materials (Perylene-N and SiO2), and the other structure is stacked liner structure it can be defined as dielectric-metal-dielectric (Perylene-N-Cu-Perylene-N) and (SiO2-Cu-SiO2).

In this paper we have chosen Perylene-N is better as compared to SiO2 because there are some properties like dielectric constant of SiO2 is 3.9 but for Perylene-N, dielectric constant is 2.4. The volume resistivity of SiO2 is >1018 but for Perylene-N is 1.4x1017.

The melting point of SiO2 is >1500 but for Perylene-N is 420. The linear coefficient of thermal expansion is 0.5 but for Perylene-N it has 69. Coefficient of thermal conductivity for SiO2 is 1.4 but for Perylene-N it has 0.126.

## II. MODEL DESCRIPTION

The analyzed structure is done by two different ways one is potential variation analysis and other is frequency variation analysis.

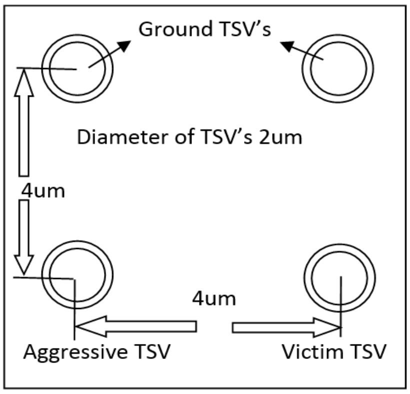


**Fig.1. Top view of TSV model**

Fig.1 above shows the top view of TSV structure. In this each TSV diameter is of 2um with a liner thickness of 0.15um and height of 8um and TSV to TSV are separated with pitch of 2um. The distance between two TSV's is 4um.

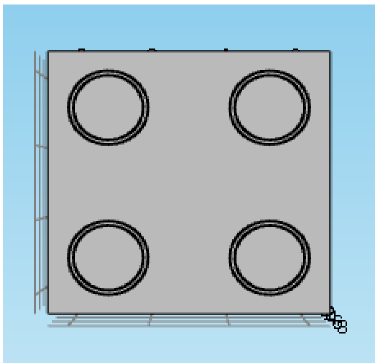

**Fig.2. TSV model using stacked layers of liners.**

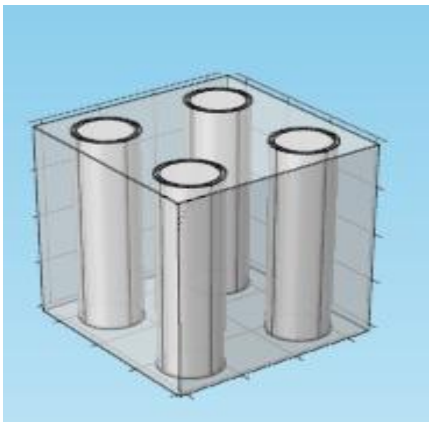

**Fig.3. Aggressive and Victim TSV are in 3D model.**

From the figures above shows that one TSV acts as an aggressive TSV and other TSV acts as a victim TSV. We are analyzing the potential variation by applying 1V electrical potential to the aggressive TSV which will affect victim TSV and also by analyzing the noise performance at high frequency i.e., 1THz.

## III. NOISE COUPLING ANALYSIS

Noise coupling is analyzed for the single liner and stacked layers of liner structure around the TSV by applying 1V electrical potential to the aggressive TSV and verifying the potential variation across the silicon substrate and victim TSV.

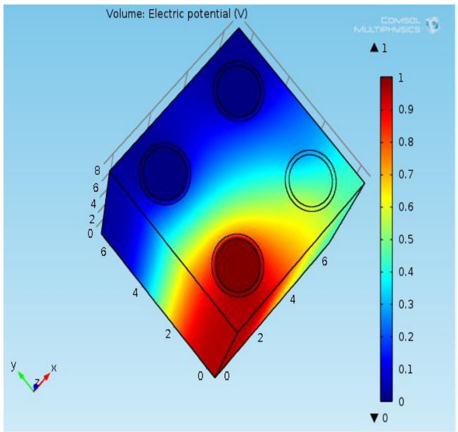


**Fig.4. Potential variation between aggressive and victim TSV's by using Perylene-N as single liner structure of 3D view.**

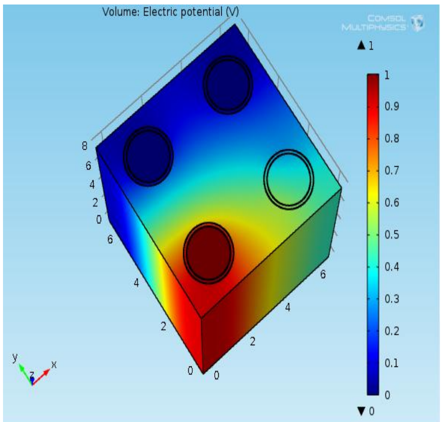


**Fig.5. Potential variation between aggressive and victim TSV's by using Perylene-N as stacked layers of liner structure of 3D view.**

Fig.6 and Fig.7 shows that noise coupling is improved by using Perylene-N as single liner around the TSV as compared to single SiO2 liner.

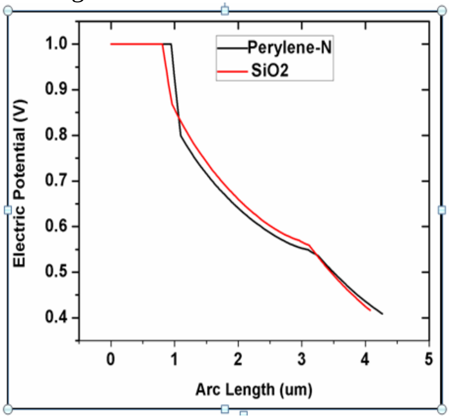


Fig.6.Comparison of potential variation between aggressive and victim TSV's by using different dielectric materials around the TSV as a single liner structure.

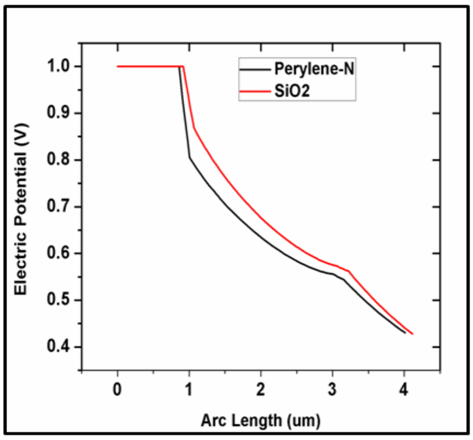


**Fig.7.Comparison of potential variation between aggressive and victim TSV's by using different dielectric materials around the TSV as a stacked layers of liner structure.**

## IV. HIGH FREQUENCY NOISE COUPLING ANALYSIS

The analysis of noise coupling at high frequency is compared with dielectric materials like Perylene-N and SiO2 .It is noticeable from Fig.8 and Fig.9 are by using Perylene-N as dielectric material at high frequency i.e., 1THz shows the better results as compared to $SiO_2$.

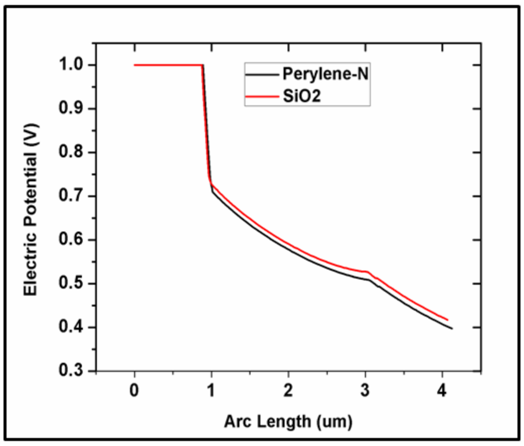


**Fig.8. Noise coupling analysis at high frequency of Perylene-N and $SiO_2$ as single liner structure around TSV with 1THz.**

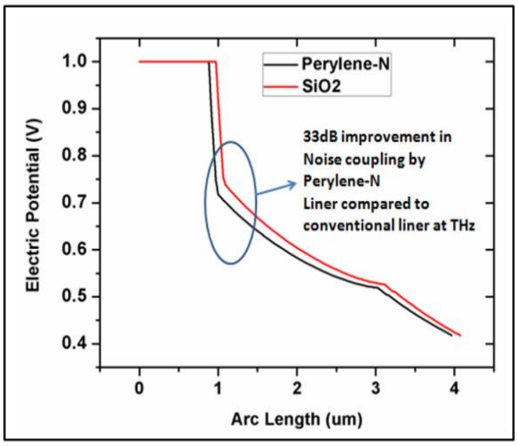


**Fig.9. Noise coupling analysis at high frequency of Perylene-N and SiO2 as stacked layers of liner structure around TSV with 1THz.**

## V. CONCLUSION

In 3D IC technology the noise coupling between aggressive TSV and victim TSV become a major problem. So in order to reduce the effect of noise coupling we introduced Perylene-N liner structure around the TSV's and also demonstrated the noise coupling performance at high frequencies i.e.,1THz. The significant improvement in noise coupling using liners made up of Perylene-N are compared to the conventional SiO2 liner in case of both proposed TSV structures i.e., single liner and multi-layer liner structures. Perylene-N offers improved noise coupling performance than conventional SiO2 as liner in both proposed TSV structures at high frequencies. Hence Perylene-N can be an ideal contender as a liner material for via last process of TSV fabrication. Furthermore, it shows excellent noise coupling performance even at higher frequencies i.e., 1THz.

## REFERENCES

1. Asisa Kumar Panigrahi, Tamal Ghosh, Siva Rama Krishna Vanjari, and Shiv Govind Singh, "Oxidation resistive, CMOS compatible Copper based Alloy ultrathin films as a superior passivation mechanism for achieving 150˚C Cu-Cu wafer on wafer thermocompression bonding, " IEEE Transactions on Electron Devices, 64(3), pp.1239-1245, 2017.
2. Asisa Kumar Panigrahi, Tamal Ghosh, Siva Rama Krishna Vanjari, and Shiv Govind Singh, "Demonstration of Sub 150 ˚C Cu-Cu thermocompression bonding for 3D IC applications, utilizing an ultra-thin layer of Manganin alloy as an effective surface passivation layer", Materials Letters 194, pp.86-89, 2017
3. Asisa Kumar Panigrahi, C. Hemanth Kumar, Satish Bonam, Tamal Ghosh, Siva Rama Krishna Vanjari, and Shiv Govind Singh, "Optimized ultra-thin manganin alloy passivated fine-pitch damascene compatible bump-less Cu–Cu bonding at sub 200 °C for three-dimensional Integration applications," Japanese Journal of Applied Physics 57, 02BC04, 2018.
4. Asisa Kumar Panigrahi, Satish Bonam, Tamal Ghosh, Shiv Govind Singh, and Siva Rama Krishna Vanjari, "Ultra-thin Ti passivation mediated breakthrough in high quality Cu-Cu bonding at low temperature and pressure," Materials Letters 169, pp. 269-272, 2016.
5. Asisa Kumar Panigrahi, Tamal Ghosh, C.Hemanth Kumar, Shiv Govind Singh, and Siva Rama Krishna Vanjari, "Direct, CMOS In-line Process flow compatible, Sub 100˚C Cu-Cu thermocompression bonding using Stress Engineering", Electronic Materials Letters 14, no. 3, pp. 328-335, 2018.
6. Joohee Kim, Jonghyun Cho, and Joungho Kim Terahertz Interconnection and Package Laboratory, KAIST, Daejeon, Korea "TSV Modeling and Noise Coupling in 3D IC", 3rd Electronics System Integration Technology Conference ESTC, Sep.2010.
7. Jonghyun Cho, Kihyun Yoon, Jun So Pak, Joohee Kim, Junho Lee, Hyungdong Lee, Kunwoo Park and Joungoho Kim, Terahertz Interconnection and Package Laboratory, KAIST, Daejeon, Korea "Guard Ring Effect for Through Silicon Via (TSV) Noise Coupling Reduction",2010 IEEE CPMT Symposium Japan,Aug.2010.
8. Shinichiro Uemura, Yukio Hiraoka, Takayuki Kai and Shiro Dosho StrATEGIC Semiconductor Development Center, Panasonic Corp. 3-1-1 Yagumo-naka-machi, Moriguchi,Osaka,Japan Production Engineering Laboratory, Panasonic Corp. "Isolation Techniques against Substrate Noise Coupling Utilizing Through Silicon Via(TSV) for RF/Mixed-Signal SoCs" IEEE Journal of Solid-State Circuits ( Volume: 47 , Issue: 4 , April 2012 ) Feb. 2012.
9. R Ranga Reddy, Sugandh Tanna,Dr. Shiv Govind Singh and Om Krishna Singh, "TSV Noise Coupling in 3D IC using Guard Ring", 2015 International 3D Systems Integration Conference (3DIC), sep.2015.
10. Suraj Patil, Asisa Kumar Panigrahi, Satish Bonam, C. Hemanth Kumar, Om Krishan Singh, and Shiv Govind Singh, Department of Electrical Engineering, "Improved noise coupling performance using optimized Teflon liner with different TSV structures for 3D IC integration". 2016 IEEE International 3D Systems Integration Conference (3DIC).Nov.2016.

11. C.Hemanth Kumar, Asisa Kumar Panigrahi, Om Krishan Singh, and Shiv Govind Singh, "Noise performance improvement through optimized stacked layer of liner structure around the TSV in 3D IC". 2016 IEEE International 3D Systems Integration Conference (3DIC) Nov.2016.

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