Approximate Speculative Adder for Low Power VLSI Architectures

C. Srinivasa Murthy, K. Tarakeswara Rao, K Sridevi

Abstract*: Approximate Speculative Adder (ASA) for low energy dissipation is proposed in this paper. To enhance the speed of operation pipelining technique is been employed and also to lower the critical path delay utilization of logic gates are also reduced. The structure employs carry look ahead logic for adder implementation. Different configurations have been examined for area and speed. The prime aim lies for lowering the dissipative energy. Also clock skew technique is employed to save the dynamic power consumption. The structure is been analyzed with FPGA and also realized with ASIC. Analysis of results states about the performance of ASA can operate at higher speed than the existing structures. The structure absorbs 5.109 mm^2 of chip space. The proposed Approximate Speculative Adder consumes 52.75% of power

***Keywords:** Approximate speculative adder, carry look ahead adder, pipelining.*

I. INTRODUCTION

Device miniaturization is been a continuous process facilitating the enhancement in digital circuits. Technology scaling demands lower energy consumption, lesser area and high speed for modern digital devices. Addition is an important operation in most of the digital circuits and therefore adders with optimization in performance and parameters are required. Conventional adders dissipate good amount of power and area hence approximate adders are trending in to VLSI design. Approximate adders are profoundly attractive in the recent scaling devices, despite the fact that power and silicon space are similarly imperative. Along these lines the plan of exceptionally upgraded adders as far as speed assumes noteworthy parameter in the present period and consequently this paper centers the same plan. With passable debasement in exactness and execution, it is attainable to consider fast, low power and space utilizing approximate circuit strategy. Precision of such circuits may be sacrificed to improve the features such as speed and space of silicon and power. Thus known as approximate speculative adder (ASA). Subsequently ASA structure is been employed with FPGA using of 8, 16 and 32 bit models. Along these lines, clock for different phases of the pipelined ASA has been applied to mitigate the power utilization. ASIC design of the proposed ASA has been performed and is contrasted with the available ASA technology.

II. PROPOSED WORK

Schematic diagram is shown in fig.1 for the proposed structure of ASA for m-bit and the m-bits are divided into four equal segments i.e. n = 4. And each of these segments is applied as operand to the n-bit adder. Unlike traditional ASA, the adder unit been supplanted with 4-block carry look ahead adder to further improve the speed. Detailed Illustration of schematic is followed below.

I) Speculator and Adder Blocks: Consider X = {X0, X1,..,Xn−1} and Y = {Y0, Y1,..,Yn−1}; while, sum S = {S0, S1,..,Sn−1}, Cin carry input and $Cout$ carry output. Structural level circuit configuration is shown in Fig.1 (b). Approximation of the output carry for each 4-bit adder block is carried out. Approximation is accomplished for ' Most Significant Bits (MSB) of each block where it is approximate size of block, (i.e., MSB < n ≤4). So the input for these blocks can be either 0 or 1 which represents an error occurred.'0' represents positive and '1' indicates negative error. The output carry Cso from each block is fed as an input carry to succeeding adder blocks. Hence adders need not wait for carry. Rather, all such adders perform concurrent additions on receiving the carry from speculator blocks. Carry of Speculator block is computed as below.

$$Pi = Ai \oplus Bi;$$
$$Gi = Ai \cdot Bi;$$
$$Ci{+}1 = Gi + (Pi \cdot Ci); \rightarrow (1)$$

Where (i+1)th carry bit is computed by making use of the propagate (Pi), generate (Gi) and carry (Ci) of ith bit.

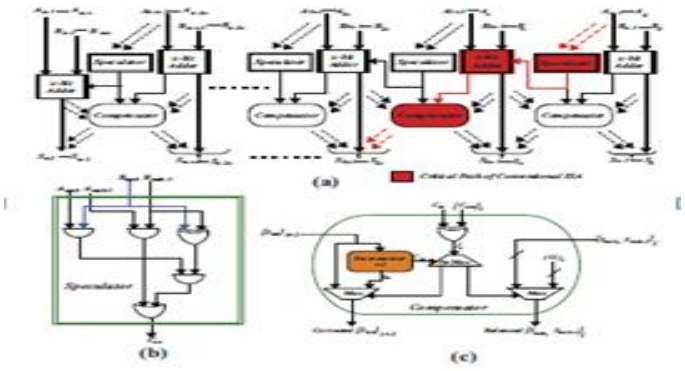

Fig.1: (a) *n*-bit ASA block diagram. (b) Netlist representation (c) Compensator structure

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Since carry look ahead has less propagation delay compared to other adder structures hence it has been employed. The adder block performs addition based on logic of carry look ahead for four-bit input and the sum is generated in parallel from each adder block is not the precise output due to the fact that the addition has been achieved by the usage of approximated carry inputs. Compensation and rectification of error in sum is corrected. Although compensator and speculator placed along critical path but as a matter of fact it is rarely activated, as in Fig. 1incidentally, it is required to mitigate this delay by practice of pipeline technique to make the structure suitable for lesser energy consumption and higher speed.

2) Error Correction Technique: Fig. 1(c) shows the structure of Error Correction. Comparing adder output and Predictive output is carried off by making use of a EXOR gate. The output from EXOR gate triggers an error flag (fe) for one of the error correction methods to correct and rectify the error, if any. If the output of EXOR-gate is '0' then the local sum is directly passed to the last output. Conversely, if the EXOR gate generates '1' then the error is of two types either low sum which is positive error or a high sum is negative error. Positive error generates '0' in the resultant of addition where '0' need to be replaced by '1' on the other hand high sum in which '1' has to be replaced by '0'. The compensator performs either unsigned increment or decrement at Least Significant Bits (LSB) to correct the error (high error is compensated by '-1' and low by '+1'). Provided there is no overflow in the result. In case of overflow, correction is accomplished by grouping most significant bits from the previous adder in the converse of error occurrence direction. If $\mathbf{2^n}$ error is occurred in the sum then correct error in the reverse direction from right most adder direction (*say* $Sn{-}1 = 1 \longrightarrow Sn{-}1 = 0$). In optimal case all LSBs are compensated in the reverse order, hence the overall error is less than 1.However, if the range of correction bits is 'd' then the 'd' LSBs are first considered from the four-bit adder block which are passed to compensator block for verification of overflow.

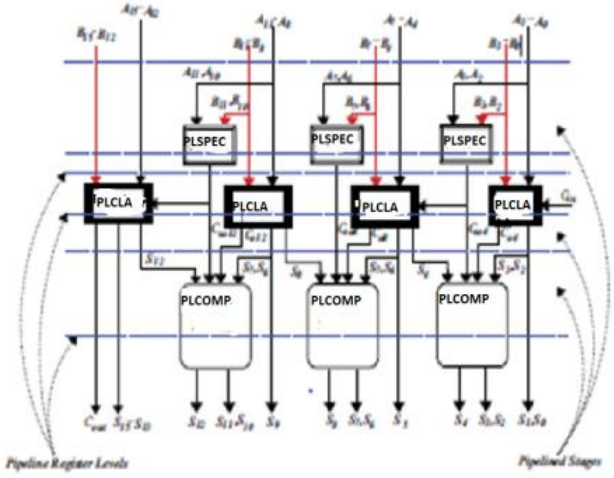

Fig. 2: Proposed Pipelined ASA VLSI architecture.

Pipelined Structure: Adder, speculator and compensator of ASA for four bit wide with pipeline are shown in fig.2. Carry-in is approximated from Prediction block for every adder and depending on the result adder computes the sum. Error is detected by evaluating approximated carry-in and carry-out from adder. Thereafter, error correction block compensates the error. Hence, the critical path of the architecture includes delays of speculator, adder and compensator. In the present context 'n' is considered to be four bit wide and structure does not altered for increment of ' n' and blocks remains same and unchanged. Experiments establish that speculator block rarely activates the critical path. Fig.3 represents the internal structure.

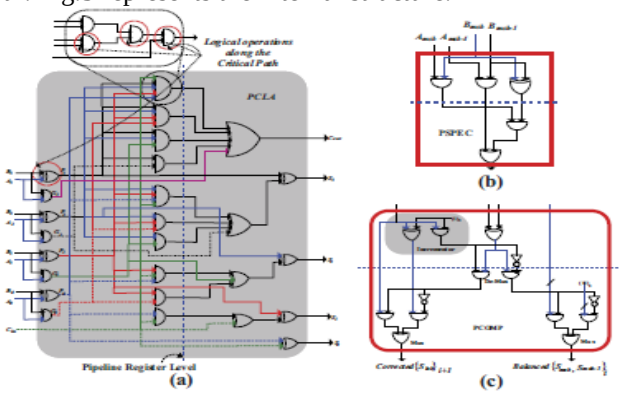

Fig. 3: Netlist of (a) Four-bit pipelined-carry look-ahead adder (PLCLA) (b) Pipelined speculator (PLSPEC) (c) Pipelined compensator (PLCOMP) for the proposed ASA VLSI structure

III. DISCUSSION OF RESULTS

Verification and validation of the proposed structure implementation on the ASIC and FPGA platforms has been briefed with experimental proofs for discussion.

A. FPGA Implementation

The proposed ASA architecture is coded in Verilog HDL and simulated and synthesized with ISE 14.3 suite. Synthesis is carried out for different inputs on Xilinx FPGA. Resource utilization and timing information is mentioned in the table.

S. No	FPGA Features	Description
01	FPGA Family	Spartan 3E
02	FPGA Device	Xc3s500e

ASA Architecture	32-bit PL ASA	32-bit NPL ASA
Technology	90	90
Sup. voltage	0.9	0.9
Seq.std.cells	222	96
Inverter std. cells	94	32
Buffer std. cells	1	-
Logic std. cells	189	86
Total no of std cells	510	217
Total Area	5.109	3.0287

	Slices	4 input lUT	IOBs	Crit.Path delay (ns)	Max.clk . Freq (MHz)
8b PL ASA	35	55	2	3.081	167.22
8bNPL ASA	21	27	27	5.396	187.76
16b PL ASA	70	110	51	3.081	324.57
16b NPL ASA	41	52	51	5.980	167.22

PL – Pipe Lined NPL -Non Pipe Lined

B. Power Consumption and Area Occupancy Report

In the digital circuit design, pipelining is the procedure of shortening the essential route on the price of place that's predominated with the aid of their registers used to create pipeline degrees in the design. Exploiting the advantages of clock gating where passive operations are suspended temporally to save powers which are normally performed at the beginning and completing of adder operation

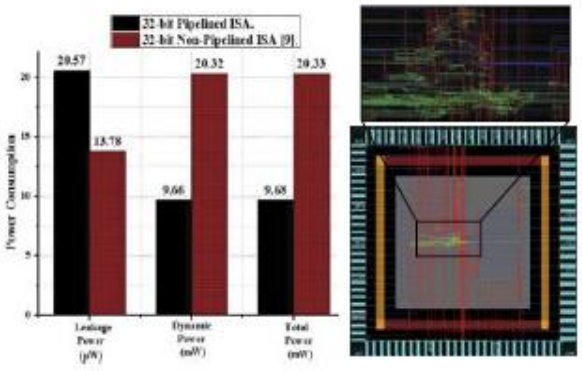

Fig. 4: Power dissipation spectrum for PL and NPL for ASIC

IV. CONCLUSION

In this paper, low power and high-speed model of ASA is proposed. The clock gated pipelined ASA architecture can enhance speed and alleviate energy consumption effectively. Experimental results showed it occupied 5.109 mm^2 of silicon area and required 9.68 mW of total power. Therefore, the proposed ASA can operate at higher speed with 47.25% decrease in energy and occupies 38.7% minimum area than the existing designs.

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