FPGA based On-Chip Phase Measurement System

Sangeetha Balne, T. Gowri, C. Kaushik

Abstract: ***Phase measurement is generally significant in electronic applications where the asynchronous connection between the signals requires to be defended — conventional automated frameworks used for time estimation, which are planned to use an old-style mixed-signal method. With the appearance of reconfigurable equipment, for example, Field Programmable Gate Array (FPGA), it is progressively worthwhile for researchers to choose for all-advanced design. Fast sequential handsets of FPGA hardware don't confirm the comparable chip inertness after each power cycle and reset cycle. This reason vulnerability of stage connection between recovered signals.In this paper, a reaearchofthephase measurement system with a focus on the frequently utilized techniques for high-resolution electronic applications is presented. The effects of phase measurement are evaluated on various performance metrics such as peak to peak jitter, power consumption,and chip area, etc.Thisresearch work motivates the researchers to do further research to preserve the synchronous relationship between signals in network-on-chip.***

Keywords: ***Electronic applications, classical mixed-signal technique, phase measurement, Reconfigurable hardware, and Transceivers.***

I. INTRODUCTION

Phase measurement used in phase data to align and synchronize signals between different circuit components. Minimized usage of full computerized structures, the reconfigurable equipment advancements like FPGA has a fundamental impact. It is fundamental that the latency-critical protocols keep up consistent stage contrasts in recovered signals for the entire investigation's run timeRationale structure for stage observing capacity to register stage move changes in 20 to 100 picoseconds (ps) is required inside the FPGA equipment .This would permit us to remove the relevant stage information and to recalibrate the framework when required to keep up the Constant Phase Relationships (CPRs).Phase difference detection of two similar frequency sinusoidal signals and Data Discriminate Technology (DDT)has been significantly utilized in a variety of fields such as Electric Power System (EPS), communication, electronic and automatic control and so on[1].

Several methods can do a phase difference measurement, for exampleindigital signal processing such as Fast Fourier Transformation (FFT) [2], Kalman filtering [3] and so on. These are significantly utilized phase difference measurement techniques,these strategies by and large need quite a while to play out the calculations.

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The phase correlation utilizes analog segments to change over the phase distinction into voltage. In spite of the fact that the strategy presents voltage float, analogand computerized quantization error boosts the estimation non-linearity and error estimation. The estimation of phase contrasts is like a Time-to-Digital Converter (TDC). The estimation of stage contrasts is normally used to calculate the stage qualification between intermittent flag and focusing on recognizing exact clock and data synchronization.

In this research work, phase measurement system with a focus on the frequently utilized techniques for high-resolution electronic applications are presented. The architecture of phase measurement is explained as follows.

II. THE ARCHITECTURE OF PHASE MEASUREMENT

Figure.1 shows the block diagram of FPGA based phase measurement, which consists of four blocks such as synchronizer, XOR-based phase detector, duty cycle computation, phase value computation.The function of each block is described in the below sections.

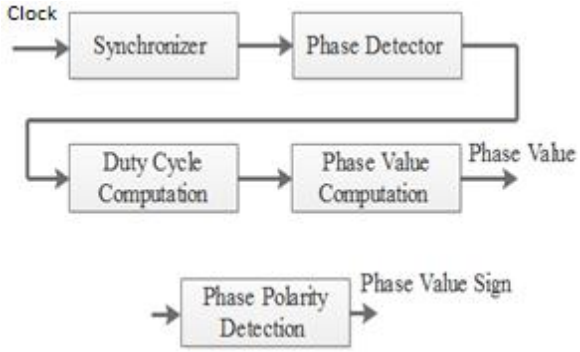

Fig.1. Block diagram of general phase measurement architecture

2.1 Synchronizer

At first, two high-frequency clock signals inside FPGA must be sampled and synchronized. There is no synchronous relationship between the reference clock (CLK1) and Sampling Clock (SC) that uses random sampling.So, the researchers utilize the systematic sampling technique for phase measurement. For this reason, the researcher synchronizes high-speed digital clocks. Two synchronous fast clock signals are examined with another free clock of much more slow frequency. The synchronizer will be formed by 4- D flip flops with Clk1, Clk 2 and sampling clock.The architecture of the synchronizer is represented in fig.2.

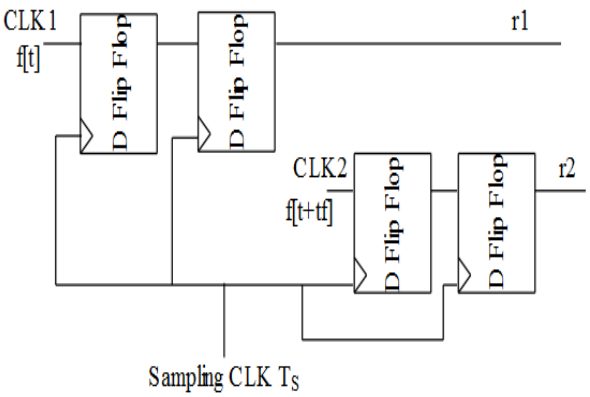

Fig.2 Architecture of synchronizer

2.2 Phase Detector

A precise stage estimation in the FPGA using subsamples gathered by efficient inspecting over the XOR-based phase identifier signal. XOR-based phase identifier presents the least planning jitter as a result of the effortlessness of its structure.The synchronized high-speed clock is fed to the XOR-based phase difference between high-frequency clock signals. Figure.3 shows the architecture of a phase detector. It includes D flip flop and bank skew operation. The dynamic phase move strategy is used to discover the measure of bank skew process which required to skey cancellation delay $tskew$ (p).Fig. 3 shows the architecture of XOR phase detector.

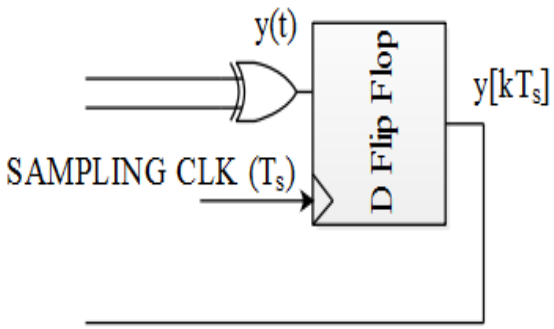

Fig.3 The architecture of the XOR phase detector

2.3 Duty Cycle Computation

The sample population size is represent as a number of samples acquired for phase computation. For counting of samples up to N for XORed signal duty cycle and reference clock duty cycle, the counters are utilized in this block. The architecture of duty cycle computation is presented in fig.4

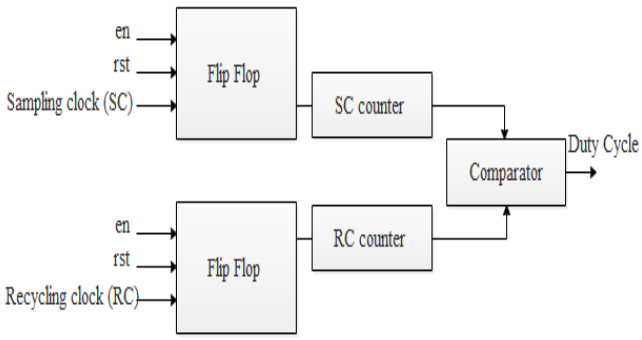

Fig. 4 Architecture of duty cycle computation

2.4 Polarity Detection

The architecture of phase polarity detection is shown infigure.5. The bank skew cancellation can be computed in this block.

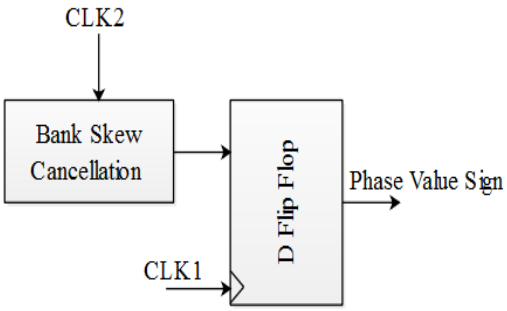

Fig. 5 The architecture of phase polarity detection

III. CHALLENGES AND DESIGNS CONSIDERATIONS

The principle of Phase Measurement Systems (PMSs) is very simple, however,itstill involves several design challenges. Most importantly entirely stable sampling frequency is huge for ideal estimation execution. On the off chance that the stage or frequency of the sampling clock isn't generally steady during the estimation and the checking of two High-Speed Clock (HSC) gets misshaped and could debase the framework precision. The proposed characterization of inspecting clock jitter execution is a basic undertaking. The power supply is another urgent part that requires legitimate plan. On the off chance that any aggravations on control course like commotion from the DC/DC converters could change the engendering postpone dormant components like FPGA. With regards to stage estimations this is unpredictable on the grounds that it will endure the checking of the clock time frame. In spite of the fact that if the two estimated HSC are entirely steady for a generally prolonged stretch of time, it is sufficient to simply boost the number of tests. At long last, any noise would vanish from the estimation if the examining proceeds with long sufficient opportunity. It's anything but an ideal arrangement however since the estimation ought to join to a suitable output as quick as would be prudent. Consequently, it is desire to figure the precise frequency proportion among HSCs and sampling clock, with the goal that the inspecting clock will move through the HSC a much number of times. The computation of optimum sampling times vs phase resolution and accuracy is presenting another challenge.

IV. OVERVIEW OF SIGNIFICANT PHASE MEASUREMENT TECHNIQUES

A few process for phase estimation have been talked about in this section. The old-style standard of utilizing the oversampling method is insufficient to calculate a relative stage distinction between the two high-frequency clocks inside an FPGA texture, whose frequency surpasses the most extreme utmost bolstered by the fabric (<500 MHz).In this paper, research on different existing techniques: Duty CycleCorrector (DCC), XOR-based phase measurement, zero crossings, delay chain, and progressive phase shift. The overview of these techniques is explained as follows.

4.1 Duty Cycle Corrector

HSC accepting and conveying is the most noteworthy difficulties. Double Date Rate (DDR) information converter where information is changed over on both edges of clock, which is an eminent choice to acquire low control with fast. A half duty cycle check signal is basic in these circuit frameworks.But, it is hard to keep up the obligation cycle of clock precisely at half in light of confounds presented by voltage, temperature, deviations of the procedure, and noise coupled to the sign transmission way.Thus DCC following the clock beneficiary is imperative to align the clock almost 50 % duty cycle to consequent hardware.Consequently, the glitch influencing the dynamic execution, which happens during the switch change is impacted by the intersection of the differential clock [2].

4.2 XOR-based phase detector

These days,thelatest procedures for precise phase estimation in FPGA using subsample gathered by orderly examining over XOR-based phase locator signal. The XOR-based phase identifier presents the least planning jitter because of the simplicity of its structures [2]. XOR-based phase finder technique is a lot of reasons to build a rationale center for relative stage estimation. In the phase counts, some other instrumentation technique is exposed to particular kinds of errors, which can be sorted as pursues. It happens in light of clock skew $tskew\ (m)$somewhere in the range of CLK1 and CLK2. Clock skew 20 is decreased by setting exact time imperatives to train the channel place and route motor to do high vigorous planning conclusion for characterized ways 21 and evades varieties of clock skew by huge an edge with each firmware update. That happens due to ank skew $tskew\ (m)$between phase identifier square and polarity recognize square. Bank skew 20 is somewhat skew which means to output skew between the signals with a signal driving info terminal. Here, $tskew(p) = \{tCLK1 - tCLK1*\} - \{tCLK2 - tCLK2*\}$.

4.3 Zero Crossing technique

The Zero Crossing Detection (ZCD) is the broadest method for estimating the Period of Periodic Signal (PPS) or frequency. The precision of estimating zero intersections for synchronizing power framework control and instrumentation needs a few systems to diminish phase discovery errors from signals defiled with noise and unessential signal. The ZCD is the broadest system for estimating the frequency or time of an intermittent signal. While ascertaining the frequency of a signal, for the most part the quantity of cycles of a reference signal is figured more than at least one time spans of the signal being estimated. The estimating numerous periods limits mistakes brought about by stage noise by making the annoyance in zero-crossing comparative with the absolute time of estimation. The outcomes are a precise estimation of the detriment of moderate estimation rates. The zero-crossing is a fundamental decision for processing stage and frequency. Reference is commonly simple to actualize and signals amplitude pace of progress is greatest at signal zero. The stage synchronized activating needs setting extra imperatives on zero-crossing location [3].

4.4 Delay Line Technique

Delay Line Technique (DLT) is an improvement from the direct checking estimation procedure. In the estimation procedure of regular systems containing direct checking, time-to-voltage change, and Vernier. To upgrade estimation exactness, two brief time interims between reference frequency signal and count gates beginning and stop edge must be processed precisely. Subsequently the multifaceted nature of execution amplifies. Something else, the estimation exactness is low, for example, direct counting system. Based on delay chain, the system utilize the frequencies. Relationship of these Reference Frequency Signals (RFSs) changes ±1 count error to ±1 defer time mistake of delay unit. This procedure requires not the intricacy of usage. The standard of defer line strategy is as per the following. For brief time interim estimation, rising and falling of count gate is synchronous with the beginning and consummation signal of the tried brief time interim, individually. RFS isn't one way however multi-way (for instance n-way). This system utilizes a delay chain, which comprises of $n-1$ delay units to produce $n-path$RFSs, which are deferred consistently in RFSs, which are postponed consistently in Reference Frequency Period (RFP). At that point the $n-path$RFSs are counted all the while under same count gate. The normal of n-way considers is used the reference frequency count. By thusly, two ±1 check error among RFS and count gate beginning and stop edge is be decreased. Estimation error can diminish by $1{\sim}2$ request of greatness contrasted and direct checking estimation procedure. Some critical stage estimation methods are portrayed in the following segment.

4.5Progressive phase shift

In this strategy, separation is the phase-contrast somewhere in the range of $signal1$ and $signal2$. In stage location circuit, the rising edges of the two signals are broke down. At the point when the signal is not adjusted, $signal1$ is delayed by time until edge arrangement of two signals is recognized. On the off chance that the edge arrangement is found after mdelays of τ have been performed. At that point the estimation aftereffect of the stage distinction can be acquired from the Eq. (1).

$$\Delta t = m \times \tau \qquad (1)$$

Despite the fact that the guideline of progressive phase shift is basic, troubles exist in the usage of the strategy. At first, limit the step delay to improve the estimation accuracy. Second, delay linearity of delay components characterizes the estimations mistake of the system. A usually used strategy to actualize a progressive phase shift is developing a delay line. This delay line can be made by simple and computerized components.

V. LITERATURE WORKS

Researchers suggested several different techniques for phase correction on FPGA platform. In this section, a brief evaluation of some significant contributions to the existing methods is presented. In Table.1 includes advantages, disadvantage and performance measures are described for each technique.

Table 1 Performance analysis for existing phase measurement techniques

Author	Method	Technology	Frequency Range	Advantage	Disadvantage	Performance Measure
Shao-Ku Kaon, Yong-De You [4]	Clock buffer with duty cycle corrector.	0.18 um CMOS	100 MHz to 1 GHz	The proposed circuit can generate around 50% duty cycle as input clock.	More power and running time affects the jitterperformance.	Maximum duty error of 0.5%,
Jianhui Wu et al. [5]	Duty cycle corrector. This works upto 3.5GHz frequency.	0.18 um CMOS	1 MHz–3.5 GHz	The proposed method was achieved the highest operation frequency and any trimming must be avoided.	Based on the input frequency, the output pulse is scaled down which degrades the output waveform.	Peak to peak jitter 33.3 ps, power dissipation is 0.6Mw at operating frequency of 2 GHz.
Prakash et al. [6]	DCC with mixed more dual loop.	SPICE using Cadence Virtuoso in CMOS process with the latest technology	4 to 8 GHz.	This work handle the high frequency clocks with less power.	The output of the comparator was not showing exactly. Too difficult to understand whether the clock pulse has been generated from OPAMP input or not.	Duty cycle accuracy is 50 ±1 %, peak to peak jitter is 1.61 ps at 8 GHz.
Fang et al. [7]	Duty cycle imbalance correction with multiphase.	0.13 µm CMOS	2.5 GHz	The proposed method has minimized the deviation of duty cycle with less power consumption.	This paper number of multiplexers was used which cause more power. because 8T has been used to design single multiplexer which increases the area also.	Maximum power consumption of 2.4 mW, Silicon area of 65 µm × 100 µm.
Harikrishna et al. [8]	XOR based phase detector.	45 nm submicron CMOS	-	This work rectify the errors on both edges of clock.	This work is too difficult to predict the differenciation in frequencies.	Phase Difference between 2π
Kim et al. [9]	CMOS folding ADC.	45 nm Samsung CMOS	1 GHz	The proposed method was improved the asymmetrical boundary condition error of the conventional folding structure.	The input operating frequency is too low around 1GHz only which reduce the system speed.	The effective chip area is 1.98 mm2, power dissipation is 80mW.
Hung et al [10]	A new delay line sharing based CMOS digital pulse width modulators circuit.	0.18 micron CMOS	200 MHz	A delay-line function block was shared with MSB and LSB groups to minimize power consumption.	Resulting Performancesare not efficient.	1.55-mW power consumption.

VI. CONCLUSION

Simple phase detector needs absolutely several special elementssuch as internal and external Phase Lock Loop (PLL) and can be utilized in high speed clocks with frequencies up to the furthest reaches of information and output ports. It just utilizes one extra autonomous clock, which is used to filter the rapid clocks. Be that as it may, its free frequency ought to be demonstrated to guarantee better execution. In spite of the fact that it is a lot easier in plan it can accomplish better execution with high precision and phase goals.Numerous researches have tried to minimize the power consumption for achieving synchronization between signals. From this works, a few studies have improved power consumption, and highly suitable for proper signal synchronization in VLSI design.

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