Design of a High Speed and Low Power Sample and Hold Circuit for 16 Bit ADC

Chakradhar Adupa, Chaithanya Mannepalli, K.Shashidhar, Srineevasa Rao Ijjada

Abstract- Data plays an important role in the present world where the communications are becoming so crucial. Data acquisition and communication systems are in need ofhigherresolution (i.e., 16 Bits)ADCs. The successive approximation (SAR) ADCis suitable for medium to high range resolution applications, the basic building block of the ADC is Sample and hold circuit which will perform a key role in data conversion from analog data to corresponding digital data.In this paper an operational amplifier with gain 96.5 dB and phase margin of 77^0 with UGB of 12 MHz is designed to implement high speed and low power sample and hold (S/H) circuit using 0.18 µm SCL CMOS Technology, for higher bit ADC applications with sampling frequency of 10 MHz consuming 182 µW power operating at 3.3 V.

Keywords:ADC,Micro-power, sampling mode, holding mode and CMOS.

I. INTRODUCTION

Sampling and hold circuit is an initial block of SAR ADCits main function is to sample the input and hold for a while continuously to generate sampled output in discrete time intervals so as to feed to the successive blocks in design. The SAR ADC block diagram is presented in fig.1 where the S/H circuit provides the output to the comparator to compare with DAC output. The key elements in SAR ADC are sample and hold circuit, comparator, SAR logic and DAC. Accuracy limitations are due to mismatches between resistors in resistive DAC and capacitors in capacitive DAC leads to variation in the corresponding currents through their branches. Another limitation is due to comparator offset which directly impacts the output to the SAR leading to major deviation from the expected result. Key block and initial block of the SAR ADC is S/H where the accuracy is limited by the switches noise, charge injection, clock feed through, aperture jitter, and settling time it should be so accurate for exact digital conversion[1][9].

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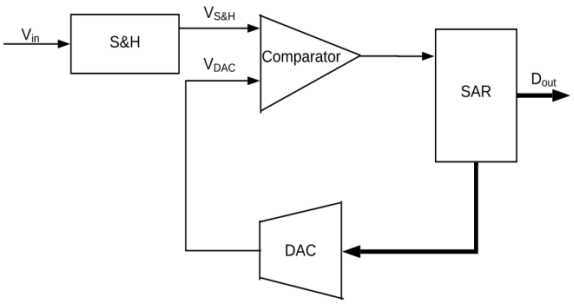

Fig.1. Block diagram of SAR ADC with sample and hold circuit

II. OPERATING PRINCIPLE SAMPLE AND HOLD CIRCUIT

The fundamental working principle of sample and hold block is that it samples the input analog signal and holds the sampled signal. Sampling period and hold period are the time required for sampling and holding the sampled signal respectively. Fig 2 shows the block diagram of sample and hold circuit sampling and holding is a prime step in the conversion process as ADC requires a certain amount of time for identifying the signal so that it can take the analog signal and can able to convert to its corresponding digital signal if the analog signal is directly applied to the ADC then it can take the signal which is continuously varying with respect to time hence there is a need of sample and hold circuit which will provide that holding period for the analog input signal while the output of this sample and hold circuit is given to the ADC for conversion. Apart from this data converter modules these sample and hold circuits are also find useful applications in the sampling Oscilloscopes as wellas data distribution systems [1-3].

The expected output of sample and hold circuit is shown in fig 3, generalized function of a sample and hold operation usually performed in the modules, the input signal is applied as V_{in} and V_{out} is output signal obtained. The basic block consists of an input and an output as well as a control signal.Expected outcome of sample and hold circuit is as the output waveforms shown in fig 3will give an insight of the process involved in the S/H circuit. The analog switch is on and off based upon the control signal,when switch is on it is operating in sampling mode and when switch is off it is operating on hold mode. The capacitor charges and discharges accordinglyto produce the sampled output.

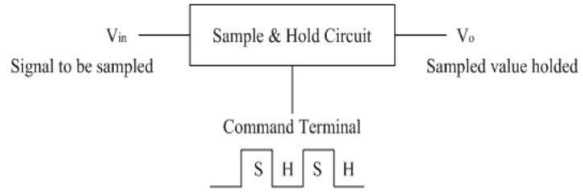

Fig.2. Block diagram of Sample and Hold Circuit

S/H circuit output gets induced by errors due to several factors in sampling mode and holding mode. The main factors effecting output is during holding mode, the errors considered are [4-5].

***Charge injection*:** MOSFET used as a switch need to be designed robust to the leakages as device dimensions shrinks down the leakages increases. During the hold mode charge gets injected from source to drain.

***Clock feed through*:** It is due to overlap capacitance this is minimum as on with charge injection but leads to error in ADC. The gate to source capacitance should be nullified by adjusting the sampling capacitance.

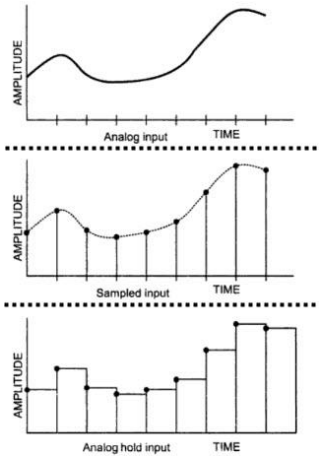

Fig.3. Expected waveforms of sample and hold block

III. DESIGN OF SAMPLE AND HOLD

Sample and hold architecture involves capacitor for hold mode, switch for sampling and a buffer or voltage follower implemented by operational amplifier [6-8].The voltage relation of the S/H circuit is given as in (1)

$$V_{out} = V_{in}\left(1 - \frac{1}{A_o}\left(\frac{C_{int}}{C_s} + 1\right)\right) \quad (1)$$

Where $V_{out}$is the output of S/H

$V_{in}$is the input to S/H

$C_{int}$is the internal capacitance of the MOS transistor Switch

C_S is the sampling capacitor

A_o is the Gain of the Amplifier

For higher bit resolution of the ADC the switch operational amplifier gain should be nearing to 100 dB and the accuracy of the output should vary in the range of microvolt in time period less than 8 ns such the sampling rate can be increased up to 100 MSPS. The amplifier designed for the switch is to be worked during both sample and hold mode with higher bandwidth range such that effective conversions can be done in wider range of applications.

***Design of switch*:**[7]The switch is to be more robust when it is in off mode the switch resistance considered to be high and also optimal for the whole circuit design the R_{on} is given by eq-2, switch plays a pivotal role in the sampling and holding process it should be so accurate that there is no leakage and overlap capacitance from source to gate should be maintained using equation 2 such that the feed through is reduced to a great extent.

$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_{TH})} \quad (2)$$

***Importance of Operational Amplifier in Sample and Hold*[10-11]:** Sampling and Holding operation circuit can be designed by using an operational amplifier which functions as a buffer. The functionality of ADC depends upon the operational amplifier design and a simple switch where switch is implemented by MOSFET. Factors like sampling rate and the resolution is pivoted on the design of sampling amplifier. The operational amplifier can be designed apart from simple differential pair, the two stage op-amp and telescopic operational amplifiers can be considered for higher gain and low offset operations.

General block representation of Op-Amp: Operational Amplifier consists of the crucial differential pair where it subdues noise and makes the output effective the differential pair gain in not enough to maintain the resolution of the ADC when chosen greater than 10 bits. The targeted ADC using the S/H circuit in this paper is of 16 bit hence the two stage operational amplifier is chosen. The characteristics of Op-Amp consider for effectiveness of the ADC operations are offset, slew rate and gain.Fig 4 represents the block diagram of Op-Amp where the input is of inverting and non-inverting terminals, these inputs are to the differential pair the input stage shown in the fig 4 is the differential stage. The intermediate stage is for compensation and the level shifting circuit is for the improving gain. The output stage is for the driving load circuit connected.

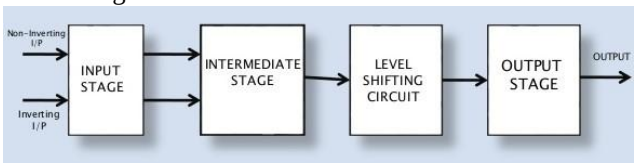

Fig.4. Block Representation of Operational Amplifier

IV. DESIGN AND ANALYSIS

Operational amplifier is designed using the standard mathematical equations[10] and the switch is designed using MOSFET with equation-2 in section-III for S/H circuit.

Operational amplifier design:

Two-stage operational amplifier is designed as [9-11] and the schematic is shown in fig 5 where the transistors M1 and M2 act as differential pair, to reduce offset these transistors need to be sized too precisely the gain also depends up on these input transistors if the transistor size is increased the gain get increased which in turn helps the S/H circuit in supporting 16 bit ADC. The M3 and M4 transistors plays the role of load pair where the gain can be adjusted using the aspect ratio of them.

The compensation capacitance and the current through M5 decide the slew rate and helps in attaining the output without clipping. The ICMR- input common mode range where the operational amplifier functions accurately is decided based on the transistors M1, M3 formaximum ICMR and M1, M5 for minimum ICMR. Transistor M6 and M7 act as gain stage for the differential amplifier this design of Op-Amp is used to drive the MOS loads hence capacitive load is selected. Transistor M8 is used to copy the current using mirror concept to bias the M5 transistor. The supply chosen is Vdd where a 3.3V supply is desired to operate the designed operational amplifier for the low offset, high speed and high gain applications.

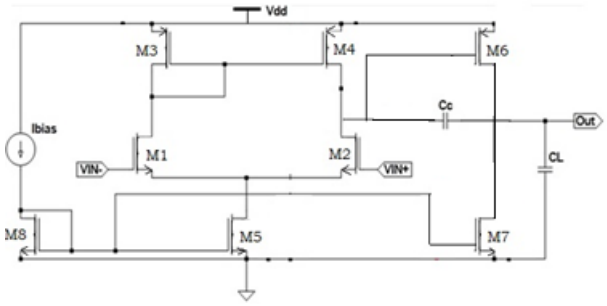

Fig.5. Schematic of Operational Amplifier for S/H Circuit

S/H circuit design:

Sampling and holding circuit schematic designed based on the analysis of section III is shown in fig 6 where the switch is designed for higher Resistance such that the accuracy is high. The operational amplifier is designed to work at supply of 3.3 V attaining the gain of 100 dB with power consumption of 145 µW and having a slew rate of 20 V/µs. The capacitor is chosen based up on the equation 1 such that the sample and hold operation is attained successfully. The schematic takes analog signal as $V_{In}$where the control signal for MOS transistor is clock and samples the input for resulting the sampled output signal of the input analog signal.

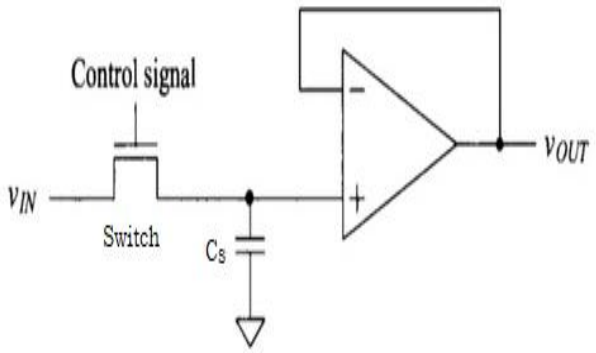

Fig.6. Schematic of S/H circuit

III. RESULTS AND ANALYSIS

The design of operational amplifier and the S/H circuit is implemented using cadence virtuoso with SCL 0.18µm CMOS Technology and obtained results are discussed in this section.

a) Operational amplifier Results:

The gain and phase plot is represented in fig.7 and fig.8 respectively where the gain is observed as 96.50dB which is nearing to 100 dB and is most suited for the design of S/H for higher resolution ADC.

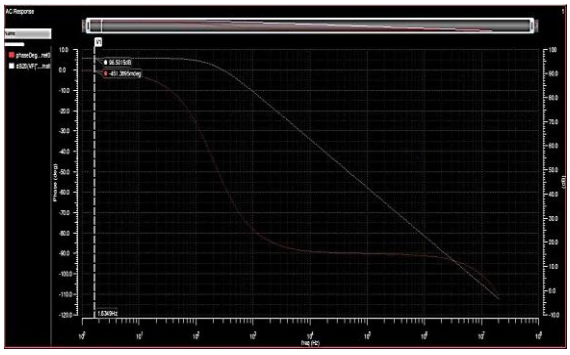

Fig. 7. Gain Plot of Operational Amplifier

The stability of the system decides the overall accuracy of the ADC, the Op-Amp designed constitutes in the operation of S/H circuit which need to be so stable such that it operates in boundary conditions. The range of frequencies in which the op-amp can be successfully operated is 12 MHz.the phase margin of the operational amplifier is 77^0. The Op-Amp designed consumes a power of 168µW.

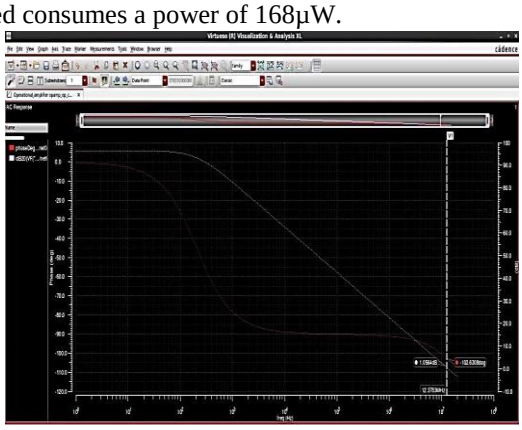

Fig. 8. Phase Plot of Operational Amplifier

b) S/H circuit Result:

Switch and operational amplifier is designed for attaining the specifications using the equations in section III by 0.18µm SCL CMOS Technology. The output waveform is depicted in fig 9. Where the input signal given on net9 is successfully sampled at a rate of 10 MHz and shown in sh_out output wave form. The sampling clock is given at a frequency of 10 MHz at net8. The input signal is of frequency 1MHz.

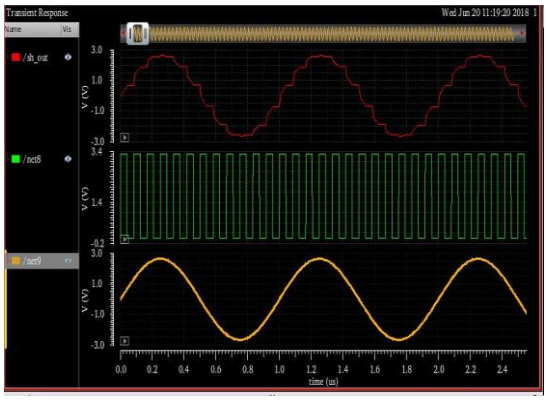

Fig. 9. Output waveforms of input, sampling and sampled Signal

The results are tabulated and compared with previous literature in table 1, where the power consumption is far better than other circuits and the designed S/H circuit is for higher resolution ADC of 16 bit. The ADC is analog device where the technology is stable at 0.18 µm Technology and the design can be further carried out even if technology gets scaled down. The table shows the technology and supply at which the circuits are designed, it also shows the type of switch and Op-Amp used to design S/H circuit. The power consumption, sampling rate and number of bits the S/H circuit supports also tabulated. The paper [6] and [7] discusses about the replacement of switch with current minimum and current subtracter circuit. Where, in this work we designed the switch using a simple MOSFET. For further improvement of the S/H circuit the switch can be modeled using special techniques with more robustness and linearization techniques, Op-Amp can be replaced with cascaded Op-Amps.

Table-I. Comparison of Designed S/H Circuit with Literature

Parameters	[6]	[7]	[8]	This Work
Tech. (µm)	0.5	0.5	0.35	0.18
Supply (V)	3	3	3.3	3.3
Type of Switch	Current minimum	Current Subtracter and Half wave rectifier	MOS	MOSFET
Type of Op-Amp	-	-	OTA	Two-Stage
Sampling Rate (MHz)	10	10	80	10
Supporting ADC Bits (Bits)	8	8	14	16
Power Consumption	250 µW	225 µW	21.5 mW	182 µW

IV. CONCLUSION

This paper discusses in detail about design and analysis of operational amplifier and S/H circuit by considering major limitations for the performance. An Op-Amp with gain of 96.5 dB operating up to frequency of 12 MHz with a phase margin of 77^0 consuming a power of 168µW is designed for implementing a high speed and low power S/H circuit with sampling frequency of MHz consuming 182 µW power operating at 3.3 V supply using 0.18 µm SCL CMOS Technology for 16 Bit SAR ADC.

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AUTHORS PROFILE

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