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Performance Analysis of Double Gate Hetero Junction Tunnel Fet

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***Abstract:** In this paper, a novel heterojunction tunnel field-effect transistor (HTFET) using Sentaurus technology computer-aided design (TCAD) simulations has been presented. The InAs/GaSb compound materials are used in both single gate heterojunction TFET (SG-HTFET) and Double gate heterojunction TFET (DG-HTFET) with SiO2 gate oxide layer to increase performance of the device.The implemented SG-HTFET and DG-HTFET device are increase the TFET's cross-sectional tunnel area. This result develops the subthreshold swing (SS) by 2.45 times, drive current (I_{ON}) is close to 10^{-6} A/µm, leakage current (I_{OFF}) is close to 10^{-17} A/µm and also diminish the ambipolarity of the device compared to the TFET.*

***Keywords :** Ambipolarity, Heterojunction TFET (HTFET), Double gate hetrojunction transistor (DG-HTFET), tunnelling field-effect transistor (TFET).*

I. INTRODUCTION

One of the major challenge in the sub-30 nm regime's scaling of CMOS technology is power consumption[1]. A MOSFET's scaling under the 30-nm regime includes extreme supply voltage (VDD) scaling. Conversely, the subthreshold slope (SS) minimum fundamental limit on VDD scaling. To overcome this problem, energy filtering mechanisms-based devices such as TFETs are being more investigated to achieve the steep switching value below 60 mV/decade(at room temperature) [2]. Using materials such as Si, Ge, SiGe, and III-V materials several device structures have been implemented over the past decade to generate TFETs with high on current(Ion), low on/off current ratio (Ion/ Ioff)[3]–[5]. Because the band gap energy of InAs / GaSb compound materials is less, these materials are competitive among other material systems.

Due to their complete process technology, HTFET's constructed using III-V materials with limited lattice imbalance such as InAs / GaSb are of great attention to the system research community[6]–[8]. Area-scaled TFET systems have been developed in the recent past to improve the cross-sectional area of the device tunnelling [9],[10].The use of area-scaled TFETs increases the device footprint area compared to existing TFETs for the same channel length[5]. Therefore, to remedy this situation, a nonplanar architecture is required [11]. Recently, a tunnel junction structure developed by Hetro junction TFET (HTFET) was proposed to increase the drive current with a reduced device footprint area[12].

The work is structured as follows: in section II the device structure and also the simulation setup for device optimization is elaborated. In section III, the proposed device simulations are presented. Comparison parameters in TFET, SG-HTFET and DG-HTFET in Section IV. And finally, the paper is concluded in Section V.

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II. DEVICE ARCHITECTURE AND SIMULATION SETUP

On the source side, an HTFET structure is doped with InAs material and GaSb material as a channel and drain side doped material.

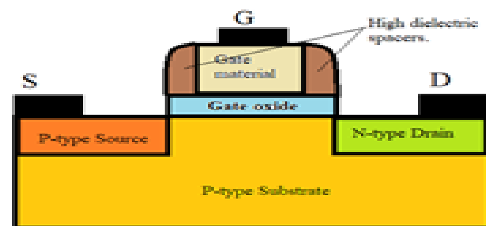
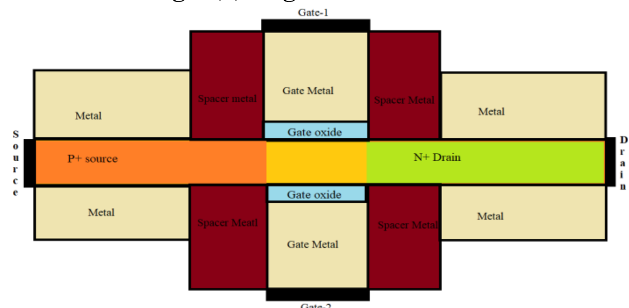


Fig. 1(a) single Gate HTFET.



(b)Double gate HTFET

The SG-HTFET and DG-HTFET device cross section is shown in Fig. 1(a) and (b) above. Throughout the simulation, a metal gate work function= 4.6 eV with a 3 nm gate oxide layer (SiO2) (EOT=0.5 nm).The doping concentration of 5×10^{19} is fixed for source and 5×10^{18} for both drain and channel .

Table 1. Simulation setup of device parameters and values.

S.NO	Para meters	values
1	p-type doping (source)	5×10^{19} cm−3
2	n-type doping (drain)	5×10^{18} cm−3
3	n-type doping (channel)	1×10^{17} cm−3
4	HfO2 material thick ness	10nm
5	SiO2 material thick ness	3nm
6	Gate metal thick ness	7nm
7	Gate workfunction	4.6 eV

The geometric setup of the hetero junction TFET as InAS material is used in source, channel and substrate.

GaSb material is used to drain. HfO2 material is used in spacer and SiO2 material used in gate oxide .The nonlocal path band to band tunnelling model[13] was used to model the tunnel in the proposed structure. In accumulation, SRH recombination and band gap narrowing (old slot boom) models are used the device. For minimalism, quantum effects are not obviously constituted in the work except otherwise highlighted. The simulation setup of device parameters and values are presented in Table 1 [8], [14].
These devices get the same surface area, but in contrast with the TFET, the HTFET has a greater cross-sectional tunnel area. For a fair assessment, both devices ' epitaxial layer thickness (t_{CH}) is set at 7 nm and channel length (L_{CH}) at 20 nm.

III. Results and Discussion

In fig. 2, I_D versus V_{GS} characteristics for HTFET is compared between drain current dynamic nonlocal path model and drain current dynamic barrier tunnel model. The dynamic barrier tunnel model performance is better than the dynamic nonlocal path model because the barrier height is changed with respect to the applied voltage The energy barrier in this condition is narrow enough where electrons will tunnel from the p+ region's valance band to the intrinsic region's conductive band. The non-local band-to-band tunnelling through the tunnel barrier and the overall bi-polar nature of the current flow are evident.

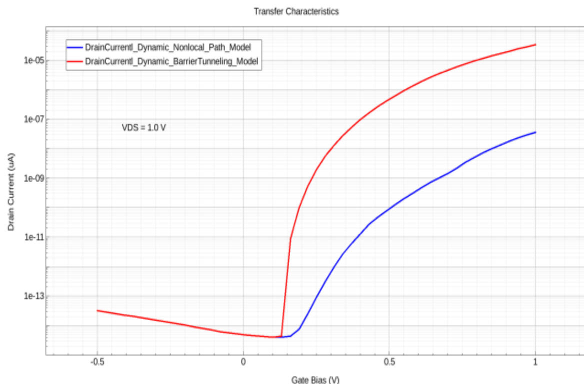


Figure 2. I_D vs V_{GS} characteristics comparison for DG-HTFET

Also note that current flow and tunneling are fairly evenly distributed across the channel width, at least in this thin-fin DG structure, even without consideration of quantum effects; the device operates in a near-flat-band condition.

For each device, many such simulations have been performed to obtain and understand their |IDS|-VG and IDS-|VDS| characteristics. For initial |IDS|-VG simulations, the source VS and drain VD voltages for the n-channel single gate and double gate HTFET devices, were biased as if in the OFF-state or just switched to the ON-state within a CMOS-like inverter, although with a supply voltage VDD of only 75 mV. For the n-channel devices, the source was grounded and VD was set to VDD; All devices show very abrupt switching in the critical sub-threshold regime.

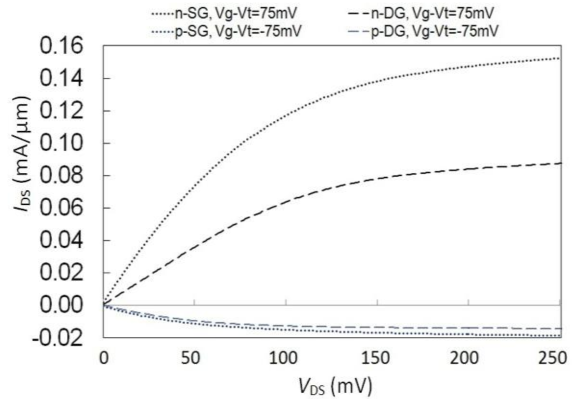


Figure 3. Comparison of performance parameters SG and DG-HTFET I_{DS} versus V_{DS} characteristics

Finally, Figure 3 shows the I_{DS} vs. $|V_D-V_S|$ for a 75 mV gate overdrive voltage $|V_G-V_{Th}|$. As can be seen, saturation is more difficult to achieve at low voltages. For $|V_D-V_S|$ of only a few kBT, back injection of charge carriers from the source would prevent saturation. The lack of saturation beyond that, however suggest perhaps some effect of the drain voltage on the channel tunneling barrier and/or channel potential profile, the TFET equivalent of drain-induced-barrier lowering. Of more concern than the lack of I_{DS} current saturation would be variation in the gate V_{Th} with $|V_D-V_S|$.

IV. Performance Comparison of Device Parameters

To get a superior perception into the performance of the SG-HTFET and DG-HTFET device, the device parameters of both HTFET devices are associated with conventional TFET in this module. The drain current (I_D) versus V_{GS} curves of both devices are shown in Fig.3. The both HTFET devices results are superior to the conventional TFET at the VGS and the VDS value of 1.0 and 0.5 V, correspondingly.

Table 2. Lists of the work out electrical parameters of the DG-TFET

PARAMETERS	TFET	SG-HTFET	DGTFET
SS (mV/decade)	43.99	41.59	41.54
I_{ON} (μA/μm)	43.8	5.26	5.84
I_{OFF} (μA/μm)	40.3	25.2	24.3
I_{ON}/I_{OFF}	1.09×10^{12}	2.087×10^{11}	2.403×10^{11}

The enhancement in drive current of the DG-HTFET device is due to the better Sub-threshold slope value of the device that is attributed to the greater tunneling area and improved gate control in the overlap region.

It is evident from the results that, the drain current performance is improving with replacement of high-k gate materials instead of using conventional SiO_2. Threshold voltage (V_{th}) of DG-TFET reduces with high-k gate, as shown in Table 2 due to improved electrostatic filed inside tunneling region. This is also a scientific indication for lower power supply.

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The output characteristic is improved with increasing drain voltage and achieves its optimum value for drain voltage V_{DS} equal to 1.0 V. The use of high-k improves the output characteristics for a low gate voltage of the order of 0.5 V. An increase in the drain voltage V_{DS} greatly increased I_{ON} current but had no effect on the threshold voltage.

V. CONCLUSIONS

Dynamic band-to-band tunnelling depends mainly upon barrier width and band alignment in III-V semiconductor based heterostructures and process materials for TFETs [15]. Improved control over the barrier shape can be obtained by strategically placing the hetero-interfaces, and desired band alignment can be achieved by changing the mole fraction of these compound materials. III-V materials also generally offer higher mobility, which further improves the subthreshold swing (SS) by 2.45 times, drive current (I_{ON}) is close to 10^{-6} A/µm, leakage current (I_{OFF}) is close to 10^{-17} A/µm compared to the TFET. Besides, these structures of single gate HTFET and Double gate HTFET diminish the ambipolarity of the device in evaluation to the conventional TFET

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It is optional. The preferred spelling of the word "acknowledgment" in American English is without an "e" after the "g." Use the singular heading even if you have many acknowledgments. Avoid expressions such as "One of us (S.B.A.) would like to thank ... ." Instead, write "F. A. Author thanks " Sponsor and financial support acknowledgments are placed in the unnumbered footnote on the first page.

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