Single Stage 38 GHz LNA using 0.1 µm GaAs HEMT

Lakshmi Balla, Venkata Krishna Sharma Gollakota

Abstract: Design of a 38 GHz low noise amplifier using a single stage common source (SSCS) with source degenerated with inductor topology with gain of 9 dB and noise figure (NF) of 1.5 dB using 0.1 µm GaAs pHEMT as active device is proposed in this paper. CS with source degenerated with inductor topology of 0.1 µm GaAs pHEMT resulted a very low NF compared to other HEMT technologies as well as other CMOS technologies at this RF range.

Keywords: pseudomorphic high electron mobility transistor (pHEMT); gallium arsenide (GaAs); Low noise amplifier; inductive source degeneration; CS topology; radio frequency (RF).

I. INTRODUCTION

Deployment of Q, V bands for satellite communication makes necessity of active devices at the millimeter wave frequencies. Design challenges at these frequencies are distributed nature of lumped components, unavailable accurate models of passive components and decreased performance of active devices. Designing of interconnections is also difficult at these frequencies. In this paper 0.1 µm GaAs pHEMT used as active device for designing a LNA. This active device offers low parasitics so that it is highly suitable in design of real time satellite communication applications. Low NF high gain are the basic needs of LNA. Advancement in technology leads to monolithic microwave integrated circuit (MMIC) technology. pHEMT is very competitive with other HEMT's. Hence MMIC LNA is necessary in millimeter wave (30 – 300 GHz) applications like satellite communications and radio astronomy. Reproductability is the main advantage of MMIC.

In beginning single stage (SS) LNA was designed using HEMT around 40 Ghz range for radio astronomy applications [1, 2]. But they obtained a very high NF. Later on SS LNA's are also designed using CMOS technologies [3, 4] with relatively low NF. This proposed work used a SSCS configuration with source degenerated with inductor results a very low NF compared to the above technologies. This inductive source degeneration gives good stability as well as good trade-off between NF and gain.

Paper contains five sections. Section I is about the introduction. Section II describes about the technology. Section III explains about LNA design. Simulated results are

discussed and compared in section IV. Finally section V is about conclusion.

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II. TECHNOLOGY

PP10-10 technology HEMT with 0.1 μm gate length and 50 μm substrate thickness is developed using E beam gate process. This pHEMT channel is made up of InGaAs material. Its maximum biasing voltage is 4V. It has high transition frequency (fT) of 130 Ghz. NF offered by this HEMT is competitive with other HEMT's. At 40 GHz frequency range this pHEMT offers a low NF around 1.5 dB and high gain of 9 dB. Due to these better features of 0.1 μm GaAs pHEMT, it is highly recommendable in designing LNA at 40 GHz range.

III. DESIGN METHODOLOGY

Various steps of designing a LNA are

Step 1: The main parameters for LNA design are gain and noise figure (NF). Based on the specifications of the LNA appropriate HEMT has to be selected as the main amplification device.

Step 2: Check stability of the HEMT and stabilize if necessary. If the HEMT is unconditionally stable then there is no need for stabilization.

Step 3: At the operating frequency, constant NF circles and constant gain circles need to be plotted to make trade off between NF and gain. After that find the source impedance.

Step 4: Design the Input matching network (IMN) and Output matching network (OMN) while simultaneously checking for stability.

Step 5: If the design does not meet the required specifications then reoptimize it using step 4 until it meets its specifications. Step 6: Design and insert the bias networks such that it does not affect the stability and RF performance.

Step 7: Using the design from previous steps, design layout for the LNA

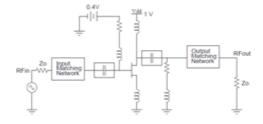


Fig. 1. Schematic of SSCS with source degenerated with inductor LNA

Schematic of SSCS with source degenerated with inductor is shown in Fig. 1. PP10-10 technology 0.1 μm GaAs pHEMT of 50 μm *2 fingers is selected as active device. DC bias of 0.4 volts given at the gate and drain is supplied with 1volt.



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Transmission line is used as inductive degeneration. Input, output matching networks are improved in such a way to match input and output impedance of 50 ohms.

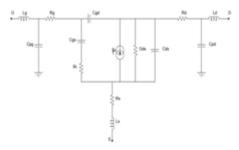


Fig. 2. Small signal equivalent schematic diagram of SSCS inductive degeneration LNA

The small signal equivalent schematic of SSCS configuration with inductive degeneration is shown Fig. 2. Where C_{gd} is gate to drain capacitance, C_{gs} is gate to source capacitance, C_{ds} is drain to source capacitance. Lg, Ld are inductors connected at gate and drain. Ls is source degeneration inductor. Rg, Rs, Rd are the gate, source and drain resistances of the HEMT respectively.

NF of the SSCS degeneration topology is given in [5] expressed by (1).

$$F_{cs.ind} = 1 + \frac{Rlg}{Rs} + \frac{Rg}{Rs} + \frac{\gamma}{\alpha} \frac{x}{Q_l} \frac{w_o}{w_T}$$

$$(1)$$

Where R_{lg} is the effective resistance of the Lg, and Rg, Rs are gate and source resistances respectively. Bias parameters are γ and α and $W_o,\ W_T$ are the operating and transition frequencies respectively. Q_l is the HEMT used in designing a LNA

From the equation (1) it can be observed that by reducing the values of Rlg, Rg low NF can be obtained but it deviates the input matching impedance. This problem is compensated by source degenerative inductor which gives good stability and good tradeoff between NF and gain.

IV. SIMULATION RESULTS

EM simulations are performed on SS LNA with Keysight ADS Momentum Microwave. EM model is developed for the entire circuit barring the active device.

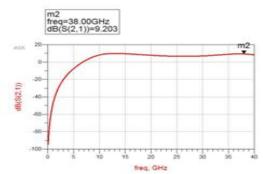


Fig. 3. Gain of 38 GHz SS monolithic LNA

EM simulated gain of LNA at 38 GHz is shown in Fig. 3. Proposed LNA obtained the gain of 9.2 dB at 38GHz. This gain is relatively high compared to the other SS LNA's [2, 6] designed with HEMT technology around 40 GHZ.

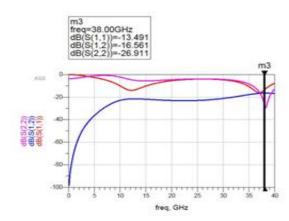


Fig. 4. Input, output return losses (IRL, ORL) of 38 GHz SS monolithic LNA

Simulation results of IRL and ORL of the proposed LNA at 38 GHz are reported in Fig. 4. This proposed LNA obtained the IRL of -13.49 dB and ORL of - 26.91dB. Proposed circuit shows better output return loss compared to [2].

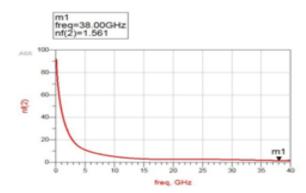


Fig. 5. NF of a 38 GHz SS LNA

Simulated results of NF of the proposed 38 GHz LNA are reported in Fig. 5. This proposed LNA Obtained a very low NF of 1.5 dB. This NF is very low compared to the other SS LNA's designed with HEMT technology as well as CMOS technology around 40 GHz frequency.



Fig. 6. Layout of a 38 GHz SS monolithic LNA

SS monolithic LNA layout is reported in Fig. 6. Its chip size is of 1.3*1.1 mm². In the layout diagram the circle shapes represent the spiral inductors and rectangular bars represent the matching networks. This work occupies less chip area compared to [2, 3].



Table- I: Comparison table

Ref	Technology	Frequency	Gain	NF	IRL	ORL	Power	Chip
					(dB)			size
		(GHz)	(dB)	(dB)		(dB)	(mw)	(mm^2)
[1]	0.25μm HEMT	43	11.5	7	-	1	1	-
[2]	0.1 μm InP pHEMT	44	8	2.5	-15	-15	5	1.5*1.4
[3]	CMOS	24	7.5	3.2	-16	-30	10.6	1.5*1.3
[4]	0.18µm CMOS	5.5	10.02	3.05	-	-	10.8	-
[6]	0.12 μm GaN HEMT	33-41	7.5	3	-	-	140	0.7*1
This work	0.1µm GaAs pHEMT	38	9.2	1.56	-13.4	-26.9	6.6	1.3*1.1

Proposed SSCS 0.1μm GaAs pHEMT LNA compared with the other designs of SS LNA's of HEMT and CMOS technologies in Table -I. [1] with 0.25 μm HEMT technology obtained better gain but high NF compared to the proposed work. [2] designed with the 0. 1μm InP pHEMT obtained only better input return loss compared to the proposed work but it has low gain, high NF, low output return loss. [3] designed with CMOS technology shows better performance in terms of IRL and ORL but it offers low gain and high NF compared to proposed work. [4] developed with 0.18μm CMOS technology obtained better gain but with a high NF. Proposed work shows the better performance compared to [6]. Finally our proposed work gives better NF compared to state of art in Table-I.

V. CONCLUSION & FUTURE SCOPE

Design of a SS 38 GHz LNA using 0. $1\mu m$ GaAs pHEMT is demonstrated. EM simulations are performed and results are verified. Designed LNA is suitable for satellite communications. This LNA with inductive source degeneration shows the better NF performance compared to the state of art. This SS LNA achieved the gain of 9.2 dB, low NF of 1.5 dB and low ORL of -26.9 dB.

FUTURE SCOPE

This SS LNA can be extended to larger number of stages to achieve high gain and low NF. Even though number of stages increased, cascading the stages does not change the NF because of friss criteria.

REFERENCES

- Saito, T., Oohashi, Y., Kurihara, H., Hirachi, Y., Kasuga, T., & Miyazawa, K. (1989, June). A cryogenic 43-GHz-band low-noise amplifier for radio astronomy. In IEEE MTT-S International Microwave Symposium Digest (pp. 853-856). IEEE.
- Wang, H., Lo, D. W., Lai, R., Yang, C. C., & Berenz, J. (1995). Cryogenically cooled performance of a monolithic 44-GHz InP-based HEMT low-noise amplifier. *IEEE microwave and guided wave letters*, 5(9), 281-283
- Sun, X., Dupuis, O., Linten, D., Carchon, G., Soussan, P., Decoutere, S., & Beyne, E. (2006). High- Q above-IC inductors using thin-film wafer-level packaging technology demonstrated on 90-nm RF-CMOS

- 5-GHz VCO and 24-GHz LNA. *IEEE transactions on advanced packaging*, 29(4), 810-817.
- Chang, C. P., Chien, W. C., Su, C. C., Wang, Y. H., & Chen, J. H. (2010). Linearity improvement of cascode CMOS LNA using a diode connected NMOS transistor with a parallel RC circuit. *Progress In Electromagnetics Research*, 17, 29-38
- Chang, C. C., & Chiang, Y. C. (2012, November). Low-noise amplifier with 12.1 dB gain and 5.456 dB NF for V-band applications in GaAs 0.15 μm pHEMT process. In 2012 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT) (pp. 16-18). IEEE.
- Sato, M., Niida, Y., Kamada, Y., Ozaki, S., Ohki, T., Makiyama, K., & Joshin, K. (2016, May). Q-Band InAlGaN/GaN LNA using current reuse topology. In 2016 IEEE MTT-S International Microwave Symposium (IMS) (pp. 1-4). IEEE.

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