

# Effective CU Design Based Implementation of a 64-Bit Processor for Signal Processing Applications

P. Anandan, C. H. Mohan Sai Kumar, B. Venkataramanaiah



**Abstract** –The aim of this paper is to design simple and Effective digital control unit for a 64-bit processor core. Proposed idea is implemented in Spartan-III FPGA Architecture. Control unit (CU) directs the operation of the processor to get results. The function of CU is to fetch their instructions, examining them and execute the programs stored in the memory and executing them one after another in Main Memory. The Central Processing Unit (CPU) is the combination of Arithmetic and Logic Unit (ALU) and CU. The CPU receives information from several different elements; they are memory, control path and data path. Control Unit is required to produce the control signals for operating data path at each clock cycle. CU generates instructions to the memory, arithmetic/logic unit and input and output devices. The proposed control unit simulated in Xilinx and implemented in Spartan 3E, achieved less delay compared to existing approaches

**Index Terms** –CPU, ALU, FPGA, RISC, REGISTER, CONTROL BUS.,CU

## I. INTRODUCTION

Generally Control unit is a one part of the main computer hardware. CU fetches instructions of programs from the primary memory to the processor instruction register and, based on this register contents, implements control signals that supervise execution of these instructions. The control signals are transferred to all smaller and larger components of the computer that participate in execution of instructions. The control signals are basically transmitted by the part of the system bus and it is called the control bus. Neenu Joseph et.al [1] designed a technique for power reduction in process and but complex architecture. They are implemented in a 32-bit RISC processor pipelined architecture for high speed application. The Clock Gating(CG) method is key for power reduction in [1]. CG is idea where the clock is blocked to the modules of the core.

Design and implementation of a microprocessor of 16 bit using control unit method, which is micro programmed and implemented on FPGA architecture and it have been presented in paper [2]. POWER dissipation reductions have combined as a main goal in the design of microprocessor, where the primary goal of the method is speed [3].

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Kui YI et.al [4] analyzes MIPS instructions, format of data path, function for decoder and also designed based implementation on CPU RISC instructions format.

Instructions set format of all MIPS is 32-bit indicated instruction set and instruction address is word implemented justification. There are 3 instruction format of MIPS, one is I-format, second one is R-format and last one is J-format. Here I represents Immediate, R represents Register and J represents Jump [4].

The Design of memory and bus architecture based Digital Signal Processor is implemented by optimization of speed of the processor [6]. Data and Address instructions are forwarded to the sequencing section and numeric section of the Digital Signal Processor when clock cycle presents [7], here no complexity in architecture, but speed is overhead. And also everything is the design targets on speed, area and also throughput. To implement specified focus on all factors in one perspective, Harvard architecture is used, here memory is divided into separate programs and data memory for applications [7]. FPGA receives upgrades in the VLSI design and verification field, and also with an ASIC impossibility [9]. This idea can aid the verifier as well as designer to perform the processes faster than existing. In addition to this literature, design of effective digital filter is implemented on FPGAs, it allows higher sampling rates than existing rates and which is available from conventional DSP cores and advantage is low cost [10]. M. Krishnan [11] proposed digital architecture multiplier based on VHDL. Customized Digital signal processor based architecture is proposed by . Gupta and Anand [12]. Holger Bock et.al [13] proposed quantum arithmetic based Arithmetic and logic unit for central processing unit.

## II. ARCHITECTURE OF CONTROL UNIT

The basic architecture of the effective digital control unit is designed for embedded and real time applications and it is shown in below figure 1. Here the control unit produces control signals that are required to control, managing among the elements of the core. CU produces and controls operations related to read and write. Instructions are related to the register as well as memory. CU is also responsible for producing signals, which takes decision related to ALU usage and other elements for processing. CU is responsible for generating corresponding branch related flags that are utilized by the BU.

The ALU implements arithmetic and logic operation, which take results from the processor core. These operation results will have one or two operands, operand values fetching from the register or from primary memory or from the immediate operand value directly from the instructions. ALU operations include Arithmetical and logical operations. Arithmetic operations are classified as Add, Sub, Compare and decrement.



Logical operations are classified as AND, OR, NOT, NAND and NOR. The ALU output transmitted either to the memory or a Multiplexer (MUX) send back to the registers. MUX is designed, implemented and performed in a single cycle. Here all operations related to ALU will carried according to the signal comes from ALU block. The Function of CU is to generate signals to the ALU, which provides the operations that the ALU will perform. ALU unit input is the five-bit op-code and the two-bit field function of word format instruction.

CU utilizes specified bits to take the correct data, which is used to control the signals to the ALU element parts, this operation cannot be used for ALU. At this point has various control signals, which forwards the particular data; it is produced by elements of ALU or data read from data memory to the registers and also to be write into the specified register. The PC retains the address of memory of specified operation of the current instruction. Whenever instruction is performed in ALU element, then the PC advances to the next instruction and to perform next task. The program Counter (PC) is reloaded with the the next instruction address directly if branch instructions exist. The CU retains the PC values to the address of register, output value which is the new address in specified bus for address. Instructions from the memory are being fetching by PC and stored in Registers The Instruction Register format has 16 bits. The primary four bits contains op-code; the secondary 4 bits are Register address, they are the least significant bits (LSB), as per addressing modes which represents either memory address operand or immediate operand. Register is used for storing short term information

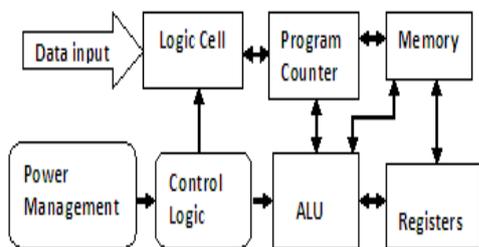


Fig. 1 Architecture of Control Unit

Control Logic function is to skip unnecessary operations and reduce complex operations into the simple operation so that the power and delay of the entire architecture of the control unit can be reduced. The memory plays an important role in this design. Memories are effectively used for storing purpose of core. Memory here is used for storing long term information. Normally storing of information from element is two types, they are data related information as well as program related information. To perform desired function a sequence of program instructions are made from elements. The input and output values are represented by data, which is transferred by PC. Main Memory is used for storing data as well as instructions. The data storing into main memory is called writing and process of receiving data or op-code from the main memory is called reading. The specified memory location is indicated and then reading or writing is to be implemented.

The multiplexer is combination circuit which accepts the selection of any one input from n-different inputs, each input indicates operation function. Select lines from multiplexer are to find out which input signal is activated and transmitted to the output of the MUX.

III. IMPLEMENTATION

The Control Unit is implemented using VHDL on FPGA Family in Xilinx Platform shown in below figure 2. Top Level Control Block with input and output signals is shown in figure 2.

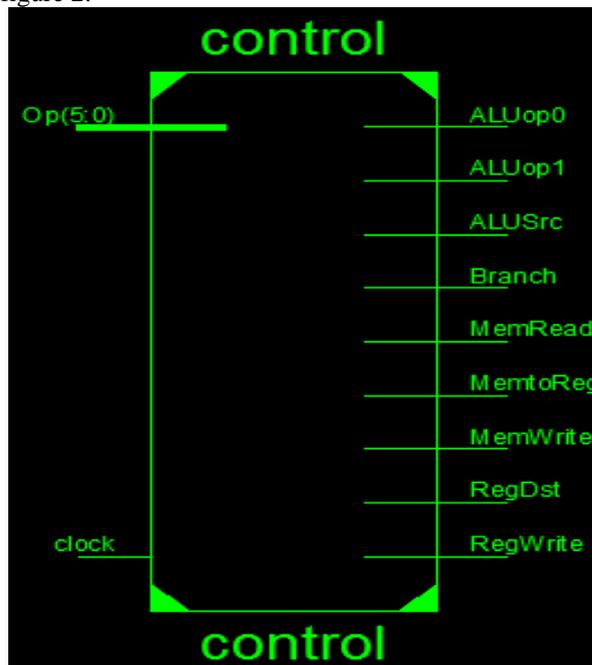


Fig. 2 Control Unit Block.

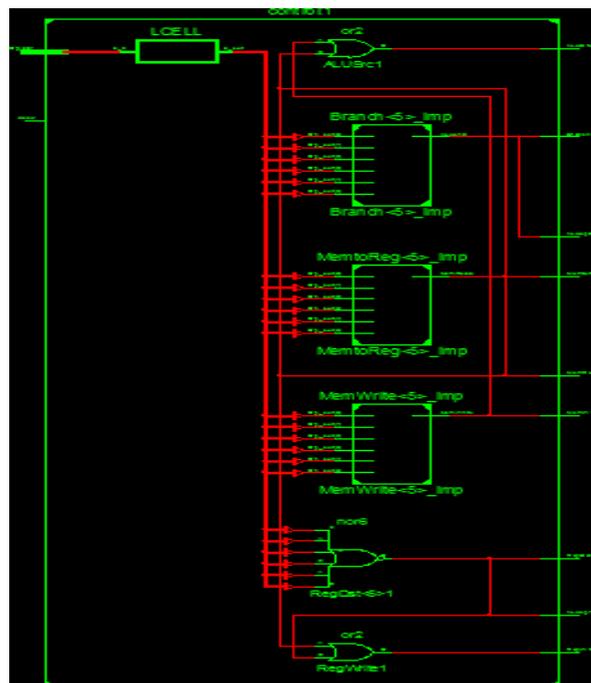


Fig. 3 RTL schematic of Control unit

Control unit is sequential circuit which depends on clock signal. Control unit output shows various operations, which includes Branch, Memory write, Memory read, Register write, Register destination and ALU operations. Operations will be performed by based on opcode. RTL Schematic of Proposed Control Unit is shown in below figure 3. RTL schematic is also analyzed with VLSI Tool.

IV. RESULTS

The architecture of Proposed is implemented in Xilinx platform on Virtex4 FPGA device by using VHDL. The TLM with input and output of Control unit is also shown in figure 4. The performance of the proposed control unit is determined in terms of efficient resource usage in terms of Look up Table's, Number of I/O Bonds and Number of used registers. Simulation results shows that Reduction of Power, Delay of Proposed control unit has been achieved

Table 1.Comparison of Device Utilization Parameters Control Unit

Parameter	16 bit control unit	Proposed control unit
Number of slice LUTs	69	6
Number of bonded IOBs	91	15
Number of LUT Flip Flop	24	6
combinational path delay	8.549 ns	1.559ns

TABLE 1 is the comparison of various parameters indicates Number of slice LUTs, Number of bonded IOBs, Number of LUT Flip Flop, and combinational path delay are specified. Proposed Control unit achieves better results compared to 16 bit control unit. Proposed architecture has achieved less hardware utilization compared to other control units design

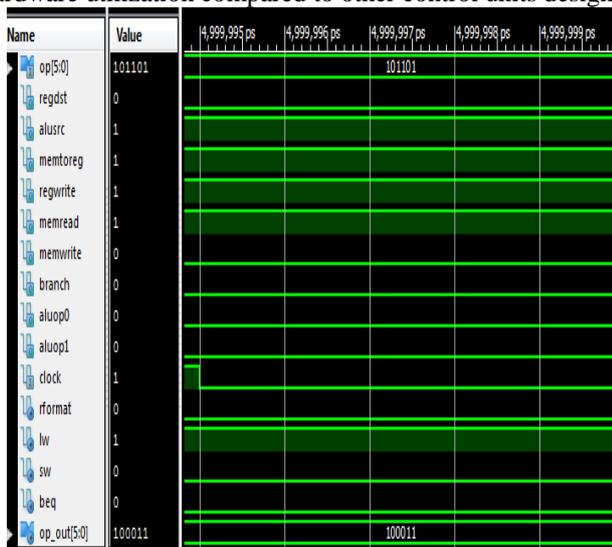


Fig 4. Top Level Module (TLM) timing diagram of control unit

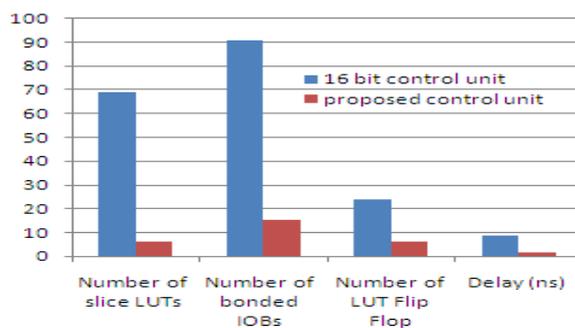


Fig 5.Comparison of Parameters for Control Unit

The comparison of different parameters related to Control Unit signals are shown in the figure 5.The Combinational delay for the proposed control unit is Minimum. Proposed Method has less Device Utilization Compared Previous Method.

V. CONCLUSION

Control unit of 64 bit processor has been designed and implemented in hardware on Xilinx Spartan FPGA. The design has been achieved using VHDL and simulated with Xilinx. Diligent Spartan 3E development board has been used for the hardware part. Expected goals of proposed idea are achieved and simulation shows that the Proposed Control unit has less path delay and it is effective than other approaches. Synthesis estimate analysis has been analyzed from results, the minimum clock period has been achieved in proposed CU architecture and the combinational path delay is 1.559 ns.

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