International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-3, January 2020

Design of Class D Audio Power Amplifier Suitable to Hearing Aid Devices

P.Devi Pradeep, A.Kamala Kumari

Abstract: ***An amplifier is an electronic circuit that improves the strength of the signal. Using an amplifier in an audio system is essential to improve the strength of the signal. Based on different applications and specifications different types of amplifiers are used. Generally in an audio system, the input signal is amplified to a minimum required power level and then the speaker is driven by it. Conventionally, the output stage of an audio amplifier uses Class-A or Class-AB operating in a linear transfer region. The power efficiency of the Class-D amplifier has a better output efficiency compared to Class-A and Class-AB amplifiers, and its distortion is lower than that of the Class-C amplifier. This is based on a known fact that the Class D amplifier has a switching action in which the transistors are either completely on or off. As a result, the amplification is achieved with no power dissipation. Hence, the size of the amplifier can be highly reduced and a smaller heat sink is required. This paper focuses on designing a Class-D power amplifier which is suitable for hearing aid devices to deliver 500mW output power and for the THD to be less than 3%. The circuit implementation is done using UMC high voltage 0.18µm technology. This amplifier consists of three stages such as the modulation stage, the driver stage, the bridge stage, and the demodulation stage. Unfortunately, the Class-D power amplifier has inherent non-linear distortion problems, which is more significant than conventional audio power amplifiers. In this thesis, negative feedback is employed to reduce THD. Without feedback, the THD is obtained as above 3%. By employing feedback, the THD was reduced by 1.96dB. This design result is discussed and through to realization; whereupon the effectiveness of each of the implementation is evaluated.***

Keywords: Amplifier, Class A, Class B, Class D, Distortion, THD

I. INTRODUCTION

Power amplifier based on the Class-D topology was introduced in the year 1958. Recent advances in integrated technology made significant changes where the large circuit audio amplifiers are converted to a simple integrated circuit. Class D amplifiers are preferred to class AB because of two main advantages. The first advantage is the efficiency of Class D is better than all other types of amplifiers due to this the power required to drive will be reduced and the heat dissipation also gets reduced. The second advantage is Class D provides PWM output whereas Class AB provides continuous output. These are the two advantages that makes the Class-D power amplifiers attractive to consumer electronics, such as portable devices like CD player, MP3 player, mobile phone, LCD-TV, PDA, etc.

Revised Manuscript Received on January 30, 2020.
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The paper is mainly aimed at the design of high efficiency audio power amplifier suitable to hearing aid devices. This involves study of different architectures to meet the requirements efficiency greater than 90% total harmonic distortion should be less than 1.5%.

A. Audio Amplification

Audio frequencies are having a range of 20 Hz to 20 KHz. Human ear can sense the signals in this range. Voice signals are having a range of 300Hz to 3500 Hz. Therefore, all voice signals can be heard but all audio signals cannot be reconstructed by a human. The figure shown below is the block diagram of audio amplifier. First the voltage is amplified and then the power is amplified to the required level.

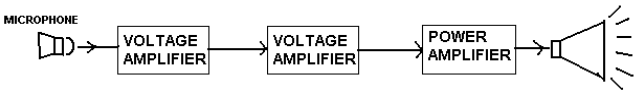

Fig1: Block Diagram of an Audio Amplifier

B. CHARACTERISTICS OF CLASS D AMPLIFIER

The theoretical efficiency of Class-D amplifier is 100%. Thus we assume that they are 'ideal' switching. In practical such ideal device or component does not exist. Hence, losses must be considered in the switching power amplifier.
The device has a high voltage and no current across its output terminal during turn-on instant. The voltage slowly starts falling from its initial value and the current starts rising towards its final value. There will be a crossover period in which both the current and the voltage are non-zero if this voltage fall is not instantaneous. During this time, large amount of energy can be dissipated. The power dissipated during this process is proportional to the crossover period and also to the switching frequency as the energy loss occurs every switching cycle [11].

II. PROBLEM DEFINITION AND CHARACTERIZATION

The hearing impaired people will take the help of hearing aid devices to lead a comfortable life. Also this was addressed in audiology. Presently the sophisticated hearing aid device is operated in analog and digital modes.

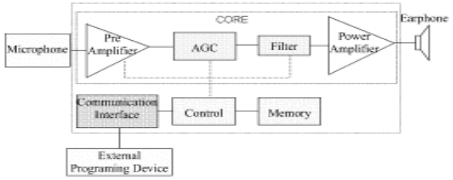

Fig2: Block Diagram of a Programmable Hearing Aid Device

The pre-amplifier is the first stage of the block diagram shown above. It provides voltage gain for low intensity electric signals which comes from the microphone. The next stage is the automatic gain control unit (AGC) which is used to maintain a constant level of output. If the electrical signal is too weak then it brings to the reference level and if the electric signal is too high then it clamps it to the reference level. The next stage of the programmable hearing aid device is the filter. Here the filter is used to allow only the required frequency levels and blocks the other frequencies thereby giving a good response of the system. The last stage of the programmable hearing aid device is the power amplifier. The power amplifier is used to increase the strength of the signal in terms of power to drive the loads like speakers.

The power reduction in ICs is a challenging aspect when technology enhances. In devices like mobile phones the battery should be small in size but the power to run the device will be huge. With limited energy in reasonable sized battery, minimum power dissipation in integrated circuits is necessary. If there is more power dissipation, then the battery life will get reduced and also we need large heat sinks to reduce the heat generated. In portable devices such as mobile phones, notebook PC's, laptops, PDA etc power amplifiers are the major power consuming devices, hence power dissipation in these audio power amplifiers have to be reduced i.e. power efficiency has to be increased and achieve high quality in small size. This motivated me to design a high efficiency audio power amplifier for cell phone driving a speaker of 500mWatts power output.

The input is given to AC'97 Audio Codec which enables to drive low-impedance speakers. Equalization is performed to improve the speaker fidelity by electronically flattening its response. This can be achieved either with analog techniques using operational amplifiers or digitally with an equalization device. There are two sets of inputs; one set of input can be connected to the audio codec while the other can be connected to the analog output of the CD-ROM.

As we are dealing with audio signals, the output signal shape i.e. audio signal output from the speaker and the input signal shape must be same. It means that our audio amplifier should have good linearity, i.e. it must have low distortion. The main distortion that occurs here is harmonic distortion; hence we have to design audio power amplifier with less than 3% THD. The frequency range of the input audio signal will be in the range of 20 Hz to 20 KHz as mentioned earlier. The input of the audio power amplifier is given as the output of the audio codec. The AC'97 V2.3 of INTEL gives general description of the audio codec for portable applications where it was given that the typical output voltage from audio codec to the headphone output line is 1V rms [4]. Hence, the peak-to-peak input signal voltage for our amplifier is 2.8V. Impedance is an important parameter used to characterize electronic circuits. Impedance is defined as opposition of current in a circuit for a given voltage as input. It is denoted by Z. This opposition comes from the passive components like resistance, capacitive reactance and inductive reactance due to the alternating current. Reactance varies with the frequency of the alternating current [17].

Here the output is designed to drive three types of loads: line-level, headphones, and speakers. Output designed for line-level usually has minimal drive capability and the load is set above 40 KΩ. Headphone impedance varies from 16 Ω to 92 Ω with 32 Ω being the most common. Speaker impedance is typically 8 Ω.

SPECIFICATIONS:

Output power:	500mW per channel
Load impedance:	8 Ω
Power efficiency:	> 90%
THD+N:	< 3%
Input signal range:	$2.80V_{p-p}(1.65 \pm 1.4V)$
Input signal frequency:	20 Hz to 25 KHz
Supply voltage:	3.3V
Temperature range:	-55^{o}c to $+125^{o}$c

SELECTION OF ARCHITECTURE:

Efficiency and total harmonic distortion are the two main factors to be considered in the selection of the architecture.

As none of the linear amplifiers have efficiency greater than 90% except Class C. But in Class C power amplifier, we will get output signal for less than 50% of the input signal, hence it is not used for audio.

The specifications we require i.e., high efficiency and low distortion are provided by class D switched mode power amplifier

Class D amplifier characteristics are reflected mainly in mobile phones. Two main characteristics are- (a) they are battery powered, (b) they suffer from thermal problems due to heat dissipation. The runtime of batteries can be improved by using a class-D amplifier.

The processor power dissipation increases with decrease in structure and at a certain point, the ambient temperature will be too high which leads the Class-AB amplifier to fail. Hence we have chosen Class D power amplifier architecture for our audio power amplifier implementation.

III. DESIGN AND IMPLEMENTATION

Basic Architecture of Audio Power Amplifier

The above figure shows the block diagram of the Class-D audio power amplifier. It is divided into three stages namely PWM generation stage, output stage and low pass filter stage. Design and implementation of each stage is explained in the following sections.

Carrier signal generator

Carrier signal generator is one of the integral parts of the pulse width modulator. Comparing the input signal with saw tooth waveform would control duty cycle. In a fixed frequency PWM using a saw tooth waveform the switching decision is made once for every switching period based on the control signal level and the time instant of decision.

The second switching action is taken due to the clock pulse at the beginning of the saw tooth. The first one is influenced by the control signal whereas the latter is not. Thus, the duty cycle is improved according to the single control signal sample per cycle.

In this design, a ramp signal is used as a carrier signal rather than a triangle wave. A comparator switches twice per cycle of a triangular carrier signal whereas the comparator switches only once per cycle of a ramp carrier signal.

Hence in the latter the number of switching transitions is reduced by half, and the dynamic power consumption of the H-bridge inverter is reduced by half. Generally carrier frequency must be 3 to 10 times the audio frequency the reason behind this is tradeoffs between performance and component size if greater than 10 times distortion increases and efficiency decreases. [6]

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Ramp generation is done using the following methods:

1st method: The circuits shown in figure 3 functions as a ramp generator. When the pulse input of M_2 is low, M_1 and M_2 are on and off respectively. During this period the capacitor 'c' charges linearly to V_{dd} through the resistive path of M_1.The V-I relationship of a capacitor is

$$V = \frac{1}{C}\int_{-\infty}^{t} Idt \qquad \text{---- 4.1}$$

As per the above equation, the voltage across the capacitor increases linearly if current through the capacitor is constant. This condition is ensured as long as M2 is in saturation mode of operation.

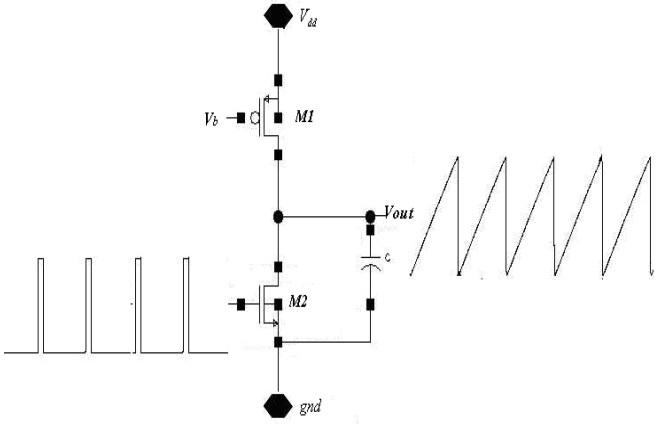

Fig3. Ramp Generation

When the pulse input of M_2 goes high, both M_1 and M_2 are on. The $\frac{W}{L}$ ratio of M_2 is chosen relatively larger than M_1 so that M_2 forms a lower resistive path than that of the M_2. Subsequently, the capacitor 'c' discharges through M_2

The constant current that M_1 has to source to the capacitor in order to generate a ramp ,voltage across the capacitor is given by

$$\text{I} = \text{C}\frac{dv}{dt} \qquad \text{----------} \qquad 4.2$$

In this design, it is desirous to generate a ramp waveform whose frequency is 250KHz.This corresponds to a period of 4000ns.The charging time is chosen as 3950ns and the discharging time is chosen as 50ns.The value of the capacitor 'c' is chosen to be equal to 1.1pF, and from equation ---, for a ramp voltage of 1.8volts and charging time of 3950ns, the constant charging current, I is 0920 μ A. The maximum value of the output ramp is equal to $V_{dd} - V_{dsat,M1}$.

The aspect ratio of M_1 is determined from equation 4.3

$$I_d = \frac{1}{2} k_n' \frac{W}{L} (V_{eff})^2 \qquad \text{----------} \qquad 4.3$$

Where I_d = 0.920 μ A

V_{eff} = 50mV

k_n' = 40 $\mu \frac{A}{V^2}$.

The aspect ratio of M_2 is chosen comparatively larger than the aspect ratio of M_1 so that M_2 forms a least resistive path during the ON period of the pulse input. Subsequently, the capacitor 'c' discharges through M_2.

2nd method: Ramp signal generators in specific critical in controlling the duty cycle and frequency of pulse width modulated switching pulses. Ramp generators are designed using the Op-Amps and diodes. The diodes are connected in an opposite fashion such that the signal will not be decayed. Thus the circuit maintains a constant slope through-out its operation. [2]

Conventionally method to generate ramp signal, after an initial reset event, a capacitor is slowly charged with charge current I_{chg} until the capacitor voltage (ramp) reaches upper limit V_H in below fig 4, at which point the comparator trips and quickly resets the ramp to ground with low resistance switch S_{dchg}, marking the beginning of another cycle. The below diagram shows the conventional ramp generator.

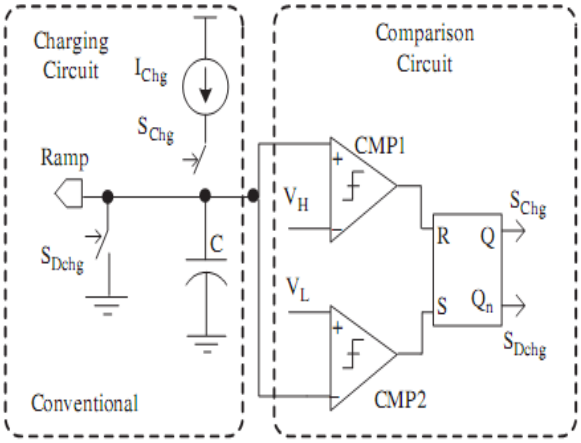

Fig.4. Conventional Ramp Generator

Pre-Amplification

For the pre-amplification stage shown in Fig.5, we choose differential amplifier with active loads. Typically, a differential amplifier with a diode connected load can give a dc gain of 20dB. It is sufficient to design a preamplifier with a dc gain of 10dB. In order to get a low propagation delay the parasitic capacitances should be eliminated as far as possible. In order to reduce parasitic capacitance the lengths of transistors are chosen to be minimum, equal to 340nm.

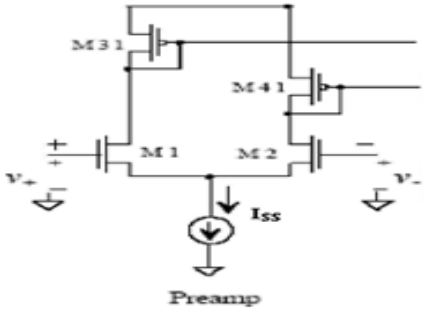

Fig .5.Pre-amplification stage

The DC gain of the pre-amplifier shown in the figure 6 is given by,

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$$A_v = g_{m1}(r_{o1} \parallel g_{m31}) \approx \frac{g_{m1}}{g_{m31}} \quad \text{-------} \quad 4.5$$

Considering the dc gain of the preamplifier is supposed to be 10dB, the aspect ratios of M_1 and M_{31} is chosen from equation 4.5.

Decision Circuit

The decision stage circuit used in comparator is shown in the Fig 6. This circuit is connected in positive feedback to increase the gain of the decision circuit. Now the gain will be increased but the stability will be reduced due to positive feedback.

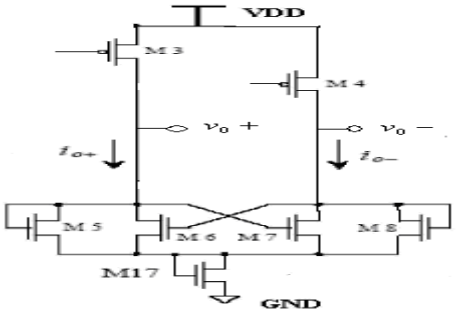

Fig.6. Decision stage

Referring to figure 6, if v_+ is larger than v_- then i_{0+} is greater than i_{0-} .In the parallel combination of M_7 and M_8, M_8 being a diode connected load forms the least resistive path. Hence most of the current i_{0-} is drawn by M_8. As i_{0-} decreases the gate to source voltage of M_8 reduces. As a result the switching takes place when the drain to source voltage of M_7 (V_{gs} of M_8) is equal to V_{THN} of M_6.When V_{gs} of M_8 equals V_{THN}, M_6 and M_8 are completely off. Hence currents i_{0+} and i_{0-} flow into M_5 and M_7 respectively. One can assume that $\beta_5 = \beta_8 = \beta_A$ and $\beta_6 = \beta_7 = \beta_B$ under these circumstances, v_0- is approximately 0v and v_0+ is

$$V_0+ = \sqrt{(2 * i_0+)/\beta_A} + V_{THN} \quad \text{--------} \quad 4.6$$

Output Buffer

The complementary outputs of the decision stage are not at supply rails. v_0- is approximately 0volts and v_0+ is given by

$$V_0+ = \sqrt{(2 * i_0+)/\beta_A} + V_{THN}$$

The next stage of decision stage is post amplifier. The output of decision stage is the input to post amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a digital signal which is obtained by using ADC. In other words the output buffer maintains the output levels at V_{dd} and GND. The output buffer used in this paper is the Complementary Self-Biased Differential Amplifier (CSDA) [10].

The CSDA (Complementary Self biased Differential Amplifier) is chosen as it includes both self-biasing and fully complementary configuration. Below figure shows two conventional CMOS differential amplifiers, in which one is the complement to the other. First, the amplifiers are selected without loads. After that the input pair drains are connected one another. Final configuration which is completely complementary and externally biased is shown in Fig 7.

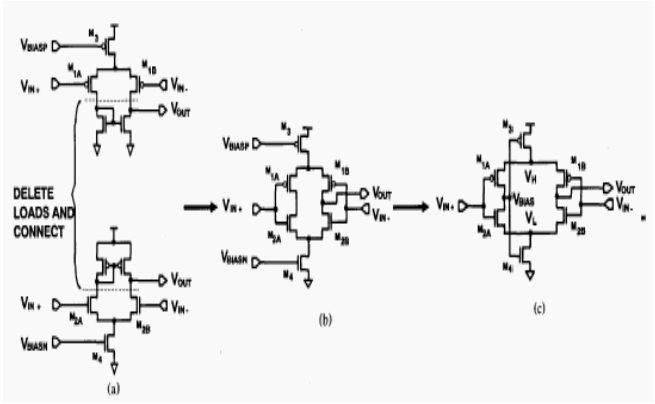

Fig.7. Derivation of CSDA

The circuit shown in Fig 7(b) cannot be biased in a stable fashion. The currents through the devices M_3 and M_4 should be equal so that the circuits are said to be biased in stable but making the two currents equal is impractical due to different noise parameters. So, the circuit in 7(b) should be modified slightly. The modified circuit is shown in fig 7(c). Bias-voltage inputs are connected to the internal amplifier node V_{bias}. As a result of this self biasing, the negative-feedback loop is formed and due to this the stability in voltages is achieved.

The devices M_3 and M_4 are operated in the non saturation region. As a result, the voltages V_H and V_L, are approximately equal to the supply voltages. The output swing will be the difference between the supply rails this provides a large margin for variations in the logic threshold of the gates. Another situation is operating the devices M_3 and M_4 in non saturation region. The output currents that are much greater than its quiescent current are provided by CSDA whereas, these output currents are set by the current-source device, which operates in the saturation region. This capacity of supplying momentarily large output current pulses makes the CSDA suitable for high-speed applications. By reducing the time constant value the charging and discharging of capacitors is made increased so that the operation speed gets improved.

The dc differential mode gain is almost doubled (+ 6 dB) because the fig 7c has four amplifiers while fig 7a and 7b have two amplifiers only. Therefore, differential-mode gain A_d, of the CSDA is given by

$$A_d = \frac{g_{m_1} + g_{m_2}}{g_0} \quad \text{----------} \quad \text{eq}$$

Where g_{m1} and g_{m2} are the trans-conductance of devices $M_{1A\text{-}B}$ and $M_{2A\text{-}B}$, respectively, and g_0 is the output conductance of the amplifier.

The next stage of output buffer is inverter. Inverter is added because to improvise the gain. Observe a problem in connecting the decision circuit directly to the output buffer. To shift the output of the decision circuit M_{17} is added in series with the decision circuit to raise the average voltage out of the decision circuit.

Retrieval Number: B7327129219/2020©BEIESP
DOI: 10.35940/ijitee.B7327.019320
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4.4 Level Shifter Design:

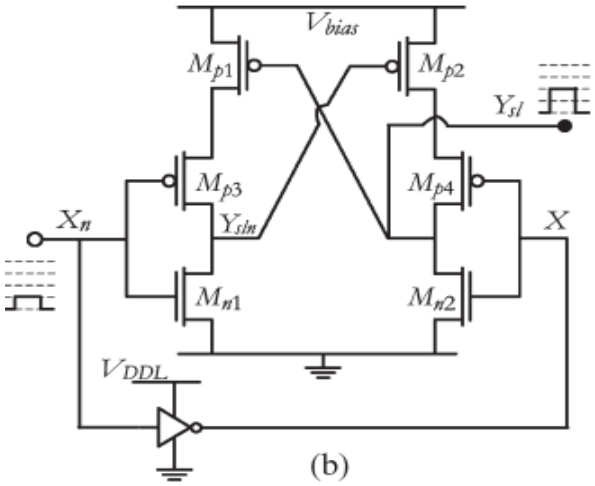

Fig.8. Level shifter circuit diagram

Level shifters are used to maintain proper driving capability and are helpful when transition of signals occurs. Level shifters are placed near the power rails.

Input applied at Xn is high. As Mp3 puts off and Mp4 puts on then the signal at X will be low. As Ysln is low it puts on the transistor $M_{p2.}$ As a result the output appears at Ysl. This output makes the capacitor to charge till Vbias. Voltage like than if input is at high 1.8 v and our bias is 3.3V then output will be 3.3V like that for input low 0v output node charges to 0V only.

The signal processing depends on the low voltage logic. However it is compulsory to impose a constraint, forcing the HV buffer Output value to 0 or 10 during out of the normal mode periods (power-down, power up, reset…etc).

4.5 Output Stage Design

The H-shape arrangement of four MOSFETs is required for this design, with the load in the center, providing a bridged output. The MOSFET is selected based on the following: requirements of peak voltage and current, reverse-recovery time of body diode, switching and conduction losses. The rating that the MOSFET is able to sustain is determined by peak voltage and current requirements.

In the Class-D amplifier the largest source of power dissipation is The H-bridge as it provides power to the speaker load. The current flows through the load are dependent on the sum of the transistor's on resistance (R_{ON}) and the load resistance since the transistors of the H-bridge operates in the triode region. The efficiency of the H-bridge is also dependent on the relative size of R_{ON}.

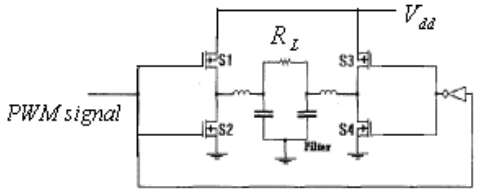

Fig.9. A full bridge output driver

The larger R_{ON} gives higher power dissipation in the transistors, results reduction of efficiency of the amplifier. 3.3V power supply would give more power driving capability for given sizes of device, so choose to use it for the H-bridge [7].

$$Efficiency = \frac{\text{speaker\_power}}{\text{speaker\_power} + \text{IC\_power}} \times 100\% \quad \text{----------} \quad 4.8$$

From the above equation the power dissipated at the chip must be less than 50mW to achieve 90% efficiency. Let us assume the power dissipated in power transistors is 1mW. In the A bridge-tied load (BTL) configuration, the number of the power transistors is four. So, the dissipation at one power transistor must be 1mW (=0.004/4) or less. The below equation describes the relationship between current and power at output stage.

$$P_0 = I^2 R_L \qquad I_{rms} = \sqrt{\frac{P_0}{R_L}} = 0.25\text{A}$$

$$V_{rms} = 2v \Rightarrow V_m = 2.828v \Rightarrow V_{p-p} = 5.656v$$

$$P_D = {I_{rms}}^2 \times R_{ON} \Rightarrow R_{ON} = 16\text{m}\Omega$$

Here P_d is the power dissipated by one power transistor, R_{ON} is the ON resistance of a power transistor, V_{RMS} is the output RMS voltage, V_{p-p} is the peak-to-peak output voltage and I_{p-p} is the peak-to-peak current. Above equation shows that R_{ON} = 16mΩ . Now, calculate the size of a power transistor from equation below.

$$R_{ON} = \frac{L}{\mu_n C_{ox} W (V_{GS} - V_T)} \quad \text{----------} \quad 4.9$$

For $\mu_n C_{ox}$ = 263 $\mu A/V$, V_{GS} = 3.3V, V_T = 0.43V and L=340nm**,** the width of the power transistor should be at least 28mm for the static power consumption to be lesser than 1mw per transistor.

H-Bridge driver stage

For the static power consumption of the H-bridge transistors to be small the size of the transistors should be as large as possible. As discussed in the previous section, the width of the NMOS transistor should be of the order of 28mm.This large dimension of the NMOSFET channel's width increases the input capacitance.

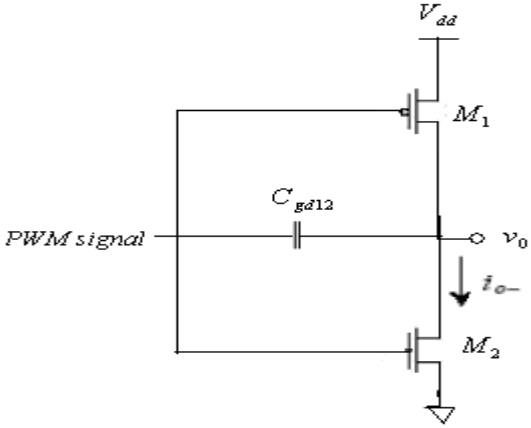

Fig.10. Inverter

The input capacitance, C_{in} is given by

$$C_p = \frac{3}{2} \times w \times l \times C_{ox}'$$

,

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$$C_n = C_p/3 \quad C_{tot} = C_n + C_p$$

For W_n = 30mm, W_p = 10mm, C_{in} is approximately 40pf.

Hence a PWM signal is loaded by a large input capacitance of the H-bridge's inverter. This can increase the comparison time of the comparator, and can distort the PWM signal.

It is desirous to design a circuit to drive large capacitive load of the order of 40pF with as minimum delay as possible. If a single inverter were to drive C_{load}, the delay would be

$$t_{PHL} + t_{PLH} = (R_n + R_p).(C_{out} + C_{load}) \text{ --- } 4.10$$

Cascaded N inverters are used where each inverter is larger than the previous one by a factor A (that is, the width of each MOSFET is multiplied by A). Then a minimum delay can be obtained as long as A and N is picked up correctly. If the load capacitance is equal to the input capacitance of the last inverter multiplied by A, then

Input C of final inverter = $C_{in1}.A^N$ --------- eq 4.11

Where C_{in1} is the input capacitance of the fundamental first inverter. Re-arranging equation 4.11 gives

$$A = \left[\frac{C_{load}}{C_{in1}}\right]^{\frac{1}{N}} \quad \text{--------- } 4.12$$

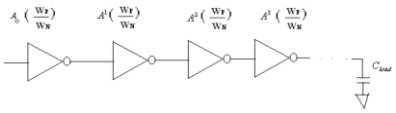

Fig .11. Cascading of CMOS inverters used to drive a large capacitive load

The minimum delay is obtained by choosing N from the equation

N=ln (Cload/Cin1) ---- 4.13

The first inverter in the cascade is sized in such a way that the switching point is at $\frac{V_{dd}}{2}$.The switching point voltage of CMOS inverter is given by

$$V_{sp} = \frac{V_{DD} - |V_{tp}| + \sqrt{\frac{k_n}{k_p}}V_{tn}}{1 + \sqrt{\frac{k_n}{k_p}}}$$

---------- 4.14

where $k_n = k_n, \frac{W_n}{L_n}$ and $k_p = k_p, \frac{W_p}{L_P}$

From the aforementioned equations the input capacitance, C_{in1} equals

$$C_{in1} = C_n + C_p$$

$$= \frac{3}{2} \times C_{ox}^{'} \times (W_n L_n + W_p L_p) = 15\text{fF}. \quad \text{-------- } 4.15$$

From equation 4.13, and for C_{load} and C_{in1} equal to 40pF and 15fF respectively,

N = 8.

From the equation 4.12, A = 2.68

Gate Drive Combinational Logic :

There exists a low resistive path between supply voltages. As it damages the circuit, the path is to be eliminated. So, the combinational logic implies to synchronize the turning ON and OFF of transistors on the same side of the H-bridge.

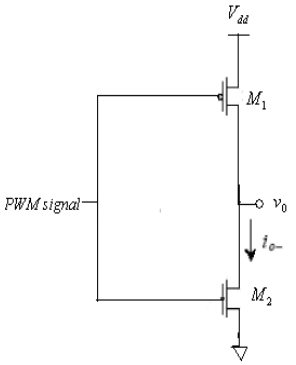

Fig.13. Inverter

Referring to figure 13, during the transition of the PWM signal from low to high and vice-versa, the transistors of H-bridge stage are ON at the same time, forming a rail to ground path. This dynamic power consumption can reduce the efficiency of the power amplifier. This low resistance path results in unwanted wasted power, switching transients and may lead to short circuit and may lead to permanent device failure [20]. In order to avoid the dynamic power consumption a combinational logic is used in conjunction with the driver stage. The gate drive logic is depicted in the Figure 12

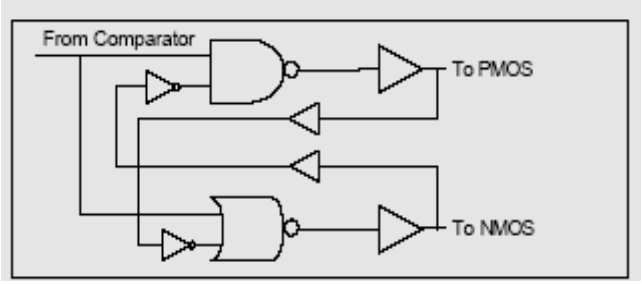

Fig .12. Combinational logic is used to drive both PMOS and NMOS transistors on the same side of the H-bridge.

The motive in designing this block is to make the H-bridge to follow the output of the comparator. When the output of comparator go high then the output of NOR gate goes low which turns OFF the NMOS thereby turning ON the PMOS which in turn makes NAND gate output low. When the output of comparator go low then NAND gate gives a high output which make the PMOS OFF. Delay is provided by the small buffers in the combinational feedback path so that the output of the H-bridge settles before the complementary device is turned on. With this combinational logic, NMOS becomes OFF before PMOS becomes ON and PMOS becomes OFF before NMOS becomes ON. At the same time the two devices being ON is avoided by this logic. Therefore during the transition of the PWM signal the transistors on the same side of the bridge are not ON simultaneously. Hence, the dynamic power consumption is avoided.

Output Filter stage

For this, a low pass Butterworth filter configuration was used. It provides a flat response in the pass band, which is important for the audio system to improve its dynamic performance.

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Also, the parts required will reduce. Since a bridge output is expected, a balanced filter is required for designing this Class-D amplifier. As a result, the LC filter will be designed using a single ended approach. For the second order Butterworth filter the transfer function is:

$$H(s) = \frac{1}{s^2 + \sqrt{2}s + 1} \quad \text{.....4.16}$$

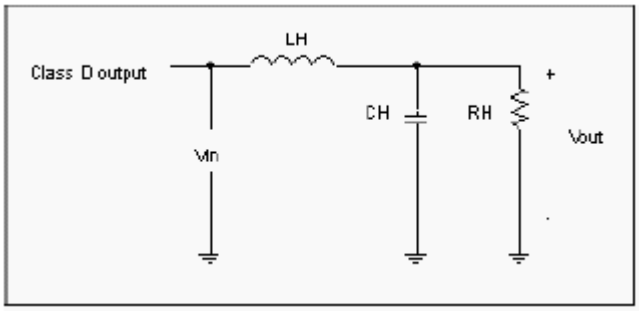

Fig.14.Low pass filter half circuit model

The LC filter is realized using the half circuit model. The transfer function of the output filter is given as:

$$H(s) = \frac{Vo(s)}{Vin(s)} = \frac{\frac{1}{LH \cdot CH}}{s^2 + \frac{1}{RH \cdot CH}s + \frac{1}{LH \cdot CH}}$$

.....4.17

The inductance and capacitance were converted to s-domain (L=Ls, C=1/Cs). The value of the half model inductor and capacitor can be determined by equating the above two equations of H(S), and can be easily converted into full model.

$$CH = \frac{1}{\sqrt{2} \cdot RH} = \frac{1}{2\sqrt{2} \cdot \pi \cdot fc \cdot RH} \rightarrow CL = \frac{1}{2\sqrt{2} \cdot \pi \cdot fcRL}$$

$$LH = \frac{1}{CH} = \frac{\sqrt{2} \cdot RH}{2 \cdot \pi \cdot fc} \rightarrow L = LH$$

.....4.18

The final LC Low Pass Filter is obtained by combining of the two half models as shown in the Fig 15. The final Butterworth low pass equations are combinations of resistors and capacitors.

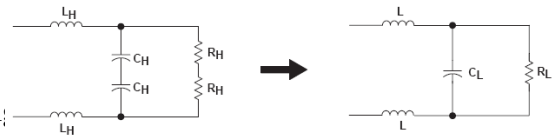

Fig.15. Combination of half circuit models

$$R_L = 2R_H$$

$$C_L = \frac{1}{2\sqrt{2}\Pi R_L f_c}$$

$$L = L_H = \frac{\sqrt{2} \cdot R_L}{2 \cdot w_0} = \frac{\sqrt{2}}{4} \cdot \frac{R_L}{\Pi f_c}$$

The inductor values actually remain the same for the half- and full-bridge circuit since there are two inductors in the low pass circuit. Based on the low pass values ,the –3-dB cutoff frequency for the LC filter, , is

$$f_c = \frac{1}{2 \cdot \pi \cdot \sqrt{2 \cdot LCL}} \quad \text{.....4.19}$$

The above equation indicates the half-circuit model to the full Butterworth low pass circuit, Where '2' in the denominator is the result of transposing the values of L and C .

ANALYSIS OF CLASS D AMPLIFIERS WITH FEEDBACK

A feed forward Class D amplifier, H_{ff} was modeled as an open-loop system as shown in Fig.16. After the feed forward function H_{ff}, we will assume that V_n are introduced, which denotes the harmonic distortion components.

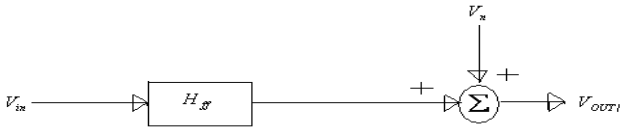

Fig.16. Open-Loop Class D Amplifier model

Since the output is

$$V_{OUT1} = H_{ff} V_{in} + V_n \quad \text{----------} \quad 4.20$$

The THD of this open loop Class-D amp is

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} (V_n)^2}}{H_{ff} V_{in}} \quad \text{----------} \quad 4.21$$

According to closed-loop system depicted below, we can further model the Class-D amplifier.

H_{fb} is the feed forward gain and G is the feedback gain. As we assumed the harmonic distortion components V_n, are introduced in the feed forward path.

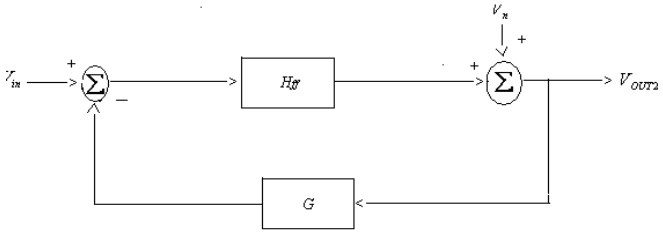

Fig.17. Closed-loop Class D amp model

Output is $V_{out2} = \frac{H_{fb} V_{in}}{1 + H_{fb} G} + \frac{V_n}{1 + H_{fb} G}$ -- 4.22

Forward gain H_{fb} will be included in the closed-loop Class-D amplifier so that the overall gain of both the open and closed-loop systems will be same.

It is given as-

$$H_{ff} = \frac{H_{fb}}{1 + H_{fb} G}.$$

In order to keep both open and closed-loop systems in view, we will rearrange the eqn. 4.21 for easy comparison with eqn. 4.20

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$$V_{out2} = H_{ff} V_{in} + \frac{V_n}{1 + H_{fb} G} \quad \text{----------} \quad 4.23$$

Class-D amplifier with feedback in figure 17 can be shown as

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^{\,2}}}{H_{ff} V_{in} \left(1 + H_{fb} G\right)} \quad \text{--------} \quad 4.24$$

From our derived equations 4.21 and 4.24, we can observe the THD of a closed-loop Class D amplifier. It can be considerably reduced by a factor (1+ H_{fb} G). Hence, it is obvious that the THD can be reduced by designing Class-D amplifier properly with feedback.

PROPOSED FEEDBACK DESIGN FOR A CLASS D AMPLIFIER

The Class D amplifier in closed loop configuration is proposed in this paper as shown in fig 17. The summing device is used to add the input signal and output through the feedback. The difference amplifier with low pass filter is comprised within the feedback network.

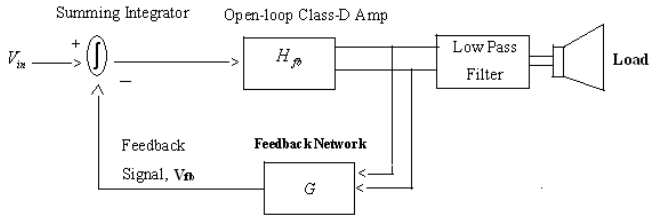

Fig.18.The Proposed Class D Amplifier with Feedback

Stability is mainly achieved only having the proper in the feedback. It can be achieved by making the gain of the feedback network less than unity because if stability is needed we need to sacrifice the gain but gain can be improvised for a stable device (vice-versa is not possible). The high frequency carrier components are attenuated by an integrator, essentially being a low pass filter. The cut-off frequency of the LPF in the feedback loop is chosen to be equal to 25 KHz.

Feedback signal from the low pass filter will make the system to reduce the non linearity and distortions.

IV.RESULT AND DISCUSSION

Here in results the diagrams are described both open loop and closed loop of amplifiers.

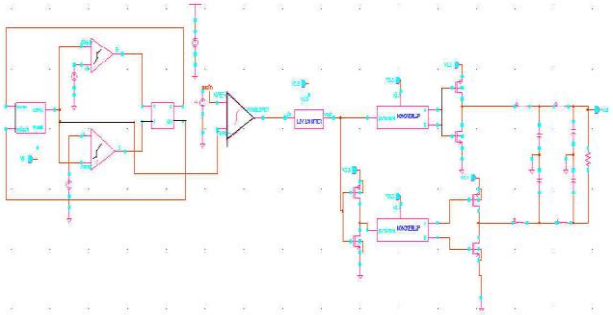

Fig. 19. Schematic of Open loop amplifier

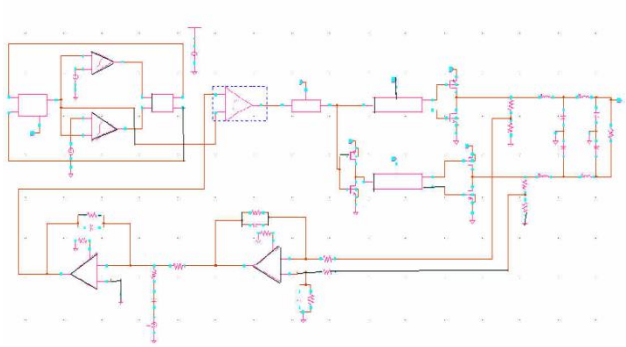

Fig.20. Schematic of Closed loop amplifier

The following diagrams show some of the layouts of the Class D power amplifier.

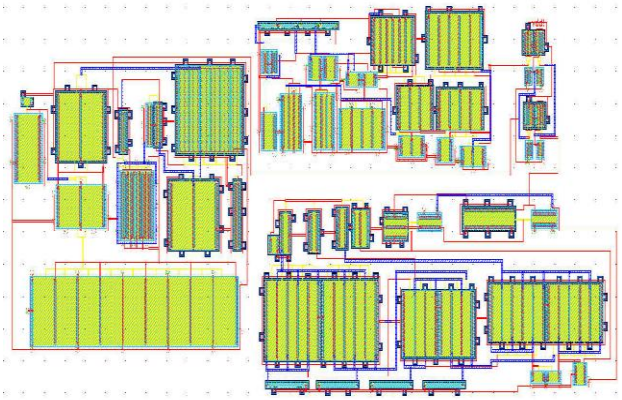

Fig.21. Layout of Ramp Generator (148 µm × 60 µm)

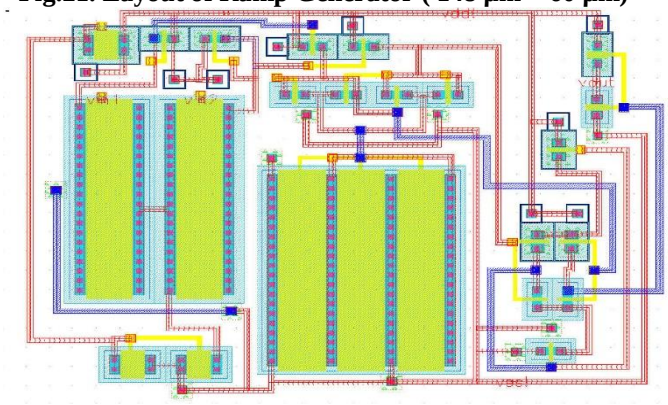

Fig.22. Layout of PWM comparator (27 µm × 19 µm)

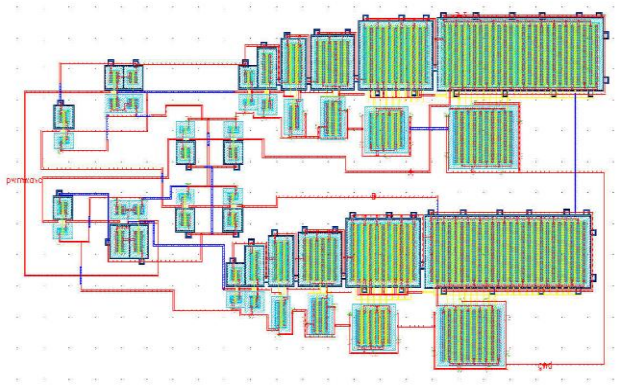

Fig.31. Layout of non overlapping combinational logic circuit (120 µm × 56 µm)

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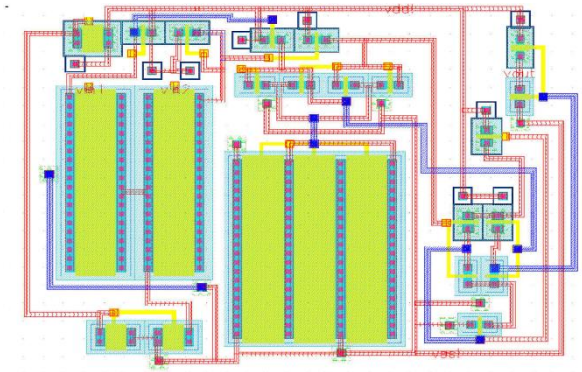

Fig.32. Layout of Level shifter (7.5µm×7.5 µm)

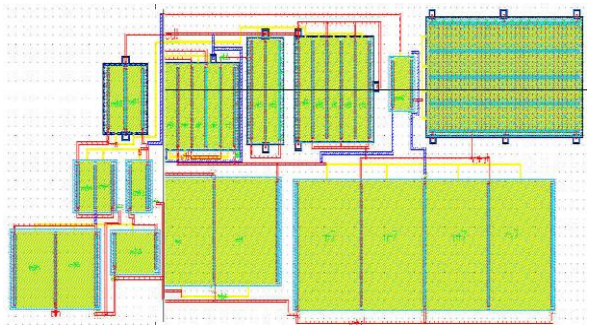

Fig.33. Layout of Op-Amp (92µm×34 µm)

	25KHz	20KHz	15KHz	10KHz	5kHz
Output Power(W)	434.4m	452.7m	473.2m	495m	515.5m
THD	2.2%	2.471%	2.639%	2.815%	3%
Efficiency	78.8%	86.2%	92.15%	92%	95.8%

Table 1: Open loop results (THD & Efficiency)

	25KHz	20KHz	15KHz	10KHz	5KHz
Output Power(W)	455.6m	471.8m	470m	538.3m	504m
THD	1.407%	1.649%	1.83%	2.04%	2.32%
Efficiency	92.05%	91.06%	89.05%	92%	92.56%

Table 2: Closed loop results (THD & Efficiency)

V.CONCLUSION AND FUTURE SCOPE

The audio power amplifier for Cell Phone driving a speaker has been designed and implemented using UMC high voltage 0.18 μ m technology. In this paper, a negative feedback is used to reduce the THD. Without feedback, the THD is above 3%.By employing feedback, the THD was reduced by 1.96dB.We have studied various classes of amplifiers like Class-A, Class-B, Class-C, Class-D, Class-AB. To achieve a high efficiency, Class D architecture has been chosen for our application. Each of the building blocks was designed with proper functionality providing low power dissipation and low distortion at the output. Several testing procedures have been implemented using sinusoidal signal and amplitude modulated sinusoidal signal as input audio signal. Output has been tested for different frequencies in the audio signal range. A Class D amplifier can be used in bridge configuration with a linear amplifier. When bridge is switched to common mode level, it results in less dissipation (app. 2 times lower than Class AB) and lesser distortion (<0.05%).Due to parasitic capacitances from lay out the delay of the comparator increases like that for op amp gain decreases by some amount this can be compensated by taking proper lay out techniques like inter digitization, common centroid and replication. High efficiency (3.5 times better than Class AB) and less distortion (0.01%@1kHz) are the features of the Class AB+D parallel amplifier and these features are not dependent on the connected load. For doing most of the filtering for a Class D amplifier, a linear amplifier can be used except that there will be a little extra power dissipation. As a result, the external filter need not be strictly linear and also the numbers of components used are reduced. Also, the transfer of the amplifier will dependent less on the connected load. But, quiescent power dissipation is much higher than in class D amplifiers, which is the main disadvantage. Thus, a new step is taken towards highly integrated power efficient audio amplifiers, which are parallel AB/D systems.

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