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Design and Implementation of FIR Filter using Efficient MAC

Bala Sindhuri Kandula, K.Padma Vasavi, I.SantiPrabha

Abstract: ***The Design And Realization Of Efficient Multiplication And Accumulation Unit (MAC) Of A Digital FIR Filter Has Substantial Influence In Designing A Well-Organized Finite Impulse Response Filter As It Is Used To Compute The Filter Response. Area Efficiency In An FIR Filter Can Be Achieved By Reducing The Gate Count Of Either Multiplier Unit Or An Adder Unit Or Both The Units Since They Are The Basic Building Blocks Of FIR Filter. This Paper Presents A VLSI Architecture For A 4-Tap FIR Filter Which Is Designed By Using Efficient Adder And A Multiplier Employing Logic Optimization Technique. Area For MAC Based FIR Filter Employing Vedic-CSLALOT Is Improved By 11.959% When Compared To Hierarchy-SQRT-CSLA. Total Power For MAC Based FIR Filter Employing Vedic-CSLALOT Is Improved By 13.15% As Against To Hierarchy-SQRT-CSLA.***

Keywords: SQRT-CSLA, CSLALOT, Hierarchy Multiplier, Vedic Multiplier

I. INTRODUCTION

Finite-Impulse-Response (FIR) filter is gaining noteworthy importance in digital communications because of its fascinating characteristics such as linearity and stability. Realization and implementation of FIR filters using hardware approach in real time applications is effectual in terms of cost and functioning when compared to software approach [1]. There is still a possibility to reduce the area which has significant impact in reducing the cost of FIR filter. This can be achieved by employing logic optimization technique. One more efficient performance metric is speed which in particular is used to determine the computation speed of the complete architecture. The combinational delay of the FIR filter can be reduced by employing efficient fast design elements in the design of MAC. The foremost structural blocks or elements used in the design of VLSI architecture for FIR filter are adder and multiplier. RCA is used as one of the basic adder module used in the design of FIR Filters if speed is not the main performance measure in the design of efficient architecture [2]. But, if speed is the main performance metric, CSLA can be one of the best choice as pre-computation of outputs with the assumption of input carry and selection technique plays the key role [3].Reduction in area of CSLA is achieved by CSLALOT[4].

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***** Correspondence Author
Bala Sindhuri Kandula*,E.C.E Department, Ph.D Scholar, JNTU ,Kakinada , Andhra Pradesh, India. Email: k.b.sindhuri@gmail.com
K.Padma Vasavi , Professor, E.C.E Department , SVECW , Bhimavaram , Andhra Pradesh, India. Email: padmavasaviece@svecw.edu.in
I. Santi Prabha, Professor , E.C.E Department, University College of Engineering, JNTU , Kakinada, Andhra Pradesh, India. Email: santiprabha@yahoo.com

Many researchers worked on the design and implementation of efficient VLSI architectures for multiplier as multiplier is one more key block which decides the computational speed, area and total power consumption of the FIR filter. While investigating several VLSI architectures for multipliers, Vedic multiplier is discovered to be one the speediest multiplier [5].Hierarchy multiplier is designed based on vedic mathematics for improvising the speed of the multiplication operations by using CSLA and BEC [6]. Till now high speed adders and multipliers have been investigated for the efficient realization of MAC based FIR filter. Thus, the complication of the filter is controlled by adders and multipliers. The paper structure is planned as follows. Section II deals with MAC based FIR Filter with different MAC's. Section III presents VLSI architectures for adders. Section IV presents VLSI architectures for multipliers. Section V discusses results and discussions. Finally, the work is concluded in Section VI.

II. MAC BASED FIR FILTER

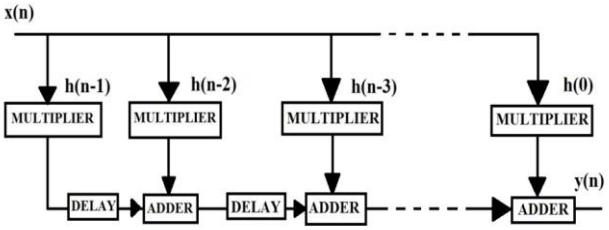

Fig. 1.VLSI architecture for MAC Based FIR Filter

The elementary blocks in designing the efficient VLSI architecture for FIR Filter depends on the efficient design of VLSI architectures for multipliers and adders. The multiplication process in the design of 4-tap MAC based FIR filter is implemented by using 8-bit vedic multiplier and 8-bit Hierarchy multiplier. 16-bit adders used in the design of VLSI architecture for MAC based FIR Filter are SQRT-CSLA and CSLALOT .The design of MAC unit by using efficient multipliers and adders is carried out and ultimately these MAC units are consigned in FIR filter architecture to estimate its functioning. The groupings of Multiplier and adder, used in the design of MAC unit for FIR filter architecture are

- Vedic-SQRT-CSLA
- Vedic-CSLALOT
- Hierarchy-SQRT-CSLA
- Hierarchy-CSLALOT

III. VLSI ARCHITECTURES FOR ADDER MODULES

A. *VLSI Architecture for CSLALOT*

The grouping mechanism of 16-bit CSLALOT is shown in Table.1.CSLALOT uses eight groups for area optimization by using MRCA1 (Modified Ripple Carry adder with input carry is equal to 'one') and mechanism used for grouping [4] is shown in Fig.2.

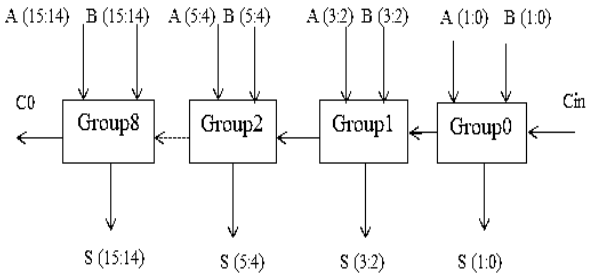

Fig. 2 CSLALOT Grouping Overview

Table.1. CSLALOT Grouping Mechanism and internal modules

Group	Set	Data -Width	CSLALOT
			Main modules
1	1	2-bit	RCA0
2	1	2-bit	RCA0
	2	2-bit	MRCA1
			2:1 Mux(3)
3	1	2-bit	RCA0
	2	2-bit	MRCA1
			2:1 Mux(3)
4	1	2-bit	RCA0
	2	2-bit	MRCA1
			2:1 Mux(3)
5	1	2-bit	RCA0
	2	2-bit	MRCA1
			2:1 Mux(3)
6	1	2-bit	RCA0
	2	2-bit	MRCA1
			2:1 Mux(3)
7	1	2-bit	RCA0
	2	2-bit	MRCA1
			2:1 Mux(3)
8	1	2-bit	RCA0
	2	2-bit	MRCA1
			2:1 Mux(3)

RCA with input carry is equal to 'zero' is coined as RCA0.Similarly RCA with input carry is equal to 'one' is coined as RCA1.Total number of multiplexers used in the design of each group is indicated in (). Area optimization for CSLALOT architecture is clearly evaluated by using theoretical approach and practically proved in [4].

More number of MRCA1's used in the design of CSLALOT definitely helps in the reduction of gate count.

B. *VLSI Architecture for SQRT-CSLA*

SQRT-CSLA adder uses five groups as shown in Fig.3.The detailed grouping mechanism is tabulated in Table-2.SQRT-CSLA mostly helps to improvise the speed or in other terms helps in reduction of combinational delay .The speed is improved by assumption of carry and computing the output from group2 onwards and finally selected by using the obtained carry from the preceding group carry which definitely helps to boost up the speed when compared to conventional RCA.

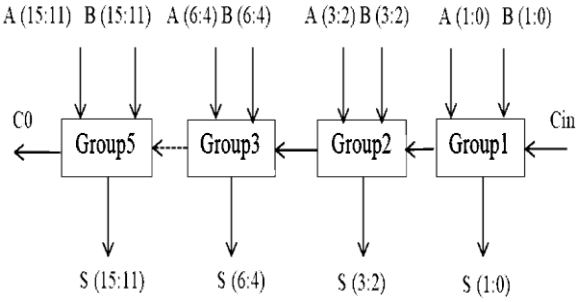

Fig. 3 SQRTCSLA Grouping Overview

Table.2. SQRT-CSLA Grouping Mechanism and internal modules

Group	Set	Data -Width	SQRT-CSLA
			Main modules
1	1	2-bit	RCA0
2	1	2-bit	RCA0
	2	2-bit	RCA1
			2:1 Mux(3)
3	1	3-bit	RCA0
	2	3-bit	RCA1
			2:1 Mux(4)
4	1	4-bit	RCA0
	2	4-bit	RCA1
			2:1 Mux(5)
5	1	5-bit	RCA0
	2	5-bit	RCA1
			2:1 Mux(6)

IV. VLSI ARCHITECTURES FOR MULTIPLIER MODULES

A. *Vedic Multiplier*

The Vedic multiplier is a simple digital multiplier architecture/algorithm that is designed based on the vertical and cross-wise multiplication of the multiplier and the multiplicand in terms of the number of bits that are specified for multiplication. It is derived from the Indian Vedic sutras from ancient scriptures that gave a set of algorithms to perform calculations in a faster manner.

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Vedic multiplier algorithm is based on one of the ancient sutras which are called as "URDHVA-TIRYAGBHYAM", which literally means vertically and crosswise and is a general multiplication formula. A, B each of 8-bit are taken as inputs for the VLSI architecture for Vedic multiplier whereas S is the obtained output as shown in Fig.4.Partial product addition is carried out by Ripple carry adders .[5]

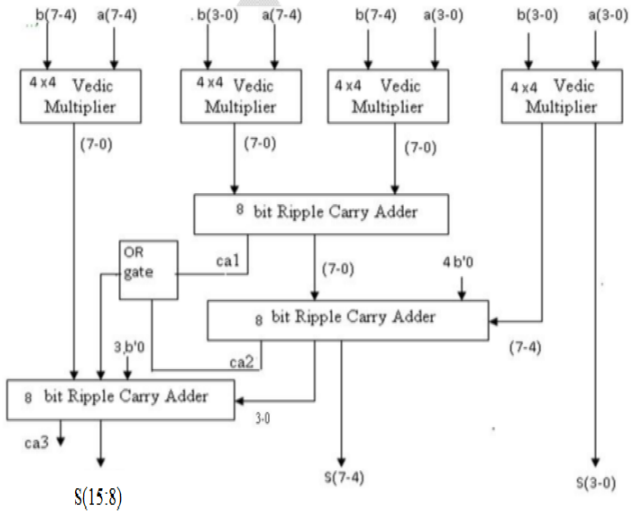

Fig. 4. VLSI architecture for Vedic Multiplier

B. *Hierarchy Multiplier using Vedic Mathematics*

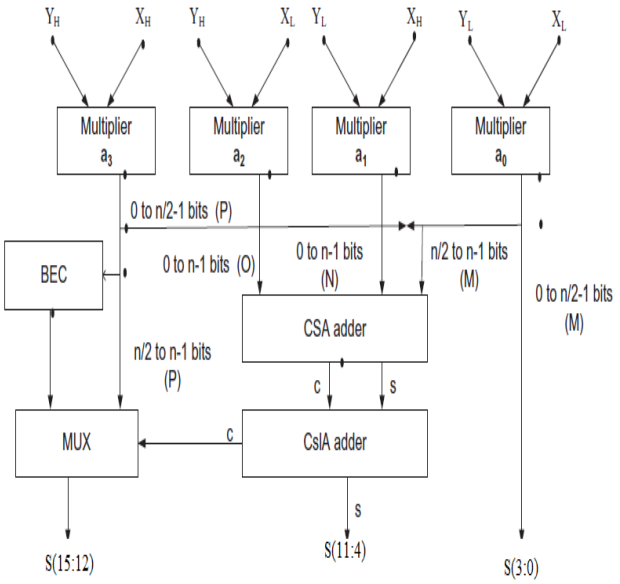

Fig. 5. VLSI architecture for Hierarchy Multiplier

Hierarchy multiplier design is carried out by using Vedic mathematics. Partial Product addition is carried out by employing CSLA for improvement the speed parameter and BEC for area Optimization. As BEC is used in the last stage, speed is not much affected. Thus multiplier is well suited for high speed. X_L, Y_L are taken as inputs and "S" is obtained as output[6].

V. RESULTS AND DISCUSSIONS

Different MAC Based FIR Filters such as Vedic-SQRT-CSLA, Vedic-CSLALOT, Hierarchy-SQRT-CSLA and Hierarchy-CSLALOT are coded in Verilog HDL. The performance factors in the design of VLSI architectures are area, delay and power. ASIC synthesis results are obtained by using Encounter RTL compiler using slow library and tabulated in Table.3, Table. 4, Table.5 and Table.6 for different MAC Based FIR filters

Table.3. Encounter Area Results for Different MAC Based FIR Filter for 4-tap

MAC	Area (μm2)
Vedic-SQRT-CSLA[1]	9468.269
Hierarchy-SQRT-CSLA	9847.269
Hierarchy-CSLALOT	**9025.275**
Vedic-CSLALOT	**8714.946**

From Table.3, it is noticed that Area for MAC based FIR Filter employing Vedic-CSLALOT is improved by 7.9% when compared to Vedic-SQRT-CSLA. Area for MAC based FIR Filter employing Vedic-CSLALOT is improved by 11.959% when compared to Hierarchy-SQRT-CSLA. Area for MAC based FIR Filter employing Vedic-CSLALOT is improved by 3.43% when compared to Hierarchy-CSLALOT

Table.4. Encounter Leakage and Dynamic Power Results for Different MAC Based FIR Filter for 4-tap

MAC	Leakage Power (nW)	Dynamic Power (nW)
Vedic-SQRT-CSLA[1]	61047.612	557064.811
Hierarchy-SQRT-CSLA	62085.180	639122.858
Hierarchy-CSLALOT	**58329.271**	**606510.194**
Vedic-CSLALOT	**52691.874**	**556247.416**

From Table.4, it is noticed that Leakage Power for MAC based FIR Filter employing Vedic-CSLALOT is improved by 13.6% when compared to Vedic-SQRT-CSLA. Leakage Power for MAC based FIR Filter employing Vedic-CSLALOT is improved by 15.129% when compared to Hierarchy-SQRT-CSLA. Leakage Power for MAC based FIR Filter employing Vedic-CSLALOT is improved by 9.66% when compared to Hierarchy-CSLALOT.

Dynamic Power for MAC based FIR Filter employing Vedic-CSLALOT is improved by 0.14% when compared to Vedic-SQRT-CSLA. Dynamic Power for MAC based FIR Filter employing Vedic-CSLALOT is improved by 12.96% when compared to Hierarchy-SQRT-CSLA. Dynamic Power for MAC based FIR Filter employing Vedic-CSLALOT is improved by 8.28% when compared to Hierarchy-CSLALOT

Table.5. Encounter Total Power Results for Different MAC Based FIR Filter for 4-tap

MAC	Total Power (nW)
Vedic-SQRT-CSLA[1]	618112.423
Hierarchy-SQRT-CSLA	701208.037
Hierarchy-CSLALOT	**664839.466**
Vedic-CSLALOT	**608939.290**

From Table.5, it is noticed that total Power for MAC based FIR Filter employing Vedic-CSLALOT is improved by 1.4% when compared to Vedic-SQRT-CSLA. Total Power for MAC based FIR Filter employing Vedic-CSLALOT is improved by 13.15% when compared to Hierarchy-SQRT-CSLA. Total Power for MAC based FIR Filter employing Vedic-CSLALOT is improved by 13.15% when compared to Hierarchy-CSLALOT

Table.6. Encounter Delay Results for Different MAC Based FIR Filter for 4-tap

MAC	Delay (psec)
Vedic-SQRT-CSLA[16]	7067
Hierarchy-SQRT-CSLA	6239
Hierarchy-CSLALOT	**6924**
Vedic-CSLALOT	**6958**

From Table.6, it is noticed that Speed for MAC based FIR Filter employing Vedic-CSLALOT is improved by 1.5% when compared to Vedic-SQRT-CSLA. Speed for MAC based FIR Filter employing Vedic-CSLALOT is less by 10.33% when compared to Hierarchy-SQRT-CSLA. Speed for MAC based FIR Filter employing Vedic-CSLALOT is less by 0.4% when compared to Hierarchy-CSLALOT

VI. CONCLUSION

MAC based FIR Filters employing Vedic–SQRT-CSLA, Hierarchy–SQRT-CSLA, Hierarchy-CSLALOT and Vedic –CSLALOT are designed and synthesized using Encounter RTL Compiler Tools. Area for MAC based FIR Filter employing Vedic-CSLALOT is improved by 7.9% when compared to Vedic-SQRT-CSLA. Area for MAC based FIR Filter employing Vedic-CSLALOT is improved by 11.959% when compared to Hierarchy-SQRT-CSLA. Area for MAC based FIR Filter employing Vedic-CSLALOT is improved by 3.43% when compared to Hierarchy-CSLALOT. From Result analysis, it has been observed that Vedic –CSLALOT MAC based FIR Filter is an area efficient MAC based FIR Filter.

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AUTHORS PROFILE

Bala Sindhuri Kandula received her B.E degree in Electronics &communication Engineering from S.R.K.R Engineering college,M.Tech degree in VLSI System Design from Shri Vishnu Engineering College for Women ,Vishnupur ,Bhimavaram and pursuing Ph.D at JNTU,Kakinada.At present, She is working as an Assistant Professor at SRKR Engineering College, Bhimavaram.She has 8 years of teaching experience. Her areas of interests are Signal Processing and Very Large Scale Integrated Circuits. She has published 15 Scopus publications in IEEE -Xplore, Elsevier and Springer Series and more than 30 Research papers in various International and National Conferences

Dr. K. Padma Vasavi is Professor and Dean of Assistive Technology at Shri Vishnu Engineering College for Women. She has 20 years of teaching experience for UG and PG students. She has been contributing immensely towards the development and production of Assistive technology Products for the physically and mentally Challenged people along with elderly persons. She was awarded with Ph.D. in Ph. D in Digital Image Processing by Jawaharlal Nehru Technological University. She pursued M.Tech in Digital Systems and Computer Electronics from Jawaharlal Nehru Technological University Hyderabad .She Published more than 10 research papers in peer reviewed and refereed international journals and presented more than 20 papers in reputed International Conferences in India .

Dr I. Santi Prabha is Rector of JNTUK. She did her B.Tech & M.Tech with specialization In Instrumentation and Control Systems from JNTU College of engineering, Kakinada. She was awarded with Ph.D. in Speech signal processing by Jawaharlal Nehru Technological University in 2005. She has more than 30 years of experience in teaching. She has guided three Ph.D. scholars and is presently guiding 9 Ph.D scholars. She has guided more than 100 M.Tech. Projects. She is a member of various professional organizations like Fellow of Institution of Engineers (India), Fellow member of The Institution of Electronics and Telecommunication Engineers and Life member of Indian Society for Technical Education. She has published more than 80 technical papers in National and International journals/ conferences. She worked as Head of ECE Department and subsequently served as Director of EOW&G, JNTUK, and Kakinada during 2009 – 2015.