

VLSI Architecture of High Performance Multiplier for High Speed Applications

J.M.Mathana, R.Menaka, R.Dhanagopal, B.Sundrambal

Abstract: In the application of digital signal process multipliers play a vital role. With advances in technology, several researchers have tried and try to design multipliers which supply high speed, low power consumption, regularity of layout and thus less space or maybe combination of them in one multiplier factor. Thus, Compact VLSI design for four bit multiplier factor is planned during this paper that is appropriate for low power and high speed applications. Multiplier factor with high performance is achieved through the novel style of hybrid single bit full adder and Dadda algorithmic rule. The important path delay and power consumption of the planned multiplier factor square measure reduced by 65.9% and 24.5% severally when put next with existing multipliers. The planned multiplier factor is synthesized exploitation CADENCE five.1.0 EDA tool and simulated exploitation spectre virtuoso.

Keywords: Multiplier; Dadda Algorithm; Gate diffusion Input (GDI); Pass transistor logic (PTL); CMOS process technology; Cadence(tool)

I. INTRODUCTION

In the real time signal processing applications, the multipliers are the basic module of the digital systems. Many research works are being done to reduce power dissipation, area and time in multipliers and dividers. The multiplier^[1] designed using approximate half adder and full adder reduces all parameters by 25% to 35%. The high speed vedic multipliers^[2] designed to implement DSP operations of finite length sequences which reduces the processing time 40% to 60% than the conventional multiplier. Fixed and floating point multipliers^[3] designed by Vedic algorithm increased the operating speed and precision of the Digital Signal Processors. Many algorithms/architectures developed and implemented using Dadda^[4], Wallace tree^[5], Vedic^[6] and Booth etc. are used to optimize power and speed.

In section II discussed about the dadda algorithm. The architecture of proposed system is explained in the part III. Part IV provides the result analysis of the proposed and existing approximate multipliers. Part V describes the conclusion.

Revised Manuscript Received on January 05, 2020

Dr.J.M.Mathana, Professor, Dept. of Electronics and Communication Engineering, Chennai Institute of Technology, Kandrathur, Chennai, Tamilnadu, India

Dr.R.Menaka, Professor, Dept. of Electronics and Communication Engineering, Chennai Institute of Technology, Kandrathur, Chennai, Tamilnadu, India

Dr.R.Dhanagopal, Associate Professor, Dept. of Electronics and Communication Engineering, Chennai Institute of Technology, Kandrathur, Chennai, Tamilnadu, India

Dr.B.Sundrambal, Professor, Dept. of Computer Science and Engineering, Chennai Institute of Technology, Kandrathur, Chennai, Tamilnadu, India

II. DADDA ALGORITHM

In the proposed work, the speed of the critical path of the multiplier is reduced by reducing the length of the tree with the help of dadda algorithm [8]. The proposed 4 bit multiplier consists of sixteen partial products. Fig. 1 shows a sample 4x4 multiplications, where the length of the tree is four. With the help of dada algorithm the length of the tree is reduced to two.

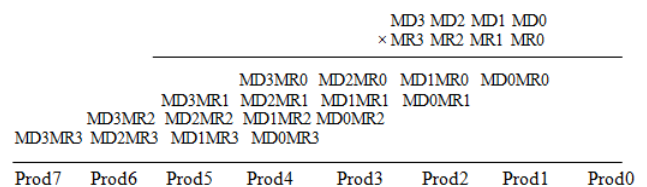


Fig.1. Sample 4x4 Multiplication

Dadda algorithm does not require any previous Level output to compute next Level output, which reduces the propagation delay. In the first Level, dada algorithm diminishes the tree length from four to three. During the second Level, the length is still reduced from three to two, and in the final Level, the total length of the multiplication tree is reduced to two. The Level wise reduction procedure is shown in below figures 2, 3 and 4.

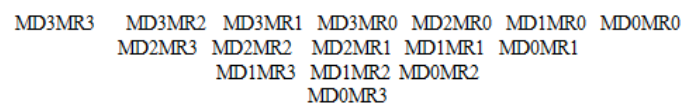


Fig.2. Level -1

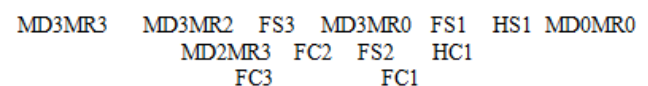


Fig.3. Level -2

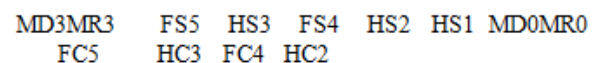


Fig.4. final Level

III. PROPOSED 4x4 MULTIPLIER

The general block diagram of projected four x four multiplier is given in Fig.5. This multiplier is developed in terms of pass transistor logic based hybrid three input binary digits adder circuit and two input binary digits adder circuit. This circuit consists of 10 transistors.

In the first Level of the multiplier there are 16 partial products and generated and implemented using 16 logical AND gates. In second Level, by using three 3-input binary digits adder circuit and one two input binary digits adder circuit the length of the tree is reduced to half. In the third Level, the length is further reduced by usage of only two- input binary digits adder

VLSI Architecture of High Performance Multiplier for High Speed Applications

circuit and two 3-input binary digits adder circuit. In order to get better output voltage finally the output signals are passed through the buffers as shown in figure 5.

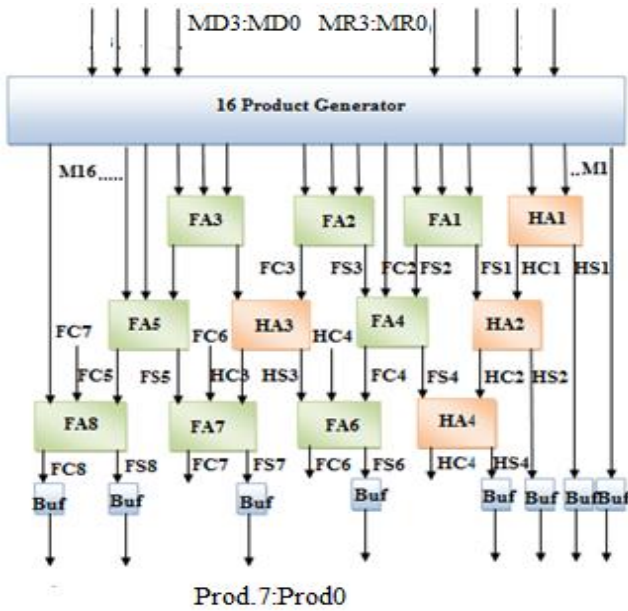


Fig.5. Architecture of proposed 4x4 multiplier

In the proposed architecture consists of eight three input binary digits adder circuit, four two input binary digits adder circuit and eight buffers. The schematic of the basic AND cell is shown in Fig.6.

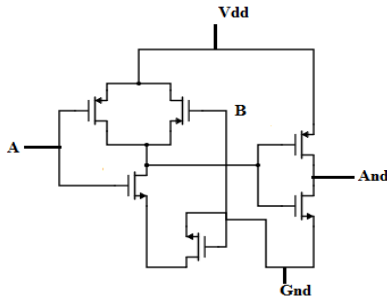


Fig.6. AND Gate [7]

Fig. 7 shows the circuit diagram of single adder user in the proposed multiplier. It has three modules T1, T2 and T3. Module T1 is the Gate Diffusion Logic (GDI) XOR gate. Module T2 and T3 are Pass Transistor Logic (PTL) XOR, PTL MUX respectively. Module T1 and T2 are responsible for the generation of sum of full adder. Carry output is generated by the help of module T3.

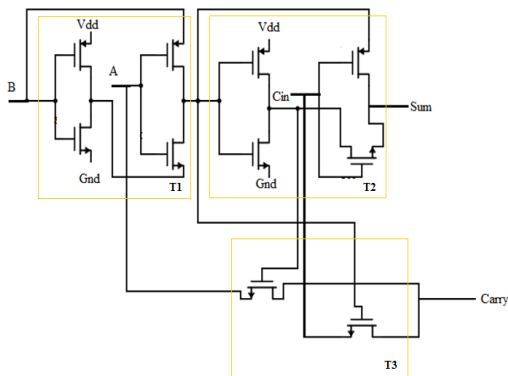


Fig.7. Proposed single bit full adder

A two input binary digits adder circuit will play vital role to design multiplier. In 4x4 multiplier design four two input binary digits adder circuit are used. The CMOS schematic diagram of the two input binary digits adder circuit is shown in Fig.8.

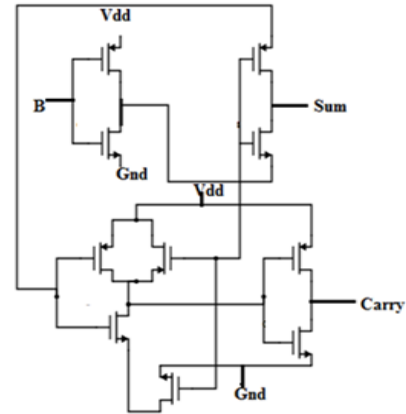


Fig.8. Two input binary digits adder circuit [7]

The buffer in the multiplier is used to propagate the signals from initial Level to final Level and also to retain the voltage level. It is shown in Fig.9

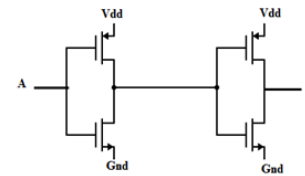


Fig.9. Buffer [7]

IV. SIMULATION RESULTS

The proposed multiplier is synthesized using CADENCE 5.1.0 EDA tool and simulated using spectre virtuoso. Fig.10 shows the RTL schematic diagram of the proposed multiplier in cadence.

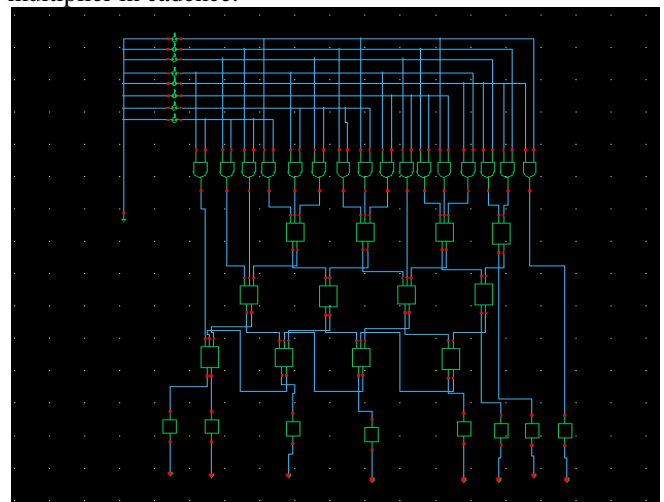


Fig.10. Technology diagram of developed system in cadence

Below figure shows the transient response of the proposed 4 bit multiplier. It shows partial product of the multiplier (Prod0, Prod1, Prod2, Prod3, Prod4, Prod5, Prod6, Prod7).

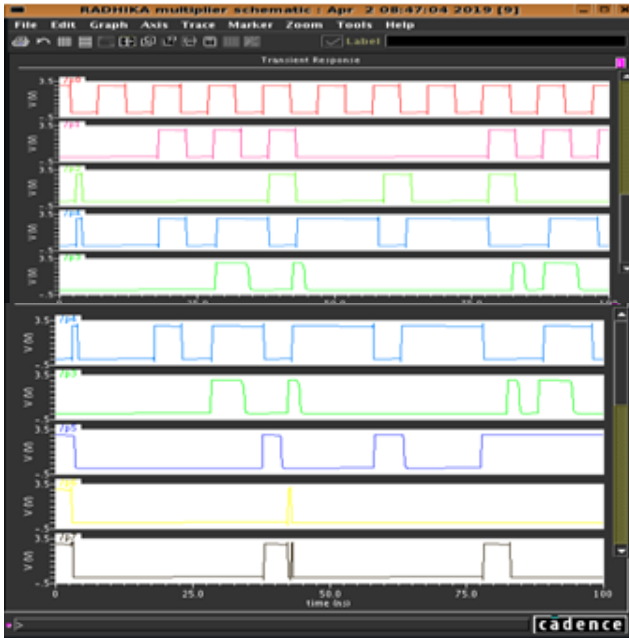


Fig.11. Transient response of the multiplier

Below figures shows the power and delay calculation in cadence.

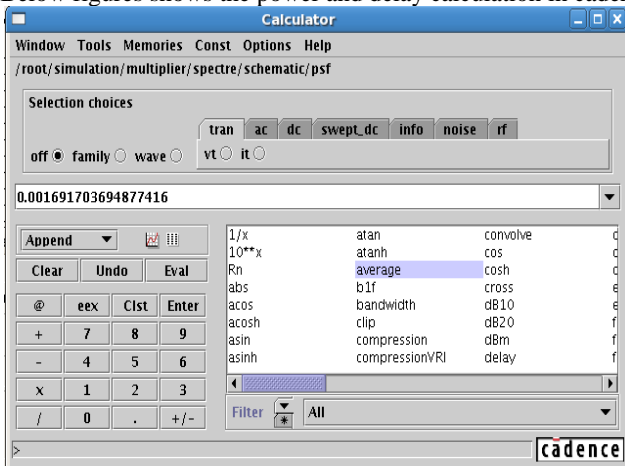


Fig.12. Power calculation in cadence

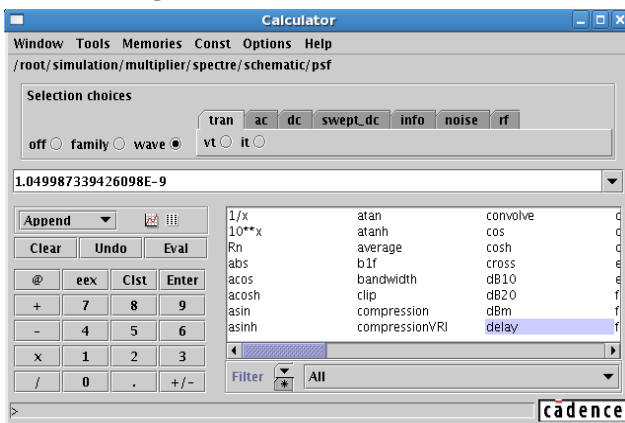


Fig.13. Delay calculation in cadence

Table I. Comparison Of Different Multipliers

Table I shows the comparison of performance parameters such as power consumption, critical path delay and number of transistors of different multipliers using different types of full adders. From this table it is observed that the circuit complexity of proposed multiplier is less and also the power

No	Multiplier	No of transistors	Power in mW	Delay in ns
1	Using Conventional CMOS Full Adder	392	0.0058	3.834
2	Using Hybrid Full Adder (Existing)	264	0.00224	3.0603
3	4-bit Dadda Multiplier using Compressor	376	1.172	0.353
4	DADDA Tree Multiplier Using Adiabatic Logic	-	77	-
5	4-bit Static CMOS based DADDA Multiplier	316	-	-
6	Proposed Multiplier	248	0.00169	1.0409

consumption of the multiplier is 1.69μW and critical path delay of the proposed multiplier is 1.04ns which is very less when compared with the other existing multipliers.

Fig.14 and Fig.15 shows the graphical representation of power and delay.

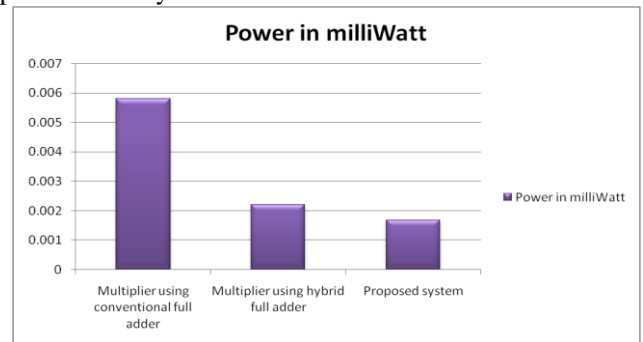


Fig.14. Comparison of power in mW

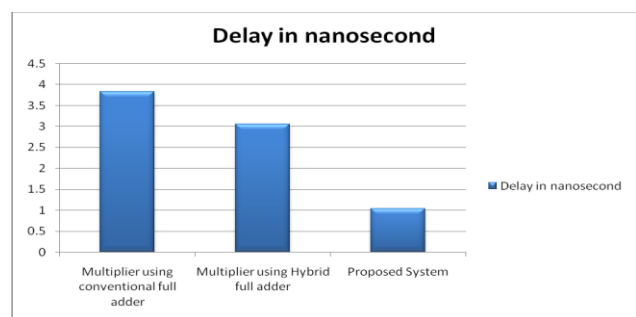


Fig.15. Comparison of delay in nano second

Table II shows the logic utilization of various modules in 4 bit multiplier.

Table II. Logic Utilization Of Various Modules

Module	No of transistors	Technique used
Full adder (area and power efficient single bit full adder)	80	Sum: GDI XOR Carry: PTL XOR

Half adder	40	CMOS Process technology
Buffer	32	CMOS Process technology
AND gate	96	CMOS Process technology

V. CONCLUSION

The proposed 4 bit multiplier with low power, minimum delay and optimum circuit complexity is being designed with hybrid efficient single bit 3-input binary digits adder circuit. In three input binary digits adder circuit, low power consumption and minimum propagation delay are achieved through PTL and GDI technique. Minimum response time the maximum throughput is achieved using hybrid three input binary digits adder circuit. Due to usage of dadaalgorithm propagation delay is reduced. The proposed 4×4 multiplier has average power consumption of 1.69μW with a propagation delay of 1.04 ns. These calculated parameters are lesswhen compared to the available multiplier design.

REFERECNES

1. Sumant Mukherjee, Dushyant Kumar Soni“Energy Efficient Multiplier for High Speed DSP Application”IJCSMC, Vol. 4, Issue. 6, pg.66 – 75,June 2015.
2. Itawadiya, A.K, Mahle, R,Patel, V,Kumar, D, "Design a DSP operations using vedic mathematicInternational Conference on," Communications and Signal Processing (ICOSP), 2013, vol.3, no.5, pp.897-902, April 2013.
3. Saokar, S.S.; Banakar, R. M.; Siddamal, S., "High speed signed multiplier for Digital Signal Processing applications," IEEE International Conference on Signal Processing, Computing and Control (ISPCC), vol.15, no.17, pp.1-6, March 2012.
4. C.S. Wallace, "A Suggestion for a Fast Multiplier", IEEE Transaction On Electronic and Computer, Vol.EC-13, PP. 14-17, February 1964.
5. Prashant D. Pawale, Venkat N Ghodke, High speed Vedic multiplier design and implementation on FPGA, International Journal of Applied Research vol.1, no.7, pp:239-2442015.
6. Muhammad HussnainRiaz, Syed Adrees Ahmed, QasimJavaid, Tariq Kamal, "Low Power 4×4 Bit-Multiplier Design using Dadda Algorithm and Optimized Full-Adder", IEEE International bhurban conference on applied sciences and technology(IBCASP),2018.
7. RishabGoyal, Sanjeev Sharma, "Single Bit Hybrid Full-Adder Cell by Gate Diffusion Input and Pass Transistor Logic(PTL) Technique,"IEEE International Conference On Advances In Electrical Technology For Green Energy,2017.
8. S. Z. Naqvi, S. Z. Hassan and T. Kamal, "A power consumption and area improved design of IIR decimation filters via MDT," International Conference on Intelligent Systems Engineering (ICISE), Islamabad, pp. 146-151, 2016.
9. Sulieman, MawahibHussein,Mahmoud, Mariam,Raafat, RemondaReda, Gehad,"Designand Simulation of a Nano-scale Threshold-Logic Multiplier" TEM Journal. Volume 8, Issue 2, Pages 333-338, ISSN 2217-8309, DOI: 10.18421/TEM82-03, May 2019

AUTHORS PROFILE



Dr.J.M.MATHANA obtained her B.E Degree in Electronics and Communication Engineering, M.E Degree in VLSI Design and Ph.D Degree in Information and Communication from Anna University, Chennai. She has over 25 years of rich experience in academic

arena and industryCurrently, she is working as Principal and Professor, ECE Department in Chennai Institute of Technology, Chennai - 69. Her research interests include the Error Corrective Coding, Interleavers, Wireless Communication and VLSI Design. Her strong commitment towards research is reflected in her contribution of more than 100 international and national publications. She is the recognized research supervisor in Anna University, Chennai and supervising 6 research scholars in Anna University, Chennai in the field of Information and Communication. She is the distinguished member of the Indian Society of

Technical Education (ISTE) and senior IEEE member. She is the reviewer in international journals like, International Journalof Institution of Engineering and Technology (IET), International Journal of Computers Communications and Control, International Journal of Advanced Research Trends in Engineering and Technologyand ICTACT Journal. She has numerous workshops/seminars/national and international conferences to her credit.



Dr R.Menaka obtained her Ph.D. Degree in the faculty of Information and Communication Engineering from Anna University, Master Degree in Applied Electronics from Anna University, Bachelor Degree in Electronics and Communication Engineering from Madras University. She has around 19 years of teaching experience. Her area of Interest includes Mobile Ad hoc Networks, Wireless Networks and Image & Signal Processing.



Dr.R.DHANAGOPAL, was born in Namakkal, TamilNadu, India. Graduated B.E(ECE) from the Jayaram College of Engineering and Technology, Trichy, Bharathidasan University, India, in 2004, ME degree in Communication Systems from Jayaram College of Engineering, Trichy, Anna University, Chennai, India , in 2008. He received doctorate in Low Power VLSI Design, in Anna University, Chennai, India in 2018. He Published 13 International Journals. Presented 12 papers in various National and International Conferences conducted in various countries like Singapore, China and Japan. Currently he is working as Associate Professor, Department of Electronics and Communication Engineering, Chennai Institute of Technology, Chennai-69. His research interest includes Low power design and testing VLSI Circuits, Image Processing, IoT, Data Mining, Antenna Design.



Dr.B.Sundarambal obtained her Ph.D Degree in the faculty of Information and Communication Engineering from Anna University, Master degree in Computer Science and Engineering from Anna University, Bachelor Degree in Electronics and Communication Engineering from Bharathiar University. She published papers in 4 international Journals. Her area of interest includes Computational Intelligence and Computer Vision. She is life member of ISTE.