Gain Error end DNL for Testing ADCs: Optimization in Time Domain

Manish Jain, R P Kumawat

Abstract – Optimization in ADC is an important component which predicts overall accuracy of a system using it. Signals are in real time nature and it is necessary to convert these signals in digital form to interpret with digital form of signals and microcomputer based systems. ADC is used to carry out these conversions process from analog to digital.

Determination of parameters of an ADC such as DNL, INL, SNR and ENOB are necessary for complete dynamic analysis and characterization of ADC. In frequently, application prerequisite input to an Analog to digital converter is time varying which requires determination of its parameters at corresponding frequency and different test conditions

In order to test an ADC, it is necessary to first determine its code transition levels. Further Gain error, DNL are estimated using code transition level based on histogram technique. If there is an code transition level error introduced then effect of this error leads to error in estimate of gain, offset, DNL and ENOB. Further estimation of variance in different parameter values is analyzed in the proposed work.

Keywords- Analog-to-digital converter, Effective No. of Bit, Histogram Technique, Offset Error, Gain Error.

I. INTRODUCTION

For ADC testing histogram method is most frequently used. this method introduced to test various ADC parameters like INL, DNL, offset and gain error. The transition level for its parameter occurs at 0.5 LSB. The gain error shows the how a actual and ideal transfer function deviates. Histogram is created through software methods followed by computation of code levels using large no. of samples The test methodology followed during development of new algorithm of testing is to simulate ADC transfer function with software. The effect of different error is calculated by simulation (with software) to meet practical conditions. ADC testing using different nonlinearities maps the actual transfer function and characteristics of an ADC.

II. COMPUTATION OF CODE TRANSITION LEVEL

Different steps for computation of basic histogram are shown in figure 1.1

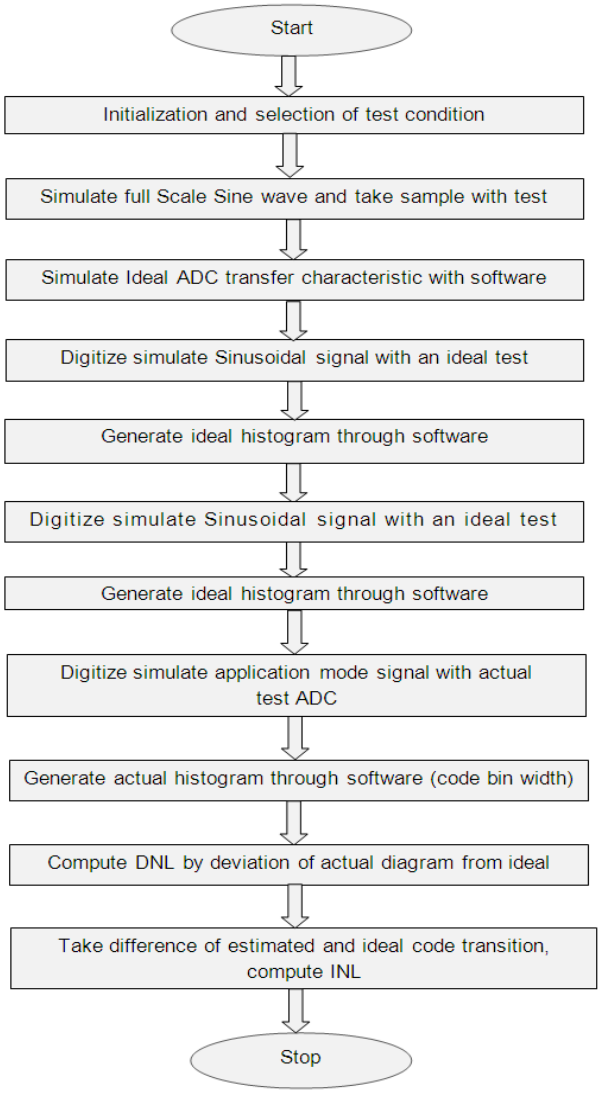

Figure 1.1 Code transition level histogram

Code transition level of ADC can be estimated using

T[k], of an N bit ADC is given as [7]

$$\hat{T}[k] = O - ACos\left[\frac{\Pi Ch[K-1]}{St}\right], K=1,2\ldots 2^{N-1} \quad (1)$$

The cumulative histogram defined by:

$$C_k = \sum_{i=0}^{k-1} h[i] \quad (2)$$

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Where, $h[i]$ = samples recorded in code bin
M = No. of samples
A = Amplitude of input sine wave, and
C = DC offset of input sine wave,

To easiest the process, offered normalized Code bin width is given by

$$\hat{W}[k] = \hat{T}[K+1] - \hat{T}[K] \quad (3)$$

Where,
T[k] = Transition voltage
U[k] = Normalized transition voltage,
Let U[k] = U for further process

For a large number of samples estimated normalized transition voltage is computed by

$$\mu_{U_{K+1}} = -Cos\left(\pi\frac{\mu_{C_K}}{M}\right) + \frac{\pi^2}{M^2}Cos\left(\pi\frac{\mu_{C_K}}{M}\right)\frac{\sigma^2_{C_K}}{2} + ... \\ ..... + (-1)^{n/2}\frac{\pi^n}{M^n}Cos\left(\pi\frac{\mu_{C_K}}{M}\right)\frac{\mu_{n_{C_K}}}{\perp n} \quad (4)$$

III. ESTIMATION OF OFFSET AND GAIN ERROR

Application mode input is made up of various sinusoidal component determined by FFT algorithm. As gain error in ADC is dependent on input frequency, so it is necessary to compute gain error for different sinusoidal component of application mode input and appropriate gain error corrections are to be applied. First for each sinusoidal component code transition level is computed by standard histogram method as reported earlier. Based upon code transition level gain error is computed. For designed transfer function the gain of estimation is offered by [6]:

$$G = \frac{2^N - 2}{T[2^N - 1] - T[1]} \quad (5)$$

For an N bit ADC gain are for ADC are offered as

$$G_i = \frac{H_{ideal} - L_{ideal}}{H - L} \quad (6)$$

Meanwhile the same offset error of ADC is designated as:

$$\hat{O}_e = L_{ideal} - \hat{G}.\hat{L} \quad (7)$$

Where,

$\hat{L}$ is the last estimated transition voltage, $\hat{L} = \hat{T}_{2^N-1}$

$\hat{F}$ is the first estimated transition voltage, $\hat{F} = \hat{T}_1$

H(0) is number of hits at lower codes and $H_{(2^N-1)}$ is number of hits at upper codes for each sinusoidal component applied to n-bit ADC. Hence offset for each sinusoidal component is computed and algebraically summed to get resultant offset for application mode input. Further corrections are applied for various errors like gain and offset for ADC transfer characteristics and corresponding ADC outputs are generated. These errors are presents in the ADC transfer characteristic may be minimized. Meanwhile, the Nonlinear error cannot be comprised to appropriate level. Hence nonlinearity error is estimated in this paper for application mode input.

IV. NONLINEARITY ESTIMATION

DNL error is defined as actual step width an ideal value of 1 LSB.

$$DNL(i) = \frac{H(i)}{H\,ideal(i)} \quad (8)$$

Where i= 1, 2……. 2^N-2

Frequency of occurrence of each code can be computed by N bit ADC under test and DAC with resolution less than (N +2) bits are computes for corresponding stimuli input signal

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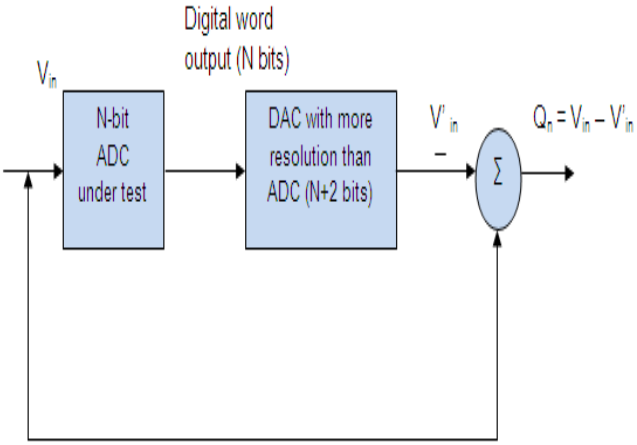


Figure 1.2 ADC input-Output Test

The modeling of an n bit ADC with different gain and DNL errors cab be followed by quantized the transfer function of practical a ADC.
The DNL and INL for first stimuli function such as sine wave may be computed by following equations computed by algorithmic interpretation in the data input for sinusoidal waves.

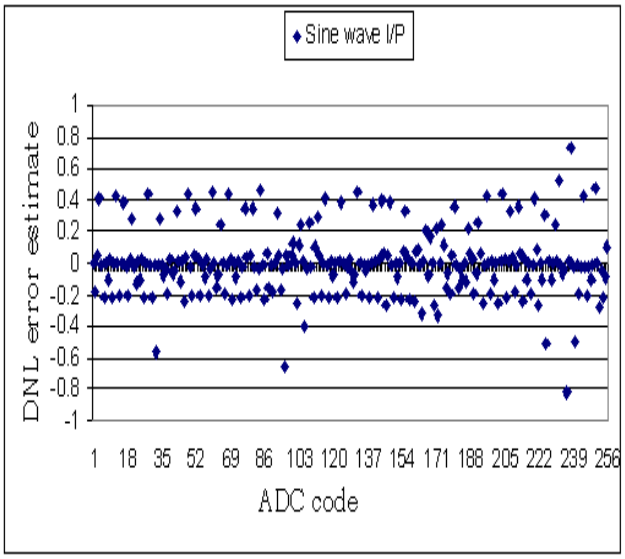
$$\left.\begin{aligned}
\tilde{h}_1(x_0) &= Y_1(0) + Y_2(0) \\
\tilde{h}_1(x_1) &= 2i^2 Y_1(1).T_1(\cos\theta_1) \\
\tilde{h}_1(x_2) &= 2i^2 Y_1(2).T_2(\cos\theta_2) \\
\tilde{h}_1(x_3) &= 2i^2 Y_1(3).T_3(\cos\theta_3) \\
\tilde{h}_1(x_4) &= 2i^2 Y_1(4).T_4(\cos\theta_4) \\
\tilde{h}_1(x_5) &= 2i^2 Y_1(5).T_5(\cos\theta_5) \\
\tilde{h}_1(x_6) &= 2i^2 Y_1(6).T_6(\cos\theta_6)
\end{aligned}\right\} \quad (9)$$

And INL h(x) for II[nd] sine wave can be defined similarly as:

$$\left.\begin{aligned}
\tilde{h}_2(x_1) &= 2i^2 Y_2(1).T_1(\cos\theta_1) \\
\tilde{h}_2(x_2) &= 2i^2 Y_2(2).T_2(\cos\theta_2) \\
\tilde{h}_2(x_3) &= 2i^2 Y_2(3).T_3(\cos\theta_3) \\
\tilde{h}_2(x_4) &= 2i^2 Y_2(4).T_4(\cos\theta_4) \\
\tilde{h}_2(x_5) &= 2i^2 Y_2(5).T_5(\cos\theta_5) \\
\tilde{h}_2(x_6) &= 2i^2 Y_2(6).T_6(\cos\theta_6)
\end{aligned}\right\} \quad (10)$$

V. SIMULATION RESULTS AND DISCUSSION

The validity of our algorithm designed can be computed and analyzed for DNL and gain error testing The Error computed can be carried out for further experimental analysis and the impression for error for different samples are shown below in the figure 1.3, 1.4, 1.5.



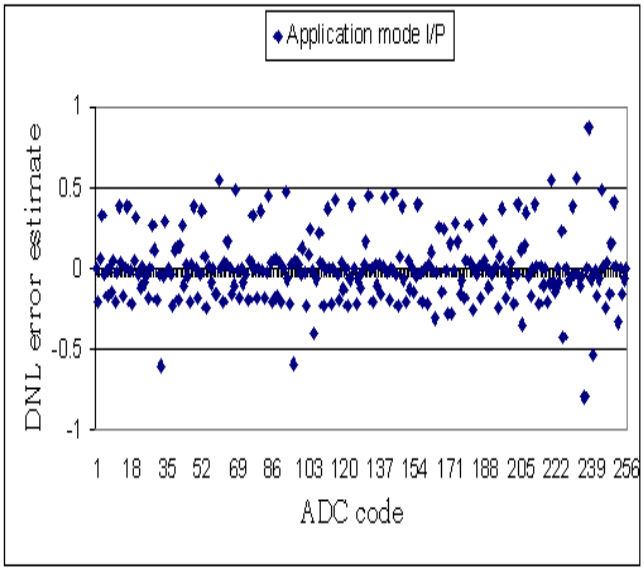


Figure1.3: DNL Error Estimated

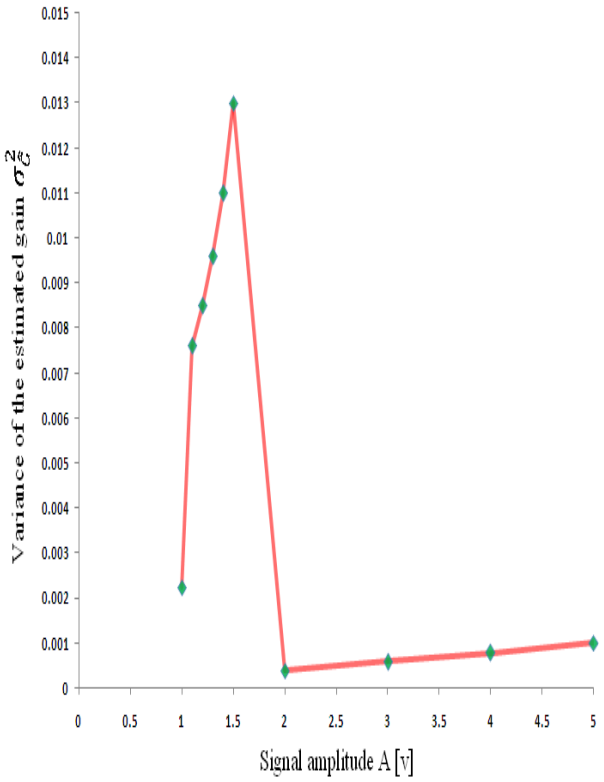


Figure 1.4 Gain estimation for 8 bit ADC

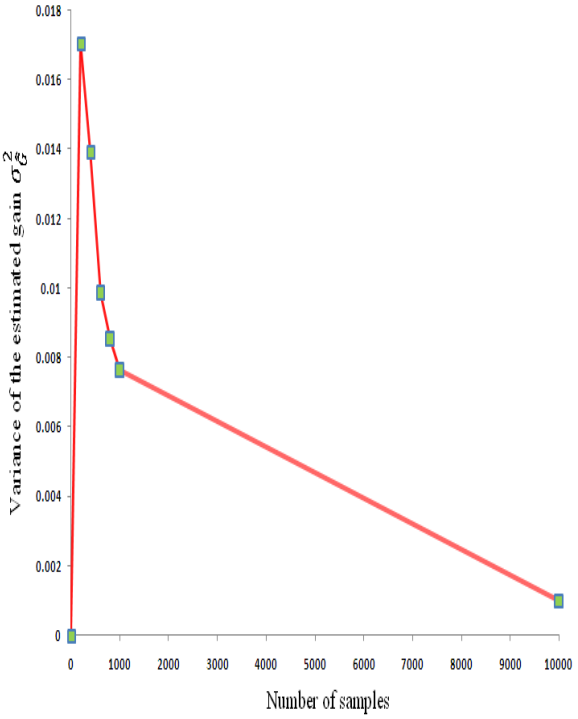


Figure 1.5 Gain estimation for 8 bit ADC under stimuli input

VI. CONCLUSION

In the proposed research work the estimation of gain and DNL error are computed with the tolerance effect of variance in the signal in the time domain analysis .the experimental analysis is carried out by additive noise aviation in the effect of standard deviation for typical 8 and 10 bit ADC gain and DNL analysis.

The full scale stimuli like sinusoidal wave are applied to 1 MHZ frequency for simulation. The sampling frequencies are modulated at 5 MHz.

Predefined large numbers of samples are taken and histogram is constructed through software followed by computation of code levels.

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Dr. Manish Jain obtained Ph.D. in 2015 in Electronics & Communication. He has vast experiences of about 18 + years. He is life member of IE, CEGR, IAENG and Editorial board members &Reviewer of some International Journal. He has authored 1 research book on DSP. Under his guidance Student project have been sanctioned for Financial Assistance by Department of Science & Technology (DST). Under his guidance 10 M.Tech and 1 PhD has been awarded. His research interest includes Semiconductor Electronics, Communication, ADC design & Testing, VLSI.

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