Buried Powered 4t Sram with Improved Write Margin

K. Manohar, M. Sri Hari, MD. Basheer Ahamad, Sai Krishna, P. Lakshman

Abstract: ***The main intention of this paper is to understand clearly about the high performance of 4T-SRAM with an improved write margin. the power consumption is often reduced considerably by using a buried power rail (BPR) to the SRAM cell, which reduces the resistance of bit line and word line. The write margin is often increased by the fine standardization of metal dimensions within the SRAM cell. Conventionally, 4T-SRAM cell offers high speed and fewer space compared to 6T-SRAM cell. 4T-SRAM is actualized using 130nm CMOS Technology.***

Keywords: SRAM, Performance, Write Margin, Buried Power Rail ,Static-noise-margin (SNM).

I. INTRODUCTION

The on-chip four-transistor static random-access memories (4T-SRAM) are employed in microprocessors to enhance and standardize the performance of system-on-chips (SoCs). Reducing the number of transistors in the elementary cell results in an overall reduction of the 4T-SRAM array used in system-on-chips (SoCs) [1]. The array efficiency and the performance of the 4T-SRAM is degraded by the resistive behavior of the metal. To reduce the resistance Ruthenium metal is replaced with the normal Gold or Aluminum metals that are used. The current was limited by the expanded bit line (BL) and thus debases the write verge and read verge of 4T-SRAM. In low power 4T-SRAM circuits, Negative bit-line write backup is employed to reduce the resistance and increase the read speed of 4T-SRAM. But, due to this Negative bit-line routing bottleneck and area are increased. Buried power rail (BPR) will resist the increment in resistance of the metal. The 4T-SRAM cell write-margin can be improved by the buried power distribution. Sixty percent of the area on system-on-chips (SoCs) is going to be tenanted by the SRAM cells

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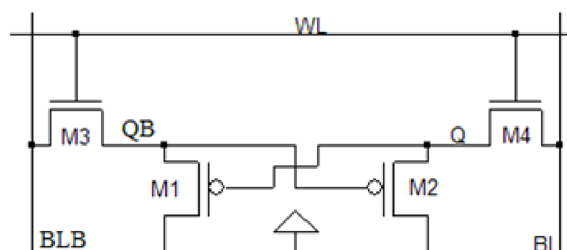

Fig. 1. 4T SRAM cell without load.

II. STATIC-NOISE-MARGIN OF SRAM CELLS

Static-Noise-Margin is employed to explain the reliability of SRAM cells. SNM is characterized because the minimal dc voltage required to invert the state of 4T-SRAM cell. Flipping of the storage nodes at a particular purpose offers SNM [1] - [3]. The foremost basic purpose in an SRAM cell is throughout a read, and after read SNM is given a lot of significance than the write SNM.

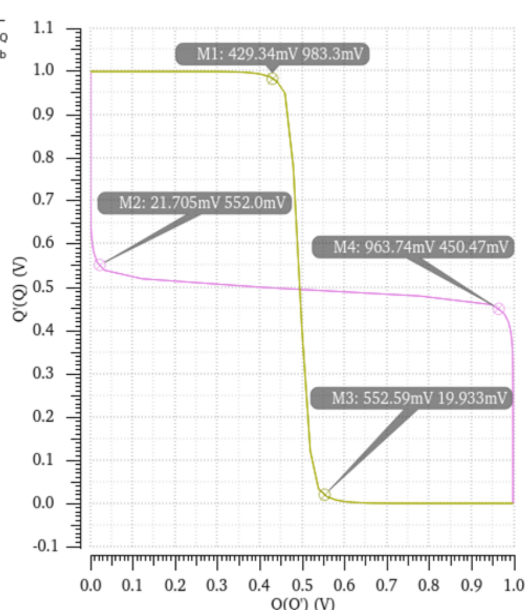

Fig. 2. Static-Noise-Margin of 6T-SRAM

The small noise variations will affect the SNM of 4T-SRAM cell. Voltage stability of 4T-SRAM is high when compared to other SRAM cells. Generally, load less 4T-SRAM cell works at a voltage of 1.2 volts.

The Static-Noise-Margin depends on (W/L) ratios of the transistors that are used to design the SRAM cell. When the miniaturized SRAM cell is considered the SNM of 4T-SRAM cell is approximately two times stronger than the 6T-SRAM cell. The dependency on the threshold changes of 4T-SRAM is less than that of the 6T-SRAM cell. The idea is to design the SRAM cell which can operate at low static noise margin for the required operation.

III. WRITE MARGIN

The concept of Negative Bit Line voltage is mostly used to increase the write verge. The effect of the Negative Bit Line voltage was reduced by the increment in the metal resistance and scaling phenomena. The alternative for the control of the read and write verges with the negative edge is to replace with the self-timing logic which is very easy for its own self-analysis. Here buried powered Technique is assisted to enhance the write margin of the SRAM. The write verge of the SRAM is moderately increased by employing the buried power rail along with the silicon substrate. The write margin will be affected if the resistance of the metal is increased, where the operation of the SRAM also slows down due to this metal resistance. The buried power rail will not consume extra area on the substrate for its existence but its work will be done effectively until there is any obstruction for it. The power consumption and the minimum voltage required will be increased if the write verge ability is degraded. The bit-cell at write verge analysis is away from both buffers and drivers of word line

IV. SRAM READ OPERATION

First, we have to know which node is holding ‘0’ and ‘1’ values in the circuit. For that we will connect the bit lines to VDD. Then make the word line HIGH, now the node with ‘0’ value will be discharged through the NMOS transistor [5]. It can also know by using the sense amplifiers which can sense the value at each node. Now by making bit line LOW or HIGH we can read or write the data at the required node. This read operation can be controlled by the self-timing logic which can self-assess itself and make the bit line HIGH or LOW. The bit line holding ‘1’ tell that it is associated with the ‘1’ at the node and the bit line holding ‘0’ tells you that it is associated with the ‘0’ at the node.

V. SRAM WRITE OPERATION

The read or write operation will be possible only when the word line is HIGH. If the word line is not given to HIGH then it will be in hold state. Bit line will act as an input line to write into the memory. To write it into the memory we will make the BLB LOW [5] then M1 is in ON condition the value held at the Q is ‘1’. The ‘1’ is stored at Q is HIGH as there is a voltage difference between M2 andM4. By forcing the BLB to zero we are able to write the required value at the node Q. The graph for the read and write operation will be shown in the below figure in detail. Figure 3. Read and Write graphs of 4T SRAM

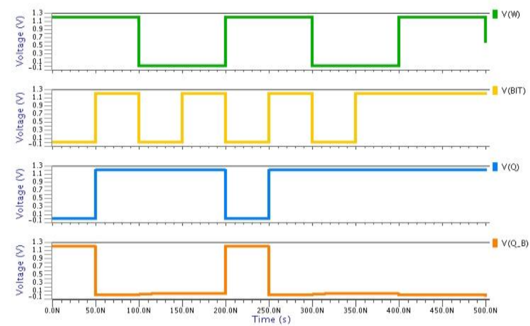

Fig. 3. Read and Write graphs of 4T SRAM

VI. BURIED POWERED RAIL

Buried metals extending the silicon are utilized in DRAM to route the word line. Buried power rails are employed for the interconnection between the standard cells. The profit of utilizing the buried powered rail [2] in SRAM is surveyed in this paper. The high-aspect-proportion of Ruthenium (Ru) is utilized in this design. The crucial steps for BPR formation will be discussed now. The BPR procedure begins preceding the fin formation. The first step is STI fill followed by CMP. Second step is 1nm Lineal deposition with TiN. In the third step the recess etching process is carried out. In the final step the dielectric plug is established on the recessed BPR. Here the top down approach is followed for BPR. The metal is totally encapsulated by front end of line processing (FOEL).

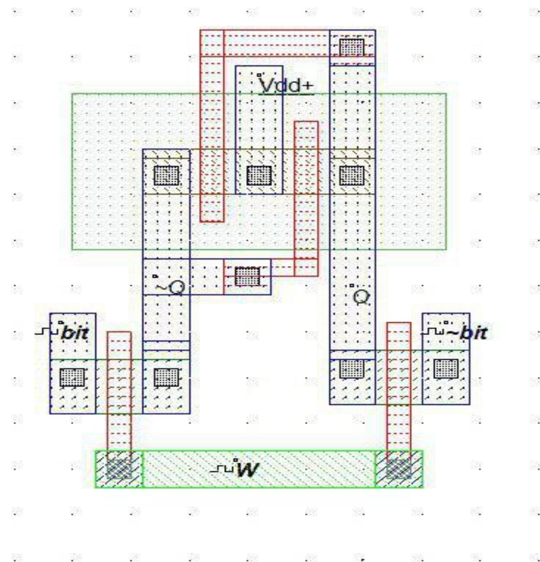

Fig. 4. Layout of 4T SRAM with buried power

VII. RESULTS

The BPR and ordinary SRAM circuits are described in this section. Parasitic parts of metal layers and dynamic devices are extricated from SRAM formats utilizing Mentor Graphics Tool expecting a 130nm CMOS Technology.

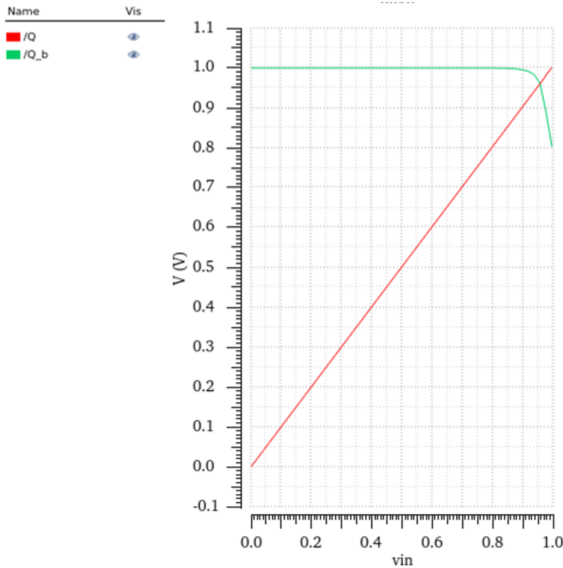

Fig. 5. DC Response for 4T SRAM

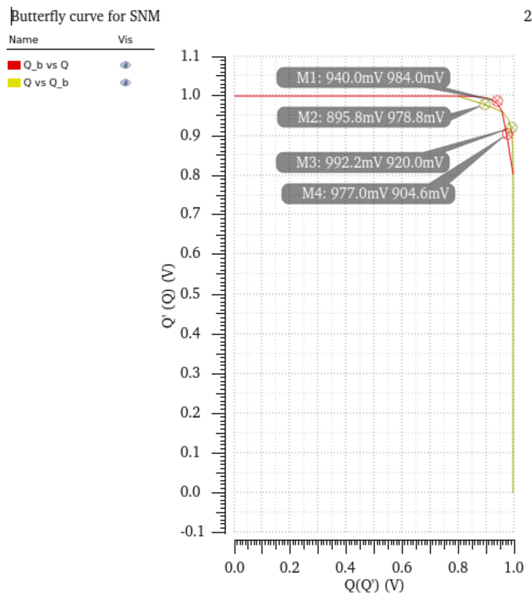

Fig. 6. SNM for 4T SRAM cell

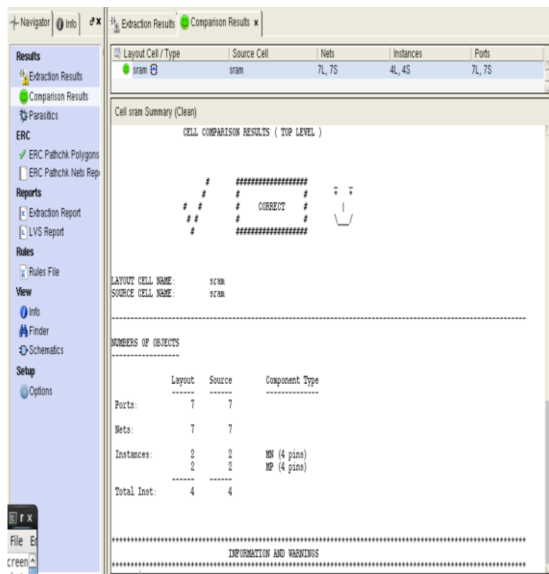

Fig. 7. Verification through LVS

VIII. CONCLUSION

The Buried powered SRAM is suggested in this paper to enhance the write verge and read verge for fast access. Buried power rails help to reduce the bit line and word line obstruction by59.2% and43.7%, separately, in a 130nm technology when contrasted with the SRAM with standard power conveyance systems. The write verge and read access verge are consequently improved by up to 340mV and 30.6%, separately, when contrasted with the traditional SRAM circuits without causing any zone punishment. Covered controlled SRAM is along these lines a potential contender for high-thickness and low-power memory sub-systems in propelled microchips.

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