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Reduction of Test Data with Hybrid Test Points

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Abstract*: ATPG vectors for a combinational circuit exhibit correlations among the bits of a test vector. We propose a BIST circuit design methodology using spectral methods which utilizes the correlation information. This circuit serves dual purposes. It generates BIST vectors that are similar to the ATPG vectors with higher test coverage as compared to random and weighted random vectors. The same circuit can also function as a test data de-compressor for compressed ATPG vectors applied from an external tester. Logic built-in self-test (LBIST) is now increasingly used with on-chip test compression as a complementary solution for in-system test, where high quality, low power, low silicon area, and most importantly short test application time are key factors affecting ICs targeted for safety-critical systems. Test points, common in LBIST-ready designs, can help to reduce test time and the overall silicon overhead so that one can get desired test coverage with the minimal number of patterns. Typically, LBIST test points are dysfunctional when enabled in an ATPG-based test compression mode. Similarly, test points used to reduce ATPG pattern counts cannot guarantee desired random testability. We present a hybrid test point technology designed to reduce deterministic pattern counts and to improve fault detection likelihood by means of the same minimal set of test points. The hybrid test points are subsequently deployed in a scan-based LBIST scheme addressing stringent test requirements of certain application domains such as the automotive electronics market. These requirements, largely driven by safety standards, are met by significantly reducing test application time while preserving the high fault coverage. The new scheme is a combination of pseudorandom test patterns delivered in a test-per-clock fashion through conventional scan chains and per cycle-driven hybrid observation test points that capture faulty effects every shift cycle into dedicated scan chains. We also exhibit test data compression capabilities of the proposed BIST architecture. This architecture provides a maximum test data compression exceeding and a proportional test time reduction for serial interface reseeding.

Keywords: Design for testability, embedded test, logic built in self-test, scan-based testing, test points.

I. INTRODUCTION

Scan is one of the most influential and industry-proven structured design for test (DFT) technologies. With a direct access to memory elements of a circuit under test (CUT), scan makes it possible to generate high quality tests and to debug the first silicon, all now supported by EDA tools.

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Its drawbacks are mainly related to the fact that the vast majority of test time is spent on shifting as virtually all memory elements form shift registers in a test mode. Indeed, 20,000 double-capture test patterns in a design with 400-cell long scan chains would require 8,000,000 and 40,000 shift and capture cycles, respectively. Thus, as low as 0.5% of cycles are spent on testing. The actual test time is also of concern as the scan shift frequency is usually much lower than that of a capture (functional) mode.

Logic built-in self-test (LBIST) – another DFT paradigm – typically employs scan as its operational baseline to achieve, with the aid of some extra on-chip test logic, high quality test while using a limited volume of test data. Classical LBIST applications include different forms of in-field test, detecting infant mortality defects or enabling the use of low-cost and/or low-speed testers that only provide power and clock signals. Interestingly, LBIST keeps up with the demands of new technologies for a valuable test alternative, for example, in the fast growing automotive electronics market. ICs in this area must adhere to stringent requirements for quality and reliability, which are driven by safety standards such as ISO 26262 and Automotive Safety Integrity Level targets. ISO 26262 compliance requires the adoption of more advanced test solutions. In particular, LBIST should respond to challenges posed by automotive parts and support a number of in-field test requirements: the ability to run periodic tests during functional operations, very short test times due to strict limits on power up or idle times, high test coverage, or even the ability to incorporate wireless communication into on-chip on-line solutions to ensure highly reliable device operations for the duration of its lifespan. One of the major problems a conventional LBIST faces is the presence of random-resistant faults. To counteract unacceptably low fault coverage for otherwise feasible pattern counts, LBIST schemes use either weighted or perturbed pseudorandom patterns. One can also modify a circuit by inserting test points that help to activate faults and observe them by means of control points (CPs) and observe points (OPs), respectively. Several computationally inexpensive techniques were proposed to pick the most suitable locations for CPs and OPs. They are based on fault simulation testability measures or hybrid methods using cost functions, gradient-based schemes, or signal correlation. Since test points need extra gates and flip-flops, a test point population is usually limited by user-defined thresholds. But it is an LBIST/test compression combined approach that can result in the shortest test time and very high test coverage, on par with the best LBIST and ATPG assets. There are common features that LBIST and test compression may offer.

For example, ATPG supports a plug-and-play capability for blocks similar to LBIST reuse with pattern retargeting (using block level patterns at higher levels). LBIST low-power test remains similar to that of test compression. The same applies to MISR based diagnosis that has the precision of ATPG but uses LBIST signatures.

Finally, for products that need in-field system test, a hybrid approach will always is preferable because of high test quality of ATPG with the autonomous testing of LBIST. Although LBIST test points may reduce pattern counts, only ATPG test points, developed specifically for deterministic test, are able to decrease the number of test vectors in a consistent manner. In this paper we discuss about proposed LBIST .in section II we will discuss about earlier work .In section III we will discuss about the proposed work .section VI provides the results and finally we will conclude the paper in section v.

II. EARLIER WORK

In this approach, observation hybrid test points capture faulty effects every shift cycle into dedicated flip-flops that form separate scan chains. Their content is gradually shifted into a compactor shared with the remaining chains that deliver responses once the entire test pattern has been shifted-in. Furthermore, hybrid control points facilitate propagation of faults towards scan chains working with observation points. Consequently, the scheme either significantly reduces test application time while preserving high fault coverage or allows applying a much larger number of vectors within the same time interval.

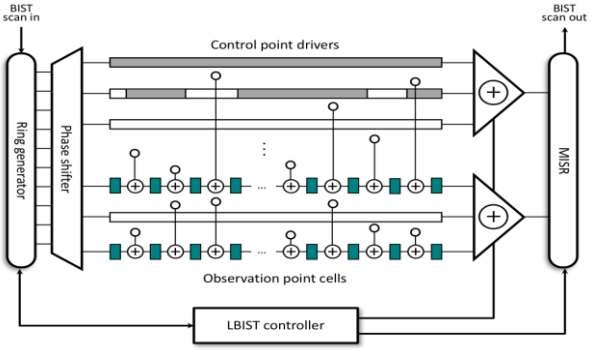

Fig.1. LBIST architecture

A basic architecture of the existing LBIST scheme appears in Fig. 1. The vast majority of scan cells from conventional scan chains (white colored), i.e., they operate either in the shift (after asserting the scan enable signal) or in the capture mode. Since control test points set internal lines to specific logic values, all flip-flops associated with them work only in the shift mode an can be arranged in two different ways: either dedicated scan chains host only drivers of control points (such as the top chain in Fig. 8) or scan cells driving control points are interspersed among other scan cells (the second chain in the figure). The green-colored cells serving the observation points are arranged into independent scan chains that accumulate test responses using XOR gates placed in the front of scan cells as show in the figure 3. It allows one to encapsulate shift and capture functionality within a single clock cycle. The global test point enable (TPE) signal activates observation points in the test mode. Test results received from CUT through inputs D are then XOR-ed with data provided by adjacent scan cells. A clock gating (CG) may also be used to actually enable or disable compaction scan chains after asserting the corresponding control (CGEN) signal. Although compaction chains may not be fed by a phase shifter this connectivity enables uniform scan-integrity tests.

III. PROPOSED METHOD

We have two sets of test points in the scan chain architectures called Observation points and control points. Because of this it will take more time and area at the phase of testing.

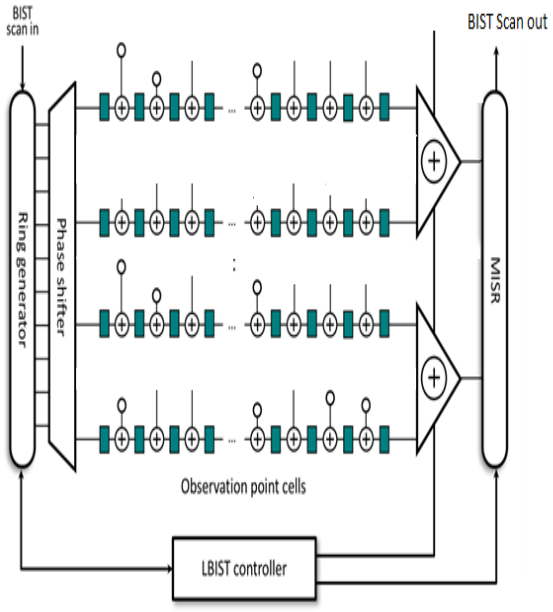

Fig. 2. Proposed LBIST

To overcome this problem we can change the Architecture by using only one set of test point in each scan chain which can have both the operations so that area and testing time may get reduced. The proposed LBIST is as shown in the above figure 2.

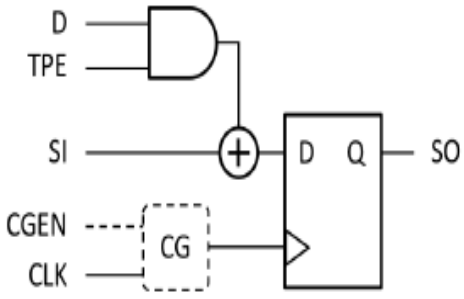

Fig. 3. Scan cell for observation point and scan points

For this operation we can change the design of Scan cell which is used in the above proposed LBIST.

IV. SIMULATION RESULTS

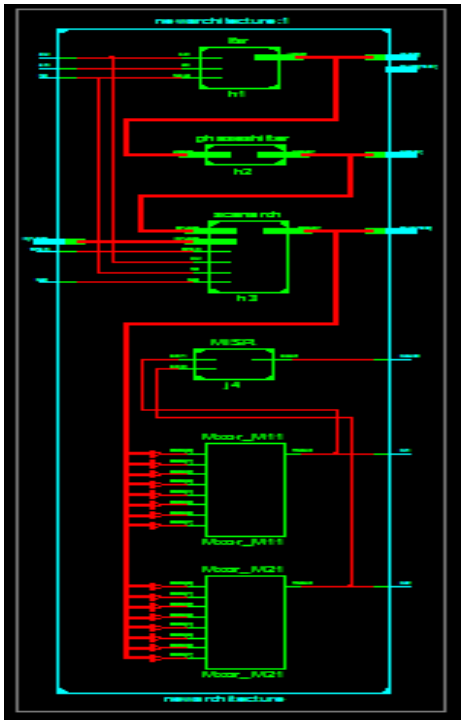

Fig.4. RTL Schematic of Proposed Hybrid architecture

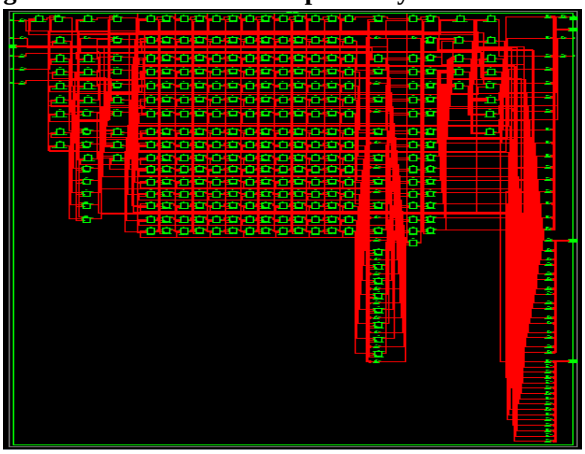

Fig.5. Technology Schematic of Proposed Hybrid architecture

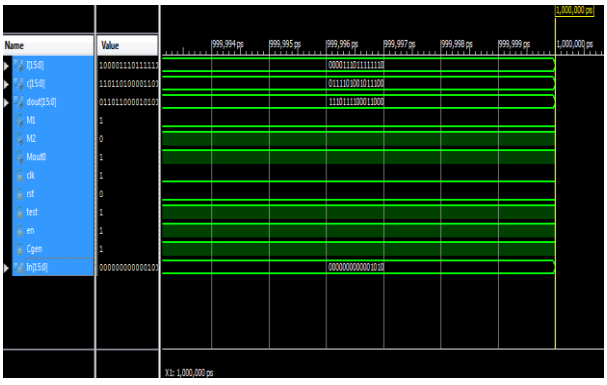

Fig. 6.Simulation Results

V. CONCLUSION

In the first part of the paper, we present a DFT scheme that aims at reducing deterministic test pattern counts and increasing circuits' random testability. This is accomplished by deploying hybrid test points in designs where on-chip sequential test compression is combined with LBIST infrastructure. The proposed scheme reduces test application time – a crucial factor when running in-system tests for safety-critical and automotive applications.

The new TPI method identifies internal conflicts that preclude efficient ATPG-based test compaction and detection of random resistant faults. Locations corresponding to such hybrid conflicts are modified by test points, which increase the number of faults targeted by a single pattern, reduce ATPG test pattern counts and a test data volume, and finally allow one to run high-quality tests during LBIST sessions. Subsequently, we propose an LBIST scheme that significantly reduces test time (or applies much more vectors within the same time interval) by having pseudorandom test patterns delivered in a test-per-clock fashion through conventional scan chains and by recording test results by means of per-cycle driven hybrid observation test points that monitor the most sensitive fault propagation paths. As shown in the paper, test results are regularly saved in a per-cycle manner by means of dedicated cells and the compaction scan chains they form.

The observation test point cells do not receive enable controls at speed – they have to be asserted only once to launch a test. Consequently, these signals do not have to be routed like clocks, and thus their distribution is not a primary concern. Experimental results for large industrial designs confirm feasibility of the solutions proposed in the paper. These results were obtained for static faults, which are widely deployed for online monitoring of safety critical applications, including automotive designs.

The paper does not discuss benefits of the proposed technique for delay fault coverage. In principle, however, there are no restrictions in extending the proposed methodology for transition or path-delay patterns other than adding more requirements such as closing timing for scan paths at speed.

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