

FPGA-Based Connected Component Algorithm for Vegetation Segmentation



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Abstract: In the process of automatic trees recognition and tracking, image target is captured by RGB camera mounted on a UAV, in processing step image captured is subjected to threshold and extract selected information, This techniques may be applied to recognize objects with different shapes and sizes. In the case of remote sensing vegetation, the image usually contains multiple connected areas or overlapped trees; the proposed system uses the shape characteristics of the image target to self-identify the suspicious overlapped features. This technique allows distinguish, analyze and detect different features in images by assigning a unique label to all pixels that refers to the same entity or object. In the process of automatically recognizing and tracking the target of an image, it is first segmented and extracted. The resulting binary image usually contains several connected regions. The system uses the shape characteristics of the target in the image to automatically identify the suspected overlapped trees. Therefore, it is necessary to detect and evaluate each connected area block separately, in this paper, the improved FPGA-specific rapid marking algorithm is used to detect and extract each connected domain.

Keywords: Precision Agriculture, Segmentation, Connected Components, FPGA.

I. INTRODUCTION

Trees planted in agricultural land provides numerous environmental benefits, since they provide oxygen, improving air quality, climate amelioration, conserving water, preserving soil, and supporting wildlife. Also they are an important source of food for humans and other organisms, therefore farmers are very interested in testing innovative solutions to improve quality and quantity of products, while reducing time and energy, managing water resources and fertilizers, and reducing emissions and pollution. In this context, precision agriculture is one of many modern farming practices that make production more efficient. Unmanned aerial vehicle (UAV) remote sensing has excellent potential for vegetation mapping, In precision agriculture application of digital image processing,

can improve decision making to find solutions for some challenging problems one of these is the recognition of important parameters related to agronomy with Accuracy, precision, and economic efficiency, then connected component analysis is one of the major steps used in numerous image processing systems.

Image Segmentation is an important technique for image processing analysis in precision agriculture, current segmentation problems includes the partitioning of an image into a number of homogeneous components. There are various methods which deal with segmentation and feature extraction for example: Markov Random Field (MRF) model [1], Edge Based Segmentation [2], histogram-based methods [3]. However, the segmentation is a challenging assignment because of the variety and complexity of video frames. To reduce the complexity of the hardware architecture, watershed transform [4] using connected component-based technique for automatic segmentation.

This paper proposes a wide range of parallel algorithms for morphological image processing, the aim of this type of image processing is to extract or enhance features from images based on shape, they are typically used for real time surveillance tasks in industrial systems [5], medical image processing[6], texture analysis[7]. Moreover, in automatic tasks such as segmentation or classification of desired objects in the image are time consuming, it has been found that a common problem is revealing which is the presence of overlapped trees due to some connected components in pixel range. In order to identify objects in a digital pattern, it is necessary to locate groups of pixels that are connected to each other; a connected region in a binary region refers to the maximal set of foreground pixel in which any two objects are connected by an 8 neighbor's pixel of foreground pixel, and for convenience. In this paper the proposed algorithm consists of three stages: preprocessing, segmentation and post-processing steps, to manipulate an image, this paper describe the work on an array of integers that contains the components of each pixel, various objects are founded in real-time by region labeling process, Therefore, Dynamic identification is necessary to detect and evaluate each connected components separately. In this paper, the enhanced fast tagging algorithm adapted to the FPGA is used to detect and extract each connected component in real-time.

II. RELATED WORK

In the automatic image recognition and tracking process, the target image is first segmented and extracted,

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the resulting binary image typically contains several connected regions and the system uses shape characteristics of the target image for automatically identify the suspect target. Therefore, it is necessary to separately detect and evaluate each connected zone block.

In order to distinguish different objects in a binary image.

There are several methods commonly used to detect connected components in binary image of [8][9]: region growing [10] is one of the approaches that segment image by detecting neighboring pixels, values of foreground/object pixels and background pixels are 1 and 0, it's a progressive scan, at each pixel "1" found unlabeled, an unused label is assigned, the algorithm is completed when the entire image is scanned.

This process is iterated for each boundary pixel in the regions of the image. This method is accurate, various connected component are detected but its time consuming, the algorithm spent the most time of finding the correct position to insert a border pixel in its data because the neighborhood of each "1" pixel must be detected one by one, and a repeated scan of "1" pixels occurs., it is needed to be completely reconfigurable to make use of parallel processing.

Tracking algorithm [11]: Each pixel in the binary image with a value "1" is tagged with a label associated with its coordinates, such as number consisting of n, m strings.

After processing, the target image is scanned and labeled, every 10 pixels is replaced by the smallest label in its surroundings pixels. After labeling, a binary image will be transferred to a labeled image.

III. MATERIALS AND METHODS

In order to achieve the implementation of the FPGA, this article proposes a domain tagging algorithm connected with a fast binary image.

Compared to the traditional binary image tagging algorithm, this algorithm has the characteristics of simple operation, regularity and flexibility; it is suitable for FPGA implementation.

With a 100 MHz clock rate, images processed at 384×288 pixels can achieve a frame rate of more than 400 frames per second, which are sufficient for real-time target recognition systems.

The processing speed can meet the requirements of most real-time target recognition systems. The algorithm can also be applied to DSP systems embedded in software programming.

A. Description of the algorithm

The proposed algorithm consists of three steps, as shown in the Figure1. The first step in which removal background is undertaken, the second step is segmentation it consists on group trees separation to subsequently detect centers of each tree in each frame. Then post processing step where edges of all trees appearing in the image are plotted.

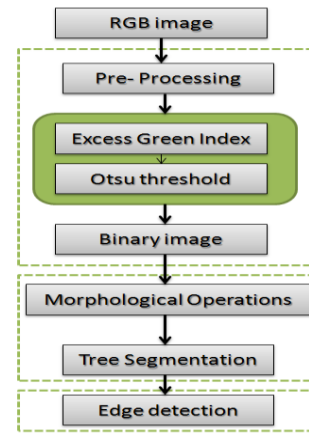


Fig. 1. Block diagram of green crop segmentation and detection algorithms.

1) Pre-processing

Image pre-processing is performed by converting the image from RGB color model to an EXG model [12]. To expedite the process, the image is binarized using Otsu's method [13] to perform automatic image thresholding, in order to automatically cluster pixels into two groups' background and foreground (Figure2), which means create a black and white image. The main idea of Otsu's algorithm is that all pixels are classified into 2 classes using that threshold.

Automatic thresholding Algorithm:

1. Select initial threshold value, typically the mean 8-bit value of the original image.
2. Divide the original image into 2 portions;
 - a) Pixel values that are less than or equal to the threshold are background
 - b) Pixel values greater than the threshold are foreground
3. Find the average mean values of the 2 new images
4. Calculate the new threshold by averaging the 2 means.
5. If the difference between the previous threshold value and the new threshold value are below a specified limit,
6. Otherwise apply the new threshold to the original image.

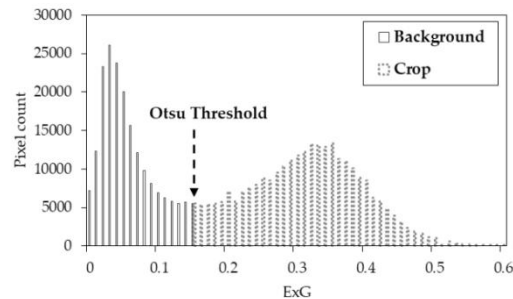


Fig. 2. Excess green (ExG) histogram for vegetation classification with the Otsu threshold value.

2) Segmentation

In order to improve the image contrast, a background template is obtained using a morphological opening over the entire image.

The full image after background removal is binarized (objects take the value 1 and background 0), the black and white image presented in Figure 3.b is obtained. As results of this binarization, there will be two overlapped and tree overlapped or more overlapped trees.

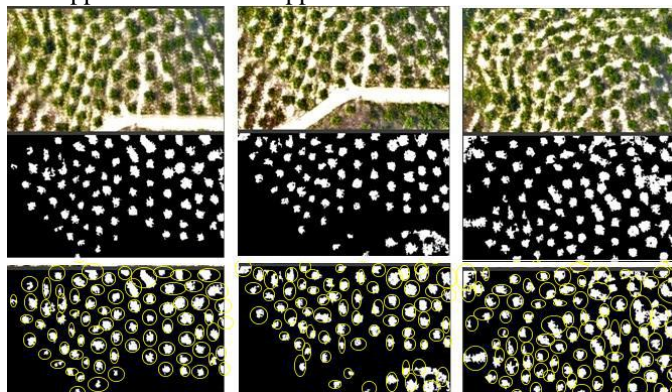


Fig. 3. Examples of trees segmentation and detection.

Misclassification can occur at the intersection of probability distribution curves. To correct these errors, the following methods are ensured:

- In the detection of a single tree or two overlapped trees, the convex hull is used, if it is equal to the tree edge, the connected component is classified as a single tree, otherwise it is classified as a group of two trees.
- In classification of groups of two or more overlapped objects, the Hough transform is used to detect the number of circles present, if the results differs with the minimal difference in the number of trees detected according to the area, Hough determines the amount taken to be true [14], but if the difference is greater than 1, the number of trees defined by the area is maintained. This procedure is also useful to classify groups of more than three trees.

Based on this idea, we can classify according to the area of the connected components found in the image in order to gain an understanding of the amount of trees that could be in each frame, individual or groups of trees are detected in Figure 4.

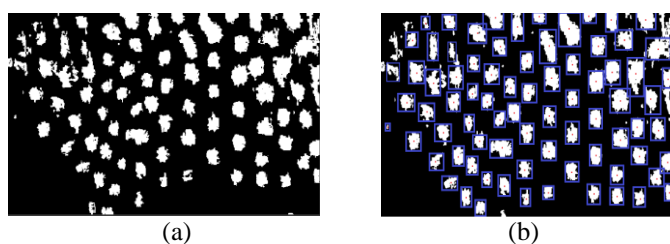


Fig. 4. Detected connected component. (a) ExG index was applied to separate plant vegetation from the soil background, (b) trees are detected and identified using the proposed algorithm.

IV. FAST TAGGING ALGORITHM

Before the marking algorithm, the hardware is used to open an independent image label cache and the connection relationship table, then, when acquiring and transmitting videos, the image is scanned line by line and then for each pixel in the video transmission order. Pixel neighborhoods are combined counterclockwise and horizontally for connectivity detection and marks in to equivalence table. The

detected results update the equivalence table and the mark cache. Finally, depending on the label in the table, merged from small to large and the merged table is used to replace the labels in the image marking cache. The following image is then the result of final tagging, and the connected components have a unique continuous natural number in the scanning order.

In this article, the domain labeling algorithm for binary image is divided into three parts:

1. Preliminary image tagging: assign a temporary tag to each pixel and record the equivalence relationship of the temporary tag in the equivalent list.
2. Organize the equivalent table: This part is divided into two steps:
 - (1) All temporary marks with an equivalent relationship are equivalent to their minimum value;
 - (2) The linked areas are renumbered in order of natural number to obtain an equivalence ratio between the temporary mark and the final mark.
3. Image substitution: the image is replaced pixel by pixel and the temporary mark is replaced by the final mark. After three steps, the algorithm generates the marked image.

A. Initial image tagging

Convention of the marking algorithm: when the algorithm detects the connected domain counterclockwise, it uses w_1 , w_2 to represent the image data of two consecutive lines. In the next clockwise direction, the connected domain detection uses k_0 , k to indicate that two consecutive lines are marked counterclockwise.

The position of the working window is shown in Figures 5 and 6, respectively; the initial temporary mark in the counter-clockwise direction is indicated by Z . The initial value of the Z tag is 1.

The binary image connected domain labeling algorithm uses the 8-connection criterion to eliminate the boundary effect of the image by reducing the range of markers.

In order to simplify the marking process, the marking process ends in the equipment at a frame-by-frame transmission time, and the marking process is divided into two consecutive types using the intermediate data buffer, type 1 being used for direct transmission of image sequences and the equipment initiating transmission of image sequences. Type 1 uses domain detection connected in reverse clock order to initially mark binary pixels in the 2×3 work window. Type 2 performs horizontal detection of the connected domain and merging of the image data initially marked with type 1, and then stores the marked result in the image storage area.

Initial tag of the image 1:

- Step 1 reads the pixels w_1 (2), w_1 (1), w_1 (0), w_0 (2), w_0 (1) and the corresponding binary pixel values.
- Step 2 Read the pixel w_0 (1) and compare it with w_1 (0), w_1 (1), w_1 (1), w_1 (2) and w_0 (2) in an anticlockwise direction. If w_0 (1) = w_1 (0), then k_0 (1) = k (2);
if w_0 (1) = w_1 (1), then k_0 (1) = k (1);
if w_0 (1) = w_1 (2), then k_0 (1) = k (If w_0 (1) = w_0 (2), then k_0 (1) = k_0 (0);
otherwise ;
(i. e. w_0 (1) \neq w_1 (2), w_1 (1), w_1 (0), w_1 (2)), k_0 (1) = Z ;
 $Z++$.

Step 3 Write the equivalence relationship table and write Z in the equivalence table with Z as the address.

W1(2)	W1(1)	W1(0)
W0(2)	W0(1)	

Fig. 5. Working window for initial marking in counter-clockwise direction.

Initial image tag 2:

- Step 1 Once you have determined the marker counter-clockwise, if $w_0(1) = w_0(2) = 1$ and the gradation of the $k_0(1)$ marker $\neq k_0(0)$ is marked, the next step is performed.
- Step 2 Suppose that $k_0(1) > k_0(0)$, so $\text{Lab}(k_0(1)) = k_0(1)$ or $\text{Lab}(k_0(1)) = k_0(0)$, then $\text{Lab}(k_0(1)) = k_0(0)$, otherwise the tracking table is followed and replaced.

- Step 3 Suppose that $k_0(1) < k_0(0)$, so the $\text{Lab}(k_0(0)) = k_0(0)$ or the $\text{Lab}(k_0(0)) = k_0(1)$, then the $\text{Lab}(k_0(0)) = k_0(1)$, otherwise the tag table is followed and replaced.

Follow-up replacement method: the follow-up replacement of step 2 is $t = \text{lab}(k_0(0))$; if $\text{lab}(t) \neq t$, leave $t = \text{lab}(t)$, repeat the execution, direct $\text{lab}(t) = t$; step 3 the follow-up replacement command $t1 = \text{lab}(k_0(1))$ and the above follow-up process is also executed for $\text{lab}(k_0(1))$.

k (2)	k (1)	k (0)
k0 (0)	k0 (1)	

Fig. 6. Working window for initial marking in the horizontal direction.

B. Sorting equivalence tables and image substitution

First, the list of equivalents is analyzed from parity table address 1, and then the equivalence relationship between each temporary mark is checked. Since the classification process starts at equivalent table address 1, the analysis of the complete equivalence table can be performed again.

The image substitution link replaces each pixel of the temporary marker image to generate a final marker image. The specific method is as follows: if the temporary reference value of the pixel whose coordinates are (n, m) in the image is S, the lab (S) is written at the position (n, m) in the image. The image obtained after the substitution, in which the connected regions are marked with a unique natural number in order, from top to bottom, appears from left to right.

C. Analysis of the algorithm characteristics

The algorithm design has the following characteristics:

The algorithm of this article marks the identification and tracking tree targets. The work of marking the other pixels of the image is done completed by the algorithm described above, so that the operation has regularity and the same address. When using hardware implementation, only the functions of the algorithm structure must be defined to be recycled, which saves the algorithm's memory resources.

During the initial image marking process, the equivalent table is pre-sorted while recording equivalent information, which allows, on the one hand, when there is a complex connection relationship between regions, to save all detected

equivalents. On the other hand, when the marking algorithm is implemented by a hardware circuit, the image preliminary marking process and the equivalent table preliminary finishing can be performed in parallel and the equivalent table preliminary finishing can simplify the next equivalent table sorting operation, which is equivalent to a compression.

In this algorithm, two measures are taken to reduce the number of temporary markers: first, repeatedly use all marker information generated in the range of 8 neighborhoods and execute the horizontal direction in the order of image transmission after marking in the opposite direction of the 8 lanes. The mark merges and reducing the probability of new mark values being assigned. Second, when the equivalent table is sorted, the equivalent mark is merged and replaced in the order of the address of the equivalent table, so that the equivalent mark is compared. Small value and will not miss the equivalent mark. Third, in combination with the video data stream transmission mode, the ping-pong structure is used for pipeline processing, and the replacement of the image mark is performed at the same time. This makes image markers perform real-time processing.

D. Implementation of the algorithm on FPGA

The FPGA (Field Programmable Gate Array) is a large-scale programmable logic device that can be used in various digital logic systems, including real-time processing, with unique advantages. In the real-time implementation of this algorithm, the FPGA Cyclone2 EP2C8 is used, which includes 8256 logical units, 18 DSP blocks and 165.888 bits of memory. These memory cells can be configured as memories of different sizes and bits, which can reduce the use of external memory, reduce the size of the hardware and facilitate miniaturization of the circuit.

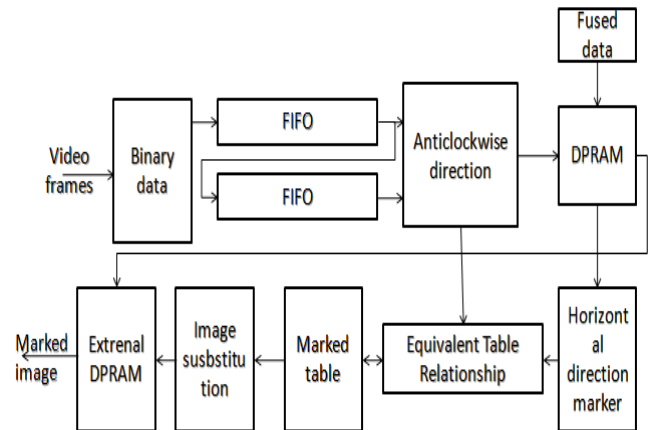


Fig. 7.FPGA Conception of a Reconfigurable Fast Tag algorithm.

Figure7 shows the hardware structure of the FPGA implementation of the fast label algorithm, mainly composed of a FIFO serial-to-parallel conversion of binary video stream delay, an anti-clockwise marking unit, a fused data transmission interface, a horizontal direction, labeling unit, a table of mark equivalence relationships, an equivalent mark, a sorting unit, image mark substitution unit, etc.

The FPGA's internal video acquisition unit digitizes the grayscale data collected according to the segmentation threshold to generate a binary video and converts the serial binary video into two lines by parallel-serial FIFO delay conversion.

The counterclockwise marking unit uses the shift register to compose the received parallel data stream, and performs counterclockwise connectivity detection on the data in the window to generate an initial equivalence relationship table and pixel data. The temporary mark is executed, the fuser unit of the horizontal direction marks; is immediately after the mark in an anti-clockwise direction and the pixel data after the initial mark is formed; and the data in the data window is marked in the horizontal direction. The equivalence judgment, the merging of tag values belonging to the same region and the monitoring of the replacement tag equivalence relationship table, all previous equivalent tag values are unified into the smallest tag value and the video stream of merged parallel tags is finally stored. In the memory group consisting of the next two-port RAM memory, the two-port external RAM marks the pixel data stored in the dual-port external RAM memory last in the next line of video data processing.

V. RESULTS AND DISCUSSION

Once a frame image of the video data is marked, the equivalence relationship table is sorted and merged into the empty video data space. When the next video data image is transmitted, the previous image data is extracted from the external dual access RAM so that the tag image substitution is completed. The tag cache is built by a ping-pong structure via dual access RAM in the FPGA, marking two lines of image data, while the external dual access RAM interface stores the marked line of image data in the tag cache structure, the ping-pong module shares three 384×10-bit dual access RAMs, and each dual access RAM corresponds to one line of image tag data. The horizontal marker, fuser unit and the external DPRAM interface are used for data storage. When the horizontal fuser simultaneously stores two of the dual-port RAMs, the external DPRAM interface performs a memory operation on the remaining third dual-port RAM to form label cache ping-pong structure storage operations. The external storage interface moves the data into the cache memory with a clock frequency 4 times higher to ensure that the external data is also moved after marking the two remaining dual access RAMs. Experience shows that 3 lines of tag data can be moved in a single line of time for transmitting tag data. To respond to the real-time pipelined processing of the tag, the dual-entry device RAM also uses a ping-pong structure. The data is extracted while the image data of a frame is stored, and the image is replaced by the mark image, and the shape of the mark result image is completed during the recovery process. Dual access RAM is defined on two areas of images A and B, and two areas of A and B are operated simultaneously using two data address ports. As a result, the marking algorithm generally delays a frame of video data transmission time and offers high performance in real time.



Fig. 8. Rapid detection of overlapped trees.

The simulation results are presented in Table1, the FPGA working clock is 100 MHz; n is the number of connected regions; T1 is the execution time of the DSP via the traditional algorithm of the convergence mark; T2 is the execution time of the FPGA via the fast label algorithm designed in this article.

Table- I: comparison results.

Frame	n°	T1 (DSP)	T2 (FPGA)
1	14	28.1 ms	2.1 ms
2	19	31.2 ms	2.1 ms
3	21	38.4 ms	2.1 ms
4	15	28.9 ms	2.1 ms

The simulation results show that, when the traditional convergence labeling algorithm runs in software mode in T1 DSP-6416 system, the processing speed of this algorithm is uncertain, depending on the shape and number of domains connected in the image. When the software mode is executed on DSP6416 system, the algorithm can process images of 384 × 288 pixels up to 50 images, but when implemented in FPGA, it achieves a processing speed of 400 frames/second with a 100 MHz clock frequency.

VI. CONCLUSION

In the process of automatically recognizing and tracking the target of an image, it is first segmented and extracted. The resulting binary image usually contains several connected regions. The proposed system uses the shape characteristics of the target in the image to automatically identify the suspected targets. Therefore, In the case of remote sensing vegetation, there is a need to develop automatic systems for plant enumeration in tree seedling crops to save human resources and improve yield estimation. So it is necessary to detect and evaluate each connected features block separately, the improved FPGA-specific rapid marking algorithm is used to detect, extract and label each connected features in the studied trees video. Experimental results indicated that the algorithm is suitable for real-time processing, 3 lines of tag data can be moved in a single line of time for transmitting tag data, thus can improve decision making to find solutions for some challenging problems one of these is the recognition of essential parameters related to agronomy with Accuracy, precision, and economic efficiency.

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