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Modeling of on-off Current and Cutoff Frequency in Organic Thin Film Transistors

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Abstract: ***Organic thin-film transistors (OTFTs) are providing incitement in various integrated circuit applications because of advantages like low cost and being flexible.In this paper we present an analytical modeling of on-off current and cutoff frequency in organic thin film transistors. The proposed model accurately describes both the parameters uniquely and is based on the standard equations of transistor . The model parameters are listed out and simulation of the final model is performed in MATLAB . Furthermore, it has been concluded that the high cutoff frequency of OTFTs can be achieved with short channel length and high gate voltage ,further high on-off current ratio can be attained by lowering semiconducting layers' thickness and increasing the mobility.***

Keywords : LCDs,OTFT,PEDOT/PSS

I. INTRODUCTION

Thin film transistor is a common transistor in printed and flexible electronics.As the name implies it is made up of thin films/layers and is therefore a very suitable construction for printed electronics.Thin films of an active semiconductor layer and dielectric layer are deposited and metallic contacts are made over a supporting substrate. The active material can be organic or inorganic.The organic thin film transistors (OTFTs) can be printed on substrates that are flexible like plastics ,paper. A common substrate is glass as TFTs are widely used in LCDs. On the other hand ,silicon wafer substrate is the semiconductor material used in the conventional transistor.

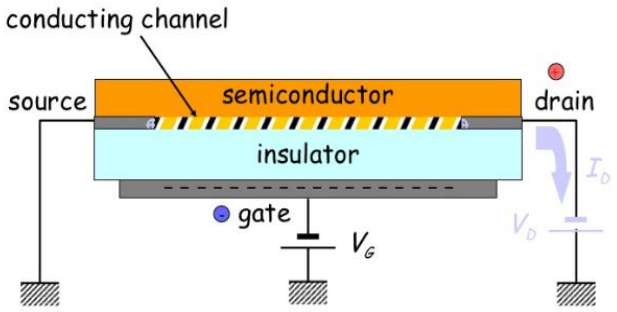

Fig.1.Thin Film Transistor

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II. MODELING AND CHARACTERIZATION

- **Drain Current**

The drain current ($I_{D)}$ varies linearly with drain source voltage ($V_{DS)}$ and the channel behaves like a resistor.This gives

$$I_D = g_d . V_{DS}$$

where g_d is the conductance of the drain.
The channel conductance g_0 is given by

$$g_0 = \frac{W}{L}\mu|Q|$$

where W is transistor channel width, L is length of the transistor, μ is the charge carrier's field effect mobility in the channel,Q is the sheet density of the accumulated layer charge.
The accumulated charge on layer in the absence of traps is given by

$$|Q| = C_I(V_{GS} - V_{TH})$$

where V_{TH} is the threshold voltage and C_I is the Gate Insulator's capacitance per unit area.

$$C_I = \frac{\varepsilon\varepsilon_0}{t_i}$$

ε:-Permittivity of free space,$\varepsilon_{0:}$.Relative Permittivity of Gate, $t_{i:}$.Gate Thickness.

B.Carrier mobility and contact resistance

The mobility of a device determines the processing speed of a device.The intrinsic charge carrier mobility ($\mu_{0)}$ is constant as it is a property of the material.Whereas, the effective charge carrier mobility (μ) include the effect of contact resistance (RC).The gate bias mobility is expressed as

$$\mu = \mu_0(V_{GS} - V_{TH})^{\alpha}$$

where μ_0 is the band mobility of an Organic semiconductor layer , the parameter α depends on the dielectric permittivity and doping density of active material.
Mobility (μ) affects the maximum drain current and the switching speed.

Effective mobility (μeff)— It is calculated by the conductance (g_{DS}) at low V_{DS} and includes the V_{GS} effect.

$$\mu_{eff} = \frac{g_{DS}L}{C_I W(V_{GS} - V_{TH})}$$

Field-effect mobility (μ_{FE})—It is obtained by the transconductance (gm) at low V_{DS}:

$$\mu_{FE} = \frac{g_m L}{WC_I}\left(\frac{1}{V_{DS}}\right)$$

Factors effecting μ_{FE}

- It is directly proportional to the dielectric constant of insulator since higher dielectric constant results in increase in polarization.As a result carrier density increases & hence mobility increases.
- Dielectric roughness also effects the field effect mobility.Mobility increases with decrease in roughness.
- Higher contact resistance of the insulator with the electrodes lowers the field effect mobility. Penetration of the electrode into the dielectric also effect the mobility.Higher the penetration lower will be the mobility. With Au coated (PEDOT/PSS),charge injection increases,& contact resistance decreases,thus mobility increases.

Saturation mobility (μ_{sat})—It describes a condition when the effective length is smaller than L . At high V_{DS}:-

$$\mu_{sat} = \frac{2L}{WC_I}\left(\frac{\Delta\sqrt{I_D}}{\Delta V_{GS}}\right)^2$$

Field Effect mobility in Linear Region(μ_{FE}):-

When ($V_{DS} < V_{GS} - V_{TH}$)i.e in the linear regime ,the mobility is extracted from the transconductance of the device (g_m),which is defined as the change in I_D with V_{GS} for small and constant values of $V_{DS.}$ i.e

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Also

$$g_m = \frac{W\mu_{FE}C_I}{L}V_{DS}$$

Rearranging and solving for mobility gives:-

$$\mu_{FE} = \frac{g_m L}{WC_I}\left(\frac{1}{V_{DS}}\right)$$

which is valid for small and constant $V_{DS.}$

Extracting Field Effect mobility in Linear Regime:-

By plotting measured I_D vs V_{GS} in a graph transconductance g_m, is extracted by fitting a line to I_D vs V_{GS} above the threshold & then extracting the slope of the fitted line.

Transconductance is defined as the ratio of the variation incurrent at the output to the variation in voltage at the input.($\Delta I/\Delta V$).

The equation for mobility in the linear region

$$\mu_{FE} = \frac{g_m L}{WC_I}\left(\frac{1}{V_{DS}}\right)$$

So,by knowing the parameters (W,L,V_{DS} & C_I) and extracting transconductance, μ can be extracted.

Extracting Field Effect mobility in Saturation Regime(μ_{sat}):-

In the saturation regime,

$$\mu_{sat} = \frac{2L}{WC_I}\left(\frac{\Delta\sqrt{I_D}}{\Delta V_{GS}}\right)^2$$

It can be extracted by fitting a line to $\sqrt{I_D}$ vs V_{GS} & then extracting the slope.

The field effect mobility can then be extracted from the expression.by knowing the other parameters (W,L,& C_I).Also, the threshold voltage V_{TH} can be extracted by interpolating the fitted line down to the V_{GS} intercept at zero I_D.

Threshold Voltage (V_{TH})

The threshold voltage (V_{TH}) is defined as the V_{GS} voltage at which the conducting channel is created.It depends on channel length L,dielectric constant of the insulator, ,doping concentration and the thicknesses of the dielectric (t_{ox}) and the active (t_{osc}) layers.Lower V_{TH} is desirable as it reduces the power consumption of the device.The threshold voltage in OTFTs are typically uncontrolled and very large due to high density of trapped charges. in the organic semiconductor.It can be extracted by extrapolating the line to zero drain current & locating the intercept with V_{GS}.

Turn-on voltage (Von)

It corresponds to the V_{GS} at which I_{DS} starts to increase.It is easily visible in the log I_{DS}-V_{GS} graph.

C.Cut off Frequency

Current-gain cutoff frequency

It is also defined as relaxation or transition frequency, which is the frequency at which the current gain is unity.

$$f_T = \frac{g_m}{2\pi C_G} \cong \frac{\mu(V_{GS} - V_{TH})}{2\pi L(L + 2L_{OV})}$$

The free carriers' mobility in the channel of device affects the cut-off frequency (f_T) which is defined by:

$$f_T = \frac{\mu V_{DS}}{2\pi L^2}$$

D.On/Off Current ratio

It is defined as the ratio of the current in the on state to the current in the off state.The on state can be referred as accumulation mode and the off state as depletion mode. It can be expressed as

$$\frac{I_{ON}}{I_{OFF}} = \frac{C_I\mu(V_{GS} - V_{TH})^2}{t_{OSC}V_{DS}\sigma}$$

where σ is channel's conductivity, C_I *is* the gate dielectric capacitance per unit area. I_{ON} can be increased and I_{OFF} can be decreased by decreasing the thickness of dielectric and semiconducting layer,respectively,

that further increases the I_{ON}/I_{OFF} ratio.It is extracted from the graph plotted of I_D vs V_{GS} characteristic on a semilog scale.

Subthreshold Slope (SS)

A sub-threshold slope (SS) is defined as the change in V_{GS} required for one decade change in I_D i.e

$$S = \frac{\Delta V_{GS}}{\Delta(\log I_D)}$$

It describes the turn-on characteristics of the device For better switching behavior,the trap density should be lowered which results in a steeper slope.The standard equation for drain current in the subthreshold regime is

$$I_D = \frac{W}{L} K\mu C_{ox}(1-e^{-qV_{DS}/kT})e^{qV_{GS}/nkT}$$

where K is a constant that depends on device structure and materials ,n is ideality factor.,k is Boltzmann's constant,T is absolute temperature.
Ideality Factor n is given by

$$n = skT \ln(10) \text{ V/decade}$$

n lies between 1 and 2 if ideal diffusion current and recombination current are comparable .An ideality factor greater than 2 indicates that there are defects in the interface which increases the recombination current.With an ideality factor of 1 ,the drain current in the subthreshold region increases one decade if the gate voltage is increased by 60 mV at room temperature(300k).

E.Transconductance

The transconductance (gm) is described as the response of the drain current with the change in V_{GS} at a constant V_{DS}.

$$g_m = \frac{\partial I_D}{\partial V_{GS}}|_{V\,DS}$$

By substituting for I_D using

$$I_{D,\,Lin} = \frac{W\mu C_I}{2L}\left[2(V_{GS}-V_{TH})V_{DS} - {V_{DS}}^2\right]$$

and

$$I_{D,\,Sat} = \mu C_I \frac{W}{2L}\left[V_{GS}-V_{TH}\right]^2$$

the transconductance in the linear and saturation regions can be calculated respectively as :

$$g_m = \mu C_I \frac{W}{L} V_{DS}$$

for Linear region when $V_{DS} < V_{GS} - V_{TH}$

$$g_m = \mu C_I \frac{W}{L}(V_{GS}-V_{TH})$$

for Saturation region when $V_{DS} \geq V_{GS} - V_{TH}$

Thus, the transconductance is proportional to the $(V_{GS} - V_{TH})$ in the saturation region, but in the linear region it is constant . Also,the transconductance in saturation region can be derived by using its following definition :

$$g_{m,\,sat} = \frac{W}{L} C_I \mu (V_{GS}-V_{TH})(1+\lambda V_{DS})$$

III. TYPES OF ORGANIC THIN FILM TRANSISTORS

Based on the position of Source, Drain, and Gate contacts with respect to the OSC layer, the structures are classified into four types.

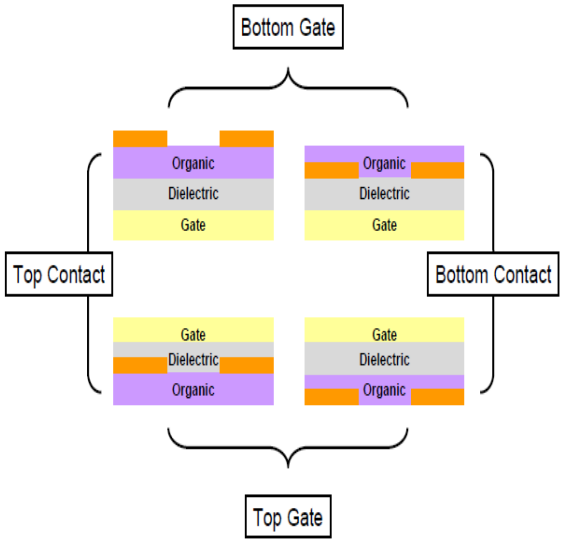


Fig.2. Four fundamental OTFT structures with different electrode and gate configuration.

A.Single Gate Structures

Top Gate OTFTs have the active layer deposited on the substrate and thereafter depositing the insulator and gate contact on top.Bottom Gate OTFTs have the gate contact and Insulator deposited first on the substrate and then the active layer.Variations are to deposit source and drain contacts on top of the insulator or on active layer .This is called top contact and bottom contact.Due to increased injection area for the charge carriers,the Bottom Gate Top Contact structure shows a lower contact resistance.

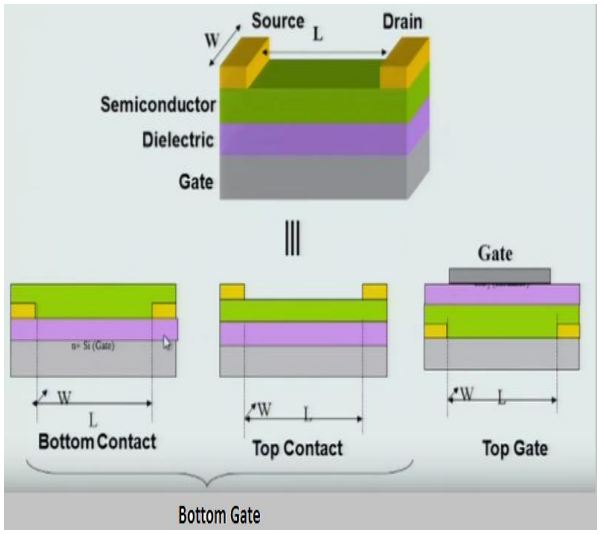


Fig .3.Single Gate Structures

B. Dual Gate Structure

Dual Gate Structures have a better control on threshold voltage, steeper sub-threshold slope (*SS*),higher on current,lower V_{TH} and higher Ids.

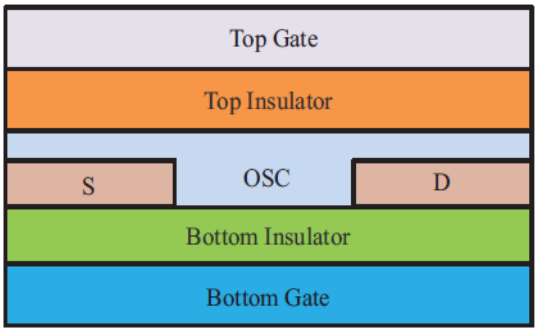


Fig.4.DG-OTFT

C.Vertical Channel Structure

It comprises of five different layers namely two semiconductor layers and three metallic layers of the source, drain, and gate as shown in Fig. 5.

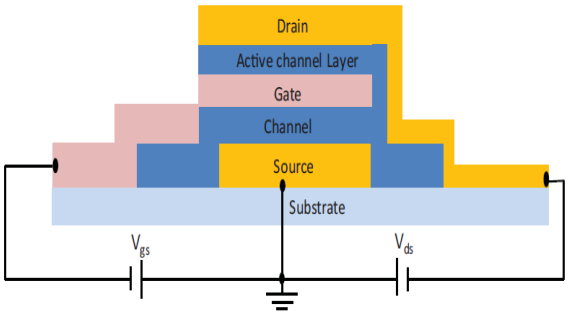


Fig.5.VC-OTFT

D.Cylindrical Gate Structure

Cylindrical gate (CG) OTFTs are used for size reduction and has good bending stability,thereby providing higher packing density.

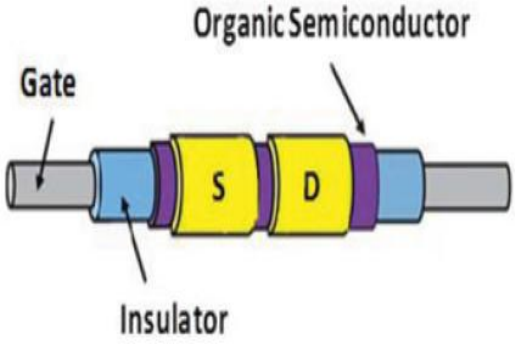


Fig.6.CG-OTFT

IV. LITERATURE SUMMARY OF PARAMETERS OF ORGANIC TRANSISTORS

Reza Meshkin et.al.,[1] presented transconductance modeling in OFETs based on the transistor equations and described the transconductance in saturation region that is suitable for analog circuit design.

Shubham Negi et.al.,[4] performed analyses of the Dual Gate OTFT and observed that there is superior carrier injection that results in significant increase in drive current as the two channels are formed in them.It is observed from the plot that the dual gate mode is best.

Umar Faruk Shuib et.al.,[16] presented the analytical model of an organic transistor and simulated the transfer and output characteristics of the device for different channel length (*L*) using MATLAB .From the simulation, it was concluded that drain current of organic transistor was increased with decrease in channel length. The ratio of change in on current to the change in off current is constant despite of varied channel length and the channel length does not depend on sub-threshold characteristics.

Brijesh Kumar et.al. [19] studied advanced organic thin film transistors structures,their charge transport phenomena, molecular structures,performance parameters,and fabrication techniques. All the OTFT structures namely single gate, dual gate, vertical channel, and cylindrical gate are studied in terms of current on/off ratio,field effect mobility, and operating voltage .

Dipti Gupta, Monica Katiyar & Deepak Gupta [44] provided the methods for mobility estimation by considering the effects of gate voltage dependence of mobility and contact resistance in TC OTFT's. The ideal MOSFET equations are modified for contact resistance for the linear region.

Christopher R. Newman et.al,[45] discussed new n-channel organic semiconductor's development, and outlined their properties and the recent progress.

V.RESULTS AND DISCUSSION

An analytical modeling for drain current in linear & saturation regimes, cut-off frequency, transconductance, & on-off current is carried out in MATLAB.The effect of interface between the layers and device dimensions is thoroughly studied.

A.Drain Current Modeling in linear region

A common model for OTFT's gives I_{DS} in the linear regime as

$$I_{D,\,Lin} = \frac{W\mu C_I}{2L}\left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}{}^2\right]$$

TABLE I . SIMULATION PARAMETERS

Parameter	Notation	Value
Width of channel	W	200 μm
Mobility	μ	0.5 cm^2/V.s
Gate Insulator Capacitance	C_I	0.6 μF/cm^2
Length of channel	L	5 μm
Threshold Voltage	V_{TH}	1.3 V

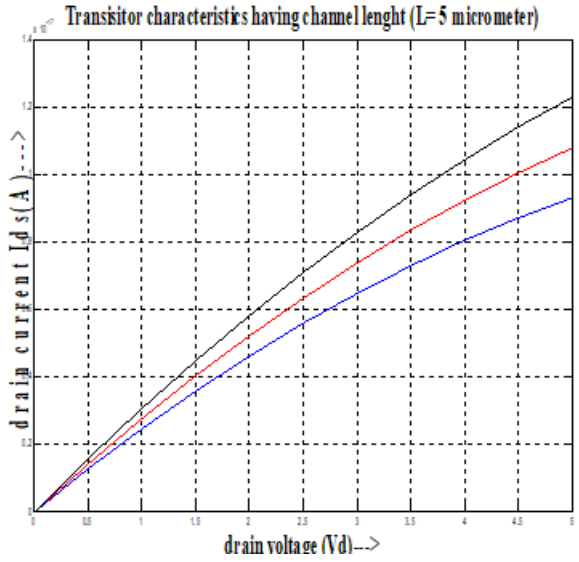
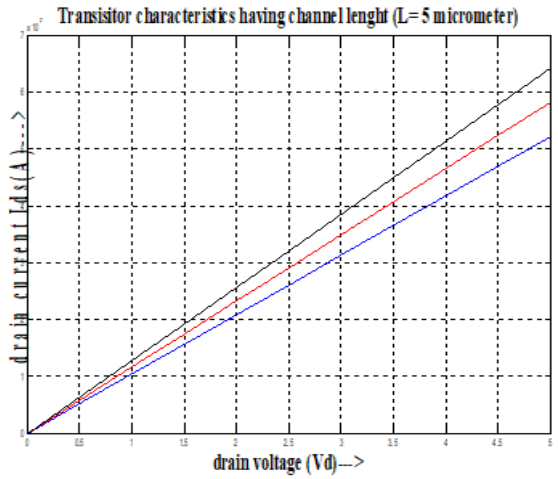


Fig. 7.Transistor Characteristics

B.Drain Current Modeling in linear region for small V_{DS}

$$I_{D,\,Lin(smallV_{DS})} = \frac{W\mu C_I}{L}\left[(V_{GS} - V_{TH})V_{DS}\right]$$



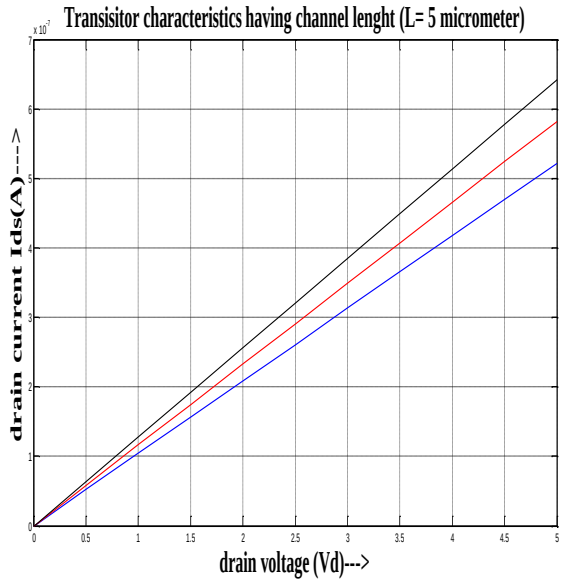


Fig. 8.Transistor Characteristics

C. Saturation Current Modeling

In the saturation region I_{DS} is given as

$$I_{D,\,Sat} = \frac{W\mu C_I}{2L}\left[(V_{GS} - V_{TH})\right]^2$$

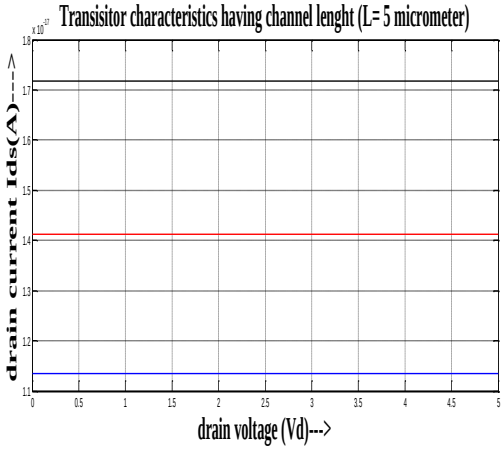


Fig. 9.Transistor Characteristics

D. Transconductance Modeling

The transconductance of transistor in saturation region is given by:-:

$$g_{m,\,sat} = \frac{W}{L} C_I \mu (V_{GS} - V_{TH})(1 + \lambda V_{DS})$$

TABLE II . SIMULATION PARAMETERS

Parameter	Notation	Value
Width of channel	W	200 µm
Length of channel	L	5 µm
Gate Insulator Capacitance	C_I	0.6 µF/cm^2
Mobility	µ	0.5 cm^2/V.s
Threshold Voltage	V_{TH}	1.3 V
Channel length modulation factor	λ	0.02 V^{-1}

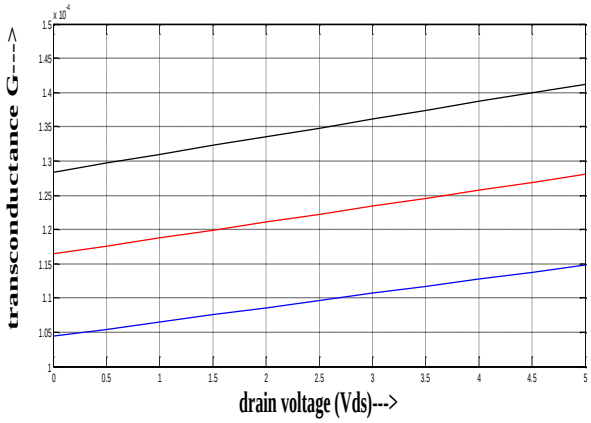


Fig. 10.Transistor Characteristics

E.Cut off Frequency Modeling

The cutoff frequency (f_{cutoff}) of OTFTs is given by:-

$$f_{cutoff} = \frac{\mu(V_{GS} - V_{TH})}{2\pi L(L + 2L_{ovlp})}$$

TABLE III . SIMULATION PARAMETERS

Parameter	Notation	Value
Mobility	μ	0.5 cm^2/V.s
Length of channel	L	5 μm
Overlap Length	Lovlp	10 μm
Threshold Voltage	V_{TH}	1.3 V

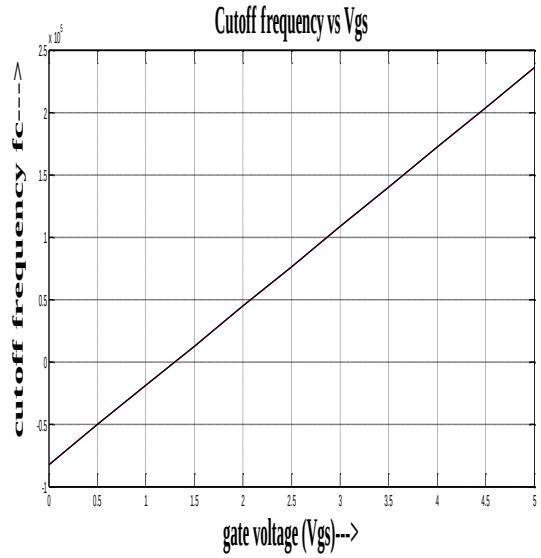


Fig. 11.Simulation of cutoff frequency with different Gate-source voltage

High f_{cutoff} of OTFTs can be achieved with short channel length and high gate voltage . This is shown in Fig.11 and Fig.12 respectively.

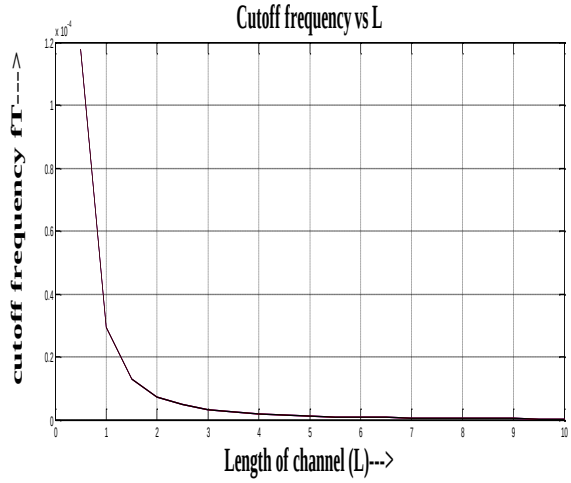


Fig. 12.Simulation of cutoff frequency with different channel length

Also, High f_{cutoff} of OTFTs can be achieved with short Ohmic contacts.and high mobility. f_{cutoff} will increase with the decrease of L_{ovlp}.

F.On -Off Current Modeling

$$\frac{I_{on}}{I_{off}} = \frac{C_I \mu (V_{GS} - V_{TH})^2}{t_{os} V_{DS} \sigma}$$

TABLE IV. SIMULATION PARAMETERS

Parameter	Notation	Value
Thickness of Semiconductor layer	tos	25 μm
Conductivity of channel	σ	0.212 *10^{-4}
Gate Insulator Capacitance	C_I	0.6 μF/cm^2
Mobility	μ	0.5 cm^2/V.s
Threshold Voltage	V_{TH}	1.3 V

The results of the simulation are shown in the figure given below.

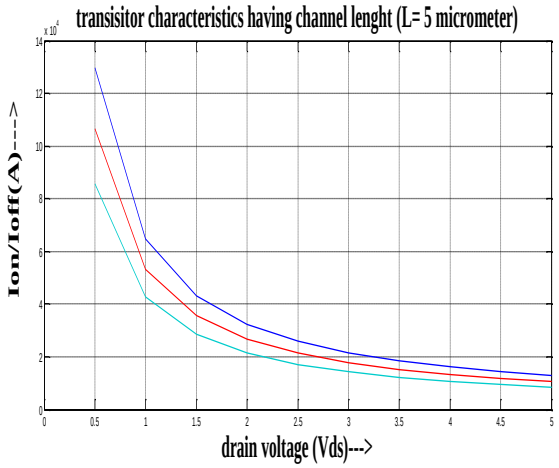


Fig. 13.Transistor Characteristics

From Fig.13 it is observed that with increase in drain voltage ,I_{on} / I_{off} decreases. It depends on the thicknesses and mobility of the semiconductor layers .

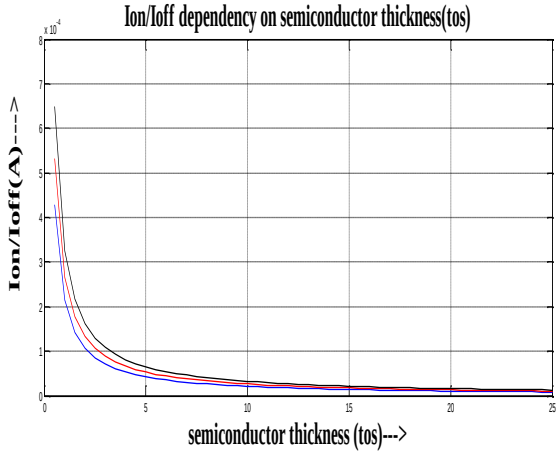


Fig. 14.Transistor Characteristics

It is observed that if the thickness of the semiconducting layers is lowered,I_{ON} increases and I_{OFF} decreases ,respectively, that increases the I_{ON}/I_{OFF} ratio.From Fig.14 it is observed that Ion / Ioff decreases when thickness of the semiconducting layers is increased and vice-versa.

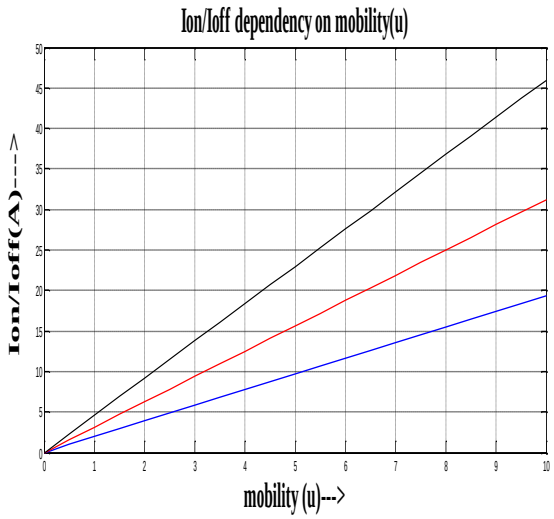


Fig. 15.Transistor Characteristics

I_{ON} increases and I_{OFF} decreases when the mobility is increased that increases the I_{ON}/I_{OFF} ratio.From Fig.15 it is observed that Ion / Ioff increases with increase in mobility linearily.

VI. CONCLUSIONS

Organic electronics are more flexible,lighter, and less expensive than their inorganic counterparts.They are also biodegradable since they are made from carbon.In this paper ,device performance of organic transistor through the simulation of MATLAB is carried out. It has been concluded that the high f_{cutoff} of OTFTs can be achieved with short channel length and high gate voltage and high current on-off ratio can be achieved by lowering the semiconducting layers' thickness and increasing the mobility.

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