

Harmonic Elimination of a PV Based Cascaded H-bridge Seven Level Inverter for Induction Motor Drive

Parul Gaur, Yajvender Pal Verma, Preeti Singh

Abstract: In today's era, reliable and good quality power is an essential requirement in industry, which can be supplied by inverters at medium and high power. Most of the appliances in the industry require high power or medium power for their operation. Power electronics devices such as inverters work on medium voltage and high power and are suitable for industrial applications and renewable particularly Photovoltaic (PV) integration. Multilevel inverters are more superior to conventional inverters because of lower harmonics and switching losses, but as the number of levels increases, complexity also increases. Therefore, maintaining the harmonics at lower level and lesser complexity of multilevel inverters is a challenge for researchers. In this research paper, a novel approach for implementation of seven level cascaded H- bridge configuration of multilevel inverter using direct current source and photovoltaic panels has been demonstrated. The basic working principle of seven level cascaded hybrid bridge inverter, pulse width modulation techniques and total harmonic distortion are explained through simulations in Matlab and Xilinx 14.3 software and the same is experimentally validated through FPGA controller based Spartan 6. The designed seven level inverter results in lower total harmonic distortion with lesser complexity when used to connect PV panels.

Keywords: Alternating Current, Cascaded H-bridge, Direct Current, Multilevel Inverter, Direct Current

I. INTRODUCTION

Advancement in technology has made power electronics an integral part of our daily life. Its applications can be seen in transportation, residential, industrial, telecommunication and aerospace sectors. Nowadays, many industrial applications require high power. In such industrial applications, power electronics converters such as multilevel inverters (MLIs) are highly recommended because of their prominent features such as reduced harmonics, minimum switching losses, electromagnetic compatibility and good power quality etc. at medium voltage and high power [1-2]. Electric power is the major form of energy source used in today's world. The objective of MLIs is to provide the improved power quality, effective control and efficient utilization of electric power.

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Nowadays, MLIs have been making major contributions in: 1) better control of electric equipment, 2) reduction of energy consumption leads to less pollution, 3) improving the efficiency by making reliable operation of semiconductor devices, 4) generating better sinusoidal output waveform with minimum harmonics and 5) enhancing the voltage profile.

MLIs have been introduced since 1975 as an alternative in high power applications [3]. Compared with conventional inverters, MLIs deal with more than two voltage levels. Voltage levels are combined in MLIs and the generated waveform results in better output waveform, minimum total harmonic distortion (THD), minimum switching losses and lesser electromagnetic interferences [4-5]. However, as the number of levels increases in MLIs, complexity also increases because of increased switching devices. maintaining the balance between the complexity and harmonics in MLIs is also a challenge. MLIs can be used in numerous applications such as high voltage direct current transmission, flexible alternating current transmission, static var compensation and harmonic suppression, energy storage systems and supplemental energy sources for e.g. wind, photovoltaic and fuel cells etc [6].

Neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) are the three different available topologies of MLIs [7]. The difference in all these topologies lies in the mechanism of switching and source of input to the MLIs. Compared with NPC and FC topology, CHB topology requires the minimum number of components and avoids the requirement of clamping diodes and capacitors as in NPC and FC topology respectively. The technical and economical factors suggest the use of CHB topology for industrial applications [8-9]. CHB topology has the potential for utility interface applications because of its capabilities for applying modulation and soft switching techniques [10-11].

The interfacing of MLIs having more number of levels and renewable energy sources is a major concern in today's world for grid and micro grids applications [12-14]. Utilization of renewable energy sources such as wind and solar energy is more advantageous in both environmentally and economically. In India, Ministry of New and Renewable Energy (MNRE) has proposed to speed up the solar power utilization to about 100 GW by 2022 [15]. More and more renewable energy sources deployment leads to benefits such as energy security, economic benefits as well as better environmental conditions [16-17]. Tremendous research work is going on photovoltaic (PV) generation systems for effective utilization of solar energy.

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In this research paper, multilevel inverter having seven levels with CHB topology is simulated and the same is validated through experimental study. Seven level CHB inverter is designed using DC source as input signal and then using PV cells rather than DC source as input signal. Seven level CHB inverter with PV cells takes more time to simulate (almost 22 minutes) than with DC source (4 minutes only). The generated MATLAB code of seven level CHB inverter with DC source is further converted into Xilinx code. Through Xilinx, coding is downloaded onto a FPGA Spartan 6 XC6SLX9 board and finally to the hardware of seven level CHB inverter. Maintaining the balance between the complexity and harmonics, the implemented multilevel inverter results in lesser complexity (as the number of levels is seven), lower harmonics as well as lower switching losses. The designed inverter can be used for generating staircase sinusoidal waveform from the DC input with lower THD.

II. MULTILEVEL INVERTER TOPOLOGIES

Nowadays, MLI configuration is mostly used in numerous industrial and grid interfaced renewable energy applications because of its numerous benefits such as minimum harmonic distortions, minimum switching and conduction losses, fault tolerance, modular structure and ease of control etc. Clamping diodes are used in NPC topology, while in FC topology capacitors are used.

CHB is an important configuration of MLIs because of its numerous advantages [18-20]. This configuration comprises the H-bridge series cells having individual direct current source for each cell. N level topology requires (N-1)/2 isolated DC sources per phase and 2(N-1) switches. For example, five level CHB inverter requires 8 switches and 2 H-bridge cells and power supplies. Each H-bridge cell produces three different voltage levels, for example, first bridge results in +Vdc, 0 and -Vdc voltages with unique combinations of switches S₁₁, S₁₂, S₁₃ and S₁₄. In this way, next bridges also results in the voltages. The alternation current (AC) of hybrid bridge cell is connected in parallel combination such that the obtained output waveform is combination of all individual hybrid bridge voltages. Figure 1 represent the CHB topology with seven level.

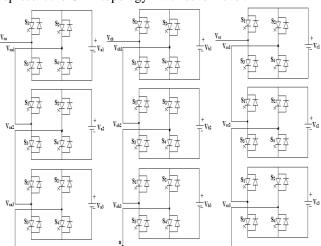


Figure 1. Seven Level CHB MLI

The output waveform generated by the MLI can be represented using Fourier series expansion, therefore the seven level CHB inverter's output voltage is represented as given below:

$$V_{ot} = \sum_{N=1}^{\infty} \frac{4Vdc}{N\pi} (\cos N\Delta_1 + \cos N\Delta_2 + \cos N\Delta_3) \sin(N\omega t)$$

(1)

Where V_{dc} is the input DC voltage, N defines the harmonic order at the output voltage of MLI, Δ_1 , Δ_2 , and Δ_3 are the three switching angles of seven level CHB inverter, which are needed to fire the switching devices of seven level inverter. Proper selection of these switching angles is necessary to reduce the harmonics of MLI's output voltage waveform. Generally, to keep the harmonics at lower levels, the switching angles Δ_1 , Δ_2 , and Δ_3 can be calculated using selective harmonic elimination equations as shown below:

$$\cos \Delta_1 + \cos \Delta_2 + \cos \Delta_3 = 3m$$

$$\cos 5\Delta_1 + \cos 5\Delta_2 + \cos 5\Delta_3 = 0$$

$$\cos 7\Delta_1 + \cos 7\Delta_2 + \cos 7\Delta_3 = 0$$
(2)

In above equation, m is the modulation index. Three firing angles of seven level CHB inverter must satisfy the constraint:

$$0 < \Delta_1 < \Delta_2 < \Delta_3 < \frac{\pi}{2} \tag{3}$$

III. PHOTOVOLTAIC SYSTEMS AND SWITCHING STRATEGIES OF MULTILEVEL INVERTER

Nowadays, use of renewable energy sources such as PV systems in MLIs is getting more attention. In PV systems, sun's radiation is converted into usable electricity. A PV system consists of the power inverter, solar panel and battery etc. PV cell is the main component of a PV system [21]. Figure 2 and 3 represent the equivalent circuit of a PV panel and a general PV system respectively.

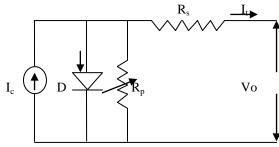


Figure 2. Equivalent Circuit of Photovoltaic Cell





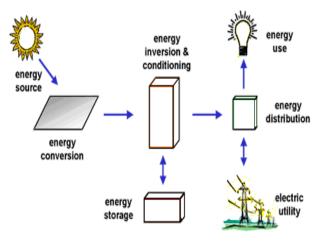


Figure 3. General Photovoltaic System

Another important aspect of multilevel inverters is the numerous modulation strategies used for firing purposes [22-24]. Aim of using these control modulation strategies is to obtain sinusoidal waveform with levels having lesser number of harmonics, lesser conduction and switching losses. Modulation strategies for MLI can be categorized in three groups such as low switching frequency, medium switching frequency and high switching frequency as represented in Figure 4. Lower value of switching frequency is required for applications with high power so as to keep the switching losses below the nominal values. Several control strategies have been reported in the literature such as space vector modulation (SVM), selective harmonic control (SHC), selective harmonic elimination (SHE) and selective harmonic mitigation (SHM) etc [25-27]. In SHE technique, Nth switching angles i.e. $\Delta_1, \Delta_2, \dots, \Delta_N$ are such selected so that the obtained output voltage waveform is with minimum harmonic distortions. In this research paper, SHE pulse width modulation technique is used for controlling of cascaded seven level inverter. SHE method works on fundamental switching frequency, which further produces output voltage waveform with minimum losses.

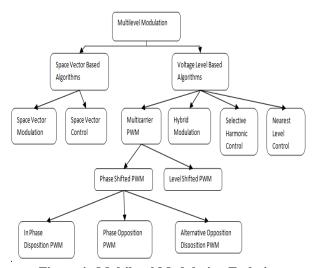


Figure 4. Multilevel Modulation Techniques

IV. SIMULATIONS AND EXPERIMENTAL RESULTS

MLIs are required for producing sinusoidal output voltage waveform with lesser harmonics. In this research work, two cases have been considered. First case, involves the simulation of seven level CHB inverter with DC source as input and the second case represents the simulation of same inverter with PV panels as input. Table 1 represents the switching pattern of the designed seven level CHB inverter.

Table 1: Defined Switching States for Seven Level CHB

MLI									
Output	Switching	S31	S12	S32	VH1	VH2			
Voltage	States								
(Vo)	S11								
3E	1	0	1	0	Е	2E			
E	1	1	1	0	0	2E			
	0	0	1	0	0	2E			
Е	1	0	1	1	Е	0			
	1	0	0	0	Е	0			
	0	1	1	0	-E	2E			
0	0	0	0	0	0	0			
	0	0	1	1	0	0			
	1	1	0	0	0	0			
	1	1	1	1	0	0			
-E	1	0	0	1	Е	-2E			
	0	1	1	1	-E	0			
	0	1	0	0	-E	0			
-2E	1	1	0	1	0	-2E			
	0	0	0	1	0	-2E			
-3E	0	1	0	1	-E	-2E			

Complete simulink model with subsystems like h-bridge and control strategy is represented in Figure 5. H-bridge block used is for seven level CHB inverter, having three h-bridges per phase, say H₁, H₂ and H₃. Each H bridge consists of four IGBTs, making total 12 switches per phase. Therefore, total 36 IGBTs switches are there in the seven level CHB inverter. Three h-bridges of each phase are connected with DC source as shown in Figure 6, while in another case these h-bridges are connected to PV panel rather than DC source as represented in Figure 7. In both cases, the designed seven level CHB inverter is same, only difference is in the input source i.e. first one is using DC source and second is using PV panel. Both cases, staircase seven level output is obtained but with PV panels, THD is low as compare to TDH with DC source. Simulation time is more in the second case (taking 20 minutes to execute) because of the complex block and subsystem of PV cells while in first case direct DC source is taken so it takes only five minutes to execute. Next step is to provide firing to the IGBTs switches of h-bridge. Firing should be provided in such a way so that first h-bridge (four IGBTs switches) is fired first, then after phase shift of 120°, next h-bridge is fired and after 240°, last h-bridge is fired so that for complete cycle, stepped sinusoidal waveform is obtained. This is done using PWM control strategy. IGBTs switches are then fired and ultimately THD is obtained, which is very low.



Therefore, the adopted technique in this research work is useful for obtaining staircase sinusoidal output in the multilevel inverter (seven level in this case, can be applied to the higher levels of inverters). Also, the designed inverter can be further used in another applications such as reactive power compensation (in static synchronous compensators) etc., which is very important and useful for large scale industries.

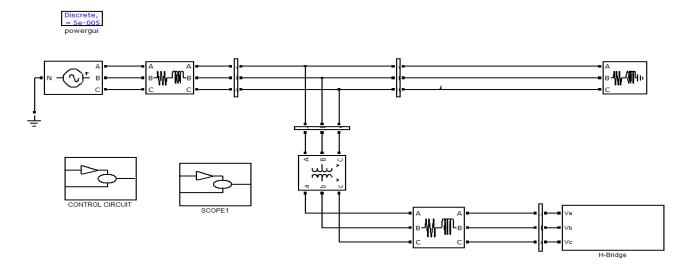


Figure 5. Simulink Model for 3 Phase Seven Level CHB Inverter

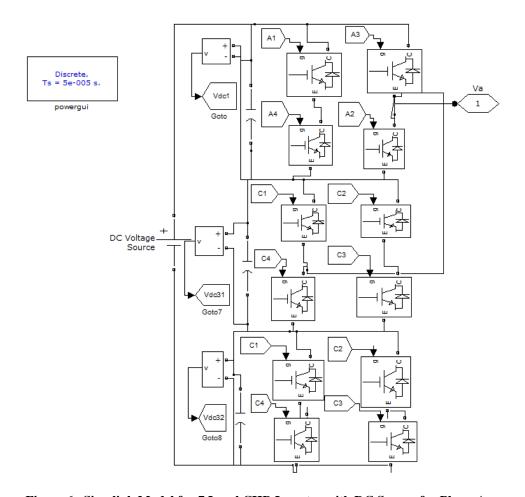


Figure 6. Simulink Model for 7 Level CHB Inverter with DC Source for Phase A





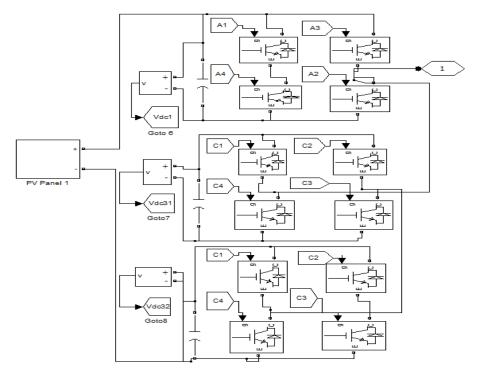


Figure 7. Simulink Model for 7 Level CHB Inverter with PV Source for Phase A

Proper choice of control strategy for firing of switching devices in MLIs is an essential step. Here, PWM strategy is used for firing the IGBTs switches of h-bridges of seven level CHB inverter. Figure 8 represents the simulink model of adopted PWM control strategy. Here, the output of phase locked loop (PLL) goes to a transformation block, which is used to perform a Park transformation.. PI controller is being used in the simulink model with proportional gain 6.5 and integral gain 0.045. Output of PI controller and PLL block goes to reference frame transformation and finally goes to demux (having three outputs). These three outputs are being used for firing of three h- bridges. Repeating sequence is used for generating triangular wave. This triangular wave is compared with the output of demux using relational operator greater than or equal to, which further leads to the generation of firing pulse, going to the one of the IGBT switches of h-bridge. Another IGBT switch of h-bridge is off due to complementary action, so logical operator NOT is being used for generation of firing pulse for this switch. In the same fashion, remaining firing pulses are obtained for the IGBTs switches of h-bridge.

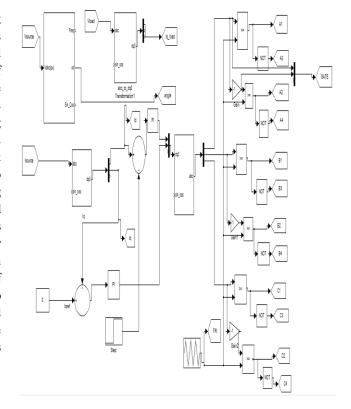


Figure 8. Simulink Model for PWM Switching Strategy of 7 Level CHB Inverter

Simulation results for the designed seven level hybrid bridge inverter are represented

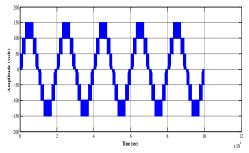
in Figure 9. Figure 9 represents the staircase output voltage levels obtained from the designed seven level CHB inverter after simulation in MATLAB and Xilinx software. In the proposed seven level CHB inverter, THD is low with lesser simulation time for DC sources as represented in Figure 10,



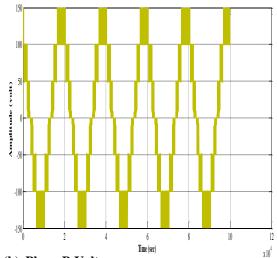
while calculated THD for CHB seven level inverter with PV source is shown in Figure 11. Table 2 and Figure 12 represents the THD (%) obtained from the two cases: first with DC source and second with PV source simulations of CHB seven level inverter. Therefore, from the simulation results, it can be concluded that with the aid of proposed seven level CHB inverter, staircase output waveform with minimum distortions (0.28%) are obtained

Table 2: THD in CHB Seven Level Inverter with DC source and with PV Source

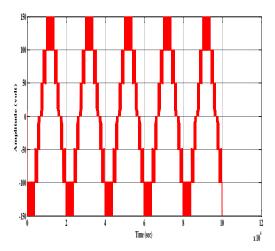
Modulation Index (Ma)	THD in CHB Seven Level Inverte r with DC Source (%)	THD in CHB Seven Level Inverter with PV Source (%)
0.7	0.28	10.27
0.75	0.27	10.25
0.8	0.27	10.24
0.85	0.25	10.24
0.9	0.25	10.23
0.95	0.26	10.24
1	0.25	10.22



(a) Phase A Voltage Levels of Seven Level CHB Inverter



(b) Phase B Voltage
Levels of Seven Level CHB Inverter



(c) Phase C Voltage Levels of Seven Level CHB Inverter

Figure 9. Simulated Voltage Levels in the CHB Inverter

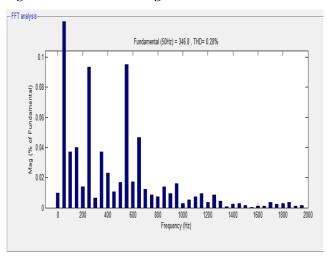


Figure 10. FFT Analysis of designed 7 Level CHB Inverter with DC source

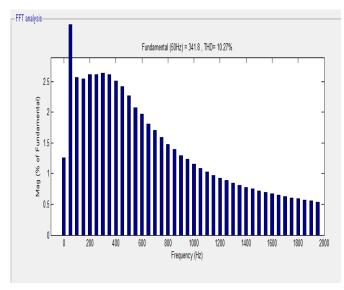


Figure 11. FFT Analysis of designed 7 Level CHB Inverter with PV source



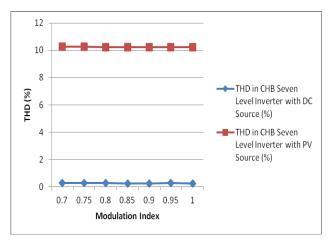


Figure 12. THD (%) in CHB Seven Level Inverter

Experimental results with a seven level CHB inverter were performed to validate the simulations. The traditional PWM and the proposed PWM technique for designed seven level CHB inverter were implemented using a FPGA controller based Spartan 6. In the FPGA controller based Spartan 6 board, the designed seven level CHB inverter coding is burnt, which provides the signals to CHB seven level inverter and finally the waveforms are observed on digital storage oscilloscope (DSO) as represented in Figure 13 and 14.



Figure 13. Generated Seven Level Voltage and Current Waveforms of CHB Inverter

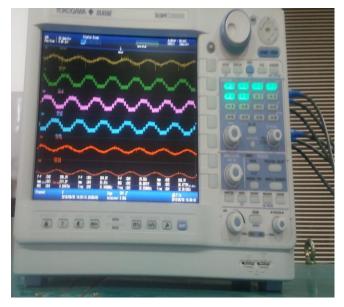


Figure 14. Voltage and Current Waveforms of Seven Level CHB Inverter on DSO

The designed system dramatically decreases the THD of the output waveform of cascaded H-bridge seven level inverter with induction motor drive. The speed of induction motor is also controlled as represented in table 3, where the input voltage through transformer is varied in steps, corresponding readings of DC link voltage, line voltage and speed of induction motor are shown.

Table 3 Voltages of CHB 7 Level Inverter with Induction Motor Drive

Input Voltage through transformer (Vin in volt)	DC Link Voltage (Vdc in volt)	Line Voltage (Vl in volt)	Induction Motor Speed (rpm)
20	7.51	13.92	4.91
30	13.62	25.82	510
40	15.96	30.05	1394
50	21.91	37.37	1404
60	26.93	46.54	1402
70	32.14	55.78	1396
80	38.61	67.34	1398
90	44.92	79.28	1400

V. CONCLUSION

Among the existing MLIs topologies, CHB topology is the most promising alternative for the PV applications. Same number of output voltage levels can be achieved using CHB topology with fewer switches as compared to other topologies. The control complexity associated with CHB configuration is directly proportional to the number of H-bridges used. In this research work, three H-bridges per phase are used, therefore,



the complexity associated with the seven level CHB inverter is less. In terms of switching losses and THD, seven level CHB inverter provides satisfactory results. Also the use of PV cells rather the DC sources are more economical and environmental friendly. Seven level CHB inverter with DC source and PV panel is implemented in MATLAB and Xilinx software and finally the simulation has been validated experimentally. The designed set up provides sinusoidal output waveforms with fewer harmonics for a seven level CHB inverter. Thus it can be concluded that CHB configuration can be used for integration of PV as it is efficient, economical and fast. However, while integration of PV through MLI, harmonic contents have been found to be more so to regulate voltage of PV buck-Boost converter can be tested.

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REFERENCES

- J. Rodriguez, J.Holtz, H. A. Rub, and G. Baoming, "Medium voltage multilevel converters-state of the art, challenges and requirements in the industrial applications," IEEE Transactions on Industrial Electronics, vol. 57, no. 8. pp. 2581-2596, 2010.
- 2. S. Bernet, "Recent developments of high power converters for industry and traction applications," IEEE Transactions on
- 3. Power Electronics, vol. 15, no. 6. pp. 1102-1117, 2010.
- J. Rodriguez, J.S. Lai, and F.Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724–738, 2002.
- J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage source converter topologies for industrial
- medium voltage drives," IEEE Transactions on Industrial Electronics, vol. 54, no. 6. pp. 2930-2945, 2007.
- S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of neutral point clamped, flying capacitors, and
- 8. series connected H-bridge multilevel converters," IEEE Transactions on Industrial Electronics, vol. 43, no. 4. pp. 1032-1040, 2007.
- H. Iman-Eini and S. B. Tennakoon, "Investigation of a cascaded H-bridge photovoltaic inverter under non-uniform isolation conditions by hardware in the loop test", International Journal of Electrical Power and Energy Systems, vol. 105, pp. 330-340, 2019.
- I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," Energy Conversion, Elsevier, vol. 52, no. 2, pp. 1114-1128, 2011.
- M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Perez, "A survey on cascaded multilevel inverters," IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2197-2206, 2010.
- K. Corzine, and Y. Familiant, "A new cascaded multilevel H-bridge drive," IEEE Transactions on Power Electronics, vol. 17, no. 1, pp 125-131, 2002.
- E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," IEEE Transactions on Industrial Electronics, vol. 62, no. 2, pp. 922-929, 2015.
- M.F. Kangarlu, and E. Babaei, "A generalized cascaded multilevel inverter using series connection of sub multilevel inverters," IEEE Transactions on Power Electronics, vol. 28, no. 2, pp. 625-636, 2013.
- M. B. Kalashania and D. Nazarpour, "New symmetric and hybrid multilevel inverter topology employed in solar energy systems," Transactions on electrical and electronic material, pp. 1-7, March 2018.
- 16. Peeyush Kala and Sudha Arora, "A comprehensive study of classical and hybrid multilevel inverter topologies for renewable energy

- applications," Renewable and Sustainable Energy Reviews, vol. 76, pp. 905–931, 2017
- M. Miranbeigi and H. Iman-Eini, "Hybrid modulation technique for grid-connected cascaded photovoltaic systems," IEEE Transactions on Industrial Electronics, vol. 63, no. 12, 2016.
- 18. https://economictimes.indiatimes.com/industry/energy/power
- N. Prabaharan and K. Palanisamy, "Analysis and integration of multilevel inverter configuration with boost converters in a photovoltaic system", Energy Conversion and Management, vol. 128, pp. 327–342, 2016.
- L. Liu, H. Li, Xue, and W. Liu, "Decoupled active and reactive power control for large scale grid-connected photovoltaic systems using cascaded modular multilevel Converters," IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 176–187, 2015.
- M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Perez, "A survey on cascaded multilevel inverters," IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2197–2206, 2010.
- A. Mokhberdoran, and A. Ajami, "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," IEEE Transactions on Power Electronics, vol. 29, no. 12, pp. 6712-6724, 2014.
- E. Babaei, S. Laali, and S. Alilu, "Cascaded multilevel inverter with series connection of novel H-bridge basic units," IEEE Transactions on Industrial Electronics, vol. 61, no. 12, pp. 6664–6671, 2014.
- S. J. Chiang, K. T. Chang, and C. Y. Yen, "Residential photovoltaic energy storage system," IEEE Transactions on Industrial Electronics, vol. 45, no. 3, pp. 385–394, 1998.
- P. Gaur and P. Singh, "Various control strategies for medium voltage high power multilevel converters: A Review", Proceedings of RAECS, UIET, Panjab University, Chandigarh, 2014.
- M.S.A. Dahidah and V.G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula," IEEE Transactions on Power Electronics, vol. 23, no. 4, pp. 1620-1630, 2008.
- A. K. Rathore, J. Holtz, and T. Boller, "Optimal Synchronous PWM for low switching frequency control of medium voltage multilevel inverters," IEEE Transactions on Industrial Electronics, vol. 57, no. 7. pp. 2374-2381, 2010.
- J. Zhao, Xiangning He, and R. Zhao, "A novel PWM control method for hybrid clamped multilevel inverters," IEEE Transactions on Industrial Electronics, vol. 57, no. 7. pp. 2365-2373, 2010.
- N. Susheela and P. S. Kumar, "Performance evaluation of carrier based PWM techniques for hybrid multilevel inverters with reduced number of components", Energy Procedia, vol. 117, pp. 635–642, 2017.
- M. Ye, L. Kang, Y. Xiao, P. Song and S. Li, "Modified hybrid modulation strategy with power balance control for H-bridge hybrid cascaded seven level inverter", IET Power Electronics, vol. 11, no. 6, May 2018.

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