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Abstract: This paper presents the simulation and measured results of a Low Noise Amplifier (LNA) working at 28 GHz for the 5G wireless system. LNA is used to amplify the weak receiving signals in the RF receiver system. The 28 GHz (Ka-band) LNA is designed to work for 5G technology wireless system. Here a Fujitsu FHR02X transistor is used in the simulation process, where the one-stage LNA is adopting a common-source with source inductive degenerative topology. In the fabrication process, GaAs pHEMT MMIC HMC519LC4 LNA is mounted on the Rogers 4003C board ($\varepsilon_r = 3.38$ and $\delta = 0.0027$) and tested using (PNA-X N5246A) Microwave Network Analyzer. The final LNA design in the simulation process achieves a power gain of 9.185 dB, input and output return losses of -13.124 dB and -15.455 dB respectively, and noise figure of 9.185 dB. Furthermore, the fabricated LNA achieves a power gain of 10.91 dB, input and output return losses of - 7.75 dB and - 22.13 dB respectively. Although the return loss (S_{11}) value is higher than -10 dB, but the LNA still able to obtain gain more than 10 dB. Thesimulation and fabricated LNA have input return loss quite closed to the given value in the datasheet. Thus, the LNA transmission line has a good output matching design.

Keywords:Low Noise Amplifier, 5G, Wireless Systems, mm-Wave, MMIC, pHEMT, Semiconductor device.

I. INTRODUCTION

Weare in the era of rapid growth in communication technology. Starting with the first generation cellular system (1G) introduced in 1970s, we are now the users of the fourth generation wireless system (4G) or also known as Long Term Evolution (LTE).

Revised Manuscript Received on January 30, 2020.

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The massive growth of smartphone users and other data consuming devices results in higher data rates demand. Due to these factors, the cellular band below 6 GHz is becoming congested [1], [2]. To overcome this problem, researchers are now working towards the new technology, called the fifth generation (5G) wireless system. Researchers are interested in deploying a new spectrum, which is millimeter-wave frequency spectrum for 5G technology [3].Ka-Band, specifically 28 GHz frequency is a popular choice among researchers to be used in 5G technology[4]. In order to manifest the idea behind 5G, researchers are focusing on front-end transceiver of the system. The transceiver is the combination of receiver and transmitter circuits. The components in transceiver should be able to suit 5G requirements. Low noise amplifier (LNA) is an electronic amplifier found at the front-end of a receiver circuit. It is used to amplify weak input signals and helpsto reduce theunwanted noise. The amplified signal is the combination of the wanted and unwanted signals. The unwanted signal which is noise cannot be eliminated from the circuit, but it can be reduced. To dothat, the LNA should have high gain to diminish the noise from the circuit. There are many types of transistors available in the market such as pHEMTs, FETs and BJTs. Every type of transistor has its own capability, advantages, and disadvantages. Recently, GaAs-based pHEMT transistors are gaining their popularity in LNA design. This is because they provide high electron mobility due to high electron confinement density in the potential well. In addition, pHEMT can improve signal-to-noise ratio especially at higher frequencies. In this project, an LNA is designed by using GaAs-based transistor working at 28 GHz frequency. The design process is done in Agilent's Advanced Design System (ADS). The simulation process uses Fujitsu's FHR02X, a GaAs-based HEMT transistor which has power gain of 9.185 dB, noise figure (NF) of 3.840 dB, input return loss, S_{11} of -13.124 dB and output return loss, S_{22} of -15.455 dB. In fabrication process, an off-the-shelf GaAs pHEMT MMIC HMC519LC4 is used. The LNA shows good performance in term of power gain as it able to produce power gain up to 10.91 dB. The input return loss $S_{11 is}$ -7.75 dB while the output return loss S_{22} is -22.13 dB.

II. RELATED WORK

There are many topologies suggested by researchers in LNA designs. Fig.1 shows a CS with resistive termination topology. In this topology, a resistor $R_{\rm l}$ is placed in parallel with the input to provide 50Ω input impedance.



The termination resistor however produces thermal noise as much as R_s does. Hence, the noise figure of this topology is very high. Since its performance in terms of noise is very poor, this circuit design is not suitable for low noise applications.

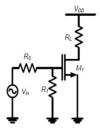


Fig. 1.Common-source with resistive termination [5]

In Fig. 2, a shunt resistive feedback is applied to a CS amplifier to achieve 50Ω input impedance. This topology is very convincing for broadband application with minimum impact on the noise performance[6]. Nevertheless, it has several drawbacks. The input impedance, Zin relies on the feedback resistor, R_{fb} and voltage gain, A_v, consequently it becomes very sensitive to any variation process. Besides, the noise figure might increase to undesirable level due to significant noise from the feedback signal.

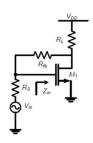


Fig. 2.Common-source with shunt feedback [5]

Fig. 3 shows a cascode topology. Designers usually used cascode topology in their designs. This is because cascode topology is very attractive in term of its gain. This topology able to achieve higher gain with lower noise figure [7], [8]. Besides, it has higher reverse isolation and lower power consumption. However, if the designer wants to have superior performance in term of gain, the noise performance will be suffered and vice versa. This is the common trade-off effect between gain and noise figure in LNA design [7].

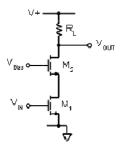


Fig. 3.Common-source with shunt feedback [5]

Transistor selection plays an important role in LNA design. Each type of transistor has its own capability and specialty. Si-based transistor is losing its popularity nowadays because its performance is far behind GaAs-based transistor. Si-based transistors are being used in LNA design for 28 GHz application [8]. Yet, the performance is far behind the LNA using GaAs-based pHEMT. This is because the electron mobility in GaAs-based transistor is 50, higher than in Si. Stability plays an important role in designing an LNA. It is necessary to check the stability of the transistor to prevent oscillation occurs at frequencies of interest [9], [10]. Asto ensure the transistor used is unconditionally stable, it needs to fulfill these two conditions; K > 1 and $|\Delta| < 1$. Equations (1) and (2) show how to calculate Rollet's stability factor, K and delta factor, $|\Delta|$ respectively [9] by using S parameters.

$$K = \frac{(1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2)}{2|S_{12}\times S_{21}|} > 1$$

$$|\Delta| = |S_{11} \times S_{22} - S_{12} \times S_{21}| < 1$$
(2)

$$|\Delta| = |S_{11} \times S_{22} - S_{12} \times S_{21}| < 1 \tag{2}$$

Power gain, noise figure, input and output return losses are important parameters used to determine the performance of the LNAs. Gain can be defined as the ability of the device to amplify the power of the receiving signal. It shows the ratio of the output to the input signal of the device. Usually, it is expressed in terms of decibels. The gain can be translated in terms of voltage gain or power gain as shown in Equations (3) and (4) respectively [9].

Voltage gain,
$$A_V = 20 \log \frac{V_{out}}{V_{in}}$$
 (3)
Power gain = $10 \log \frac{P_{out}}{P_{in}}$ (4)

Power gain =
$$10 \log \frac{P_{out}}{P_{out}}$$
 (4)

Apart from gain, noise also has a significant role when designing an LNA. In receiver application [1], [11], the noise should be as low as possible. The first stage of a receiver front-end provides the dominant noise performance of the entire system. Usually, noise is expressed in decibels. It is called as noise figure, NF. Equation (5) shows how to express noise in decibels [9].

$$NF = 10 \log F \tag{5}$$

 S_{11} is a ratio of reflected to incident waves on port 1 when port 2 is terminated by Zo. The waves can be reflected and incident voltages or reflected and incident powers. It is usually measured in decibel (dB). Equations (6) and (7) are used to calculate S₁₁ in terms of dB by using voltages and powers respectively [9]. In ideal case, there should be no signal reflected to the input port. It means that, the load fully utilizes the injected signal. However, in the LNA design, designers always considered that about 10% of the injected signal is reflected to the input port, leaving 90% of the power to be utilized by the load. A good LNA design should have

$$S_{11}(dB) = 20 \log \frac{b_1}{a_1}$$

$$S_{11}(dB) = 10 \log \frac{b_1}{a_1}$$
(6)

$$S_{11}(dB) = 10 \log \frac{b_1}{a_1} \tag{7}$$

 S_{22} is a ratio of reflected to incident waves on port 2 when port 1 is terminated by Zo. It usually measured in decibel (dB). Equations (8) and (9) are used to calculate S_{22} in terms of dB by using voltages and powers respectively [9]. A good LNA design should have S_{22} <-10 dB as well.

$$S_{22}(dB) = 20 \log \frac{b_2}{a_2}$$
 (8)

$$S_{22}(dB) = 100 \log \frac{b_2}{a_2}$$
 (9)





There are various types of transistors commercially available in the market. Recently, GaAs-based pHEMT transistors are gaining their popularity in LNA design [12]. This is because they provide high electron mobility due to high electron confinement density in the potential well. In addition, pHEMT can improve signal-to-noise ratio especially at higher frequencies. Other researchers tried to use GaAs-based FET in their LNA design for high frequencies application. Even though it provides low noise figure, however the LNA suffers in terms of gain [13]. It is essential for the LNA to have low noise figure, NF and highpower gain at the same time. In short, to realize the idea behind 5G wireless system, the LNA needs to undergo evolution to meet the specifications of this technology. A new frequency spectrum needs to be exploited since the frequency band below 6 GHz is overcrowded nowadays. Ka-band is the best candidate to be used in 5G technology. Even though there are many commercially available LNAs for Ka-band applications in the market, however, they are not suitable for wireless communication system. Hence, it is necessary to design a new LNA to be implemented in the 5G wireless system. There are many topologies can be used in the LNA designs. A common-source stage with source inductive degeneration is perfect to be adopted in the input matching because it has high gain and low noise figure. Although cascade topology is very attractive due to its high gain performance, it could not be used in this project because of the budget limitation.

III. METHODOLOGY

Firstly, the specifications of this project are set as shown in Table 1. This project is done to design an LNA working at 28 GHz forthe 5G wireless system. 28 GHz (Ka-band) is chosen in this project because many researchers proposed this frequency to be used for 5G technology. The gain and noise figure is expected to be more than 10 dB and less than 5 dB respectively. The gain is relatively high since the proposed design is for a single stage LNA.

Table 1. Specifications of the project

Performance Parameter	Specification	
Frequency	28 GHz	
Power Gain, S ₂₁	>10 dB	
Input Return Loss, S ₁₁	< -10 dB	
Output Return Loss, S ₂₂	< -10 dB	
Noise Figure	< 5 dB	

A. Checking the Stability of the Transistor

After choosing a transistor working at 28 GHz from ADS library, it needs to undergo a stability checking process to ensure that it is suitable to be used in this project. The

transistor needs to be unconditionally stable so that it does not oscillate at the frequency of interest. Fig. 4 shows how to check the stability of the transistor in ADS. In order for the transistor to be unconditionally stable, it needs to fulfill these requirements; K > 1 and mag delta $(|\Delta|) < 1$.

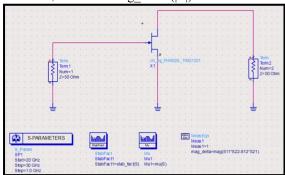


Fig. 4. Stability circuit

B. Design a Biasing Network

Next, the DC biasing point of the transistor is determined and the corresponding biasing network is designed. Fig. 5 shows the DC biasing set up in ADS.

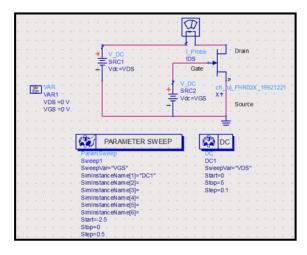


Fig. 5.DC biasing set up of the transistor

C. Input and Output Matching

After reviewing previous works on LNA, the best topology is adopted in this design. In this project, a common-source stage with source inductive degeneration topology[9]is adopted for input matching. Fig. 6 shows common-source with inductive degeneration topology. This topology is selectedasit shows a good performance in termsof noise figure and power gain.

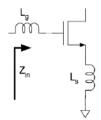


Fig. 6.Common-source with inductive degeneration topology[5]



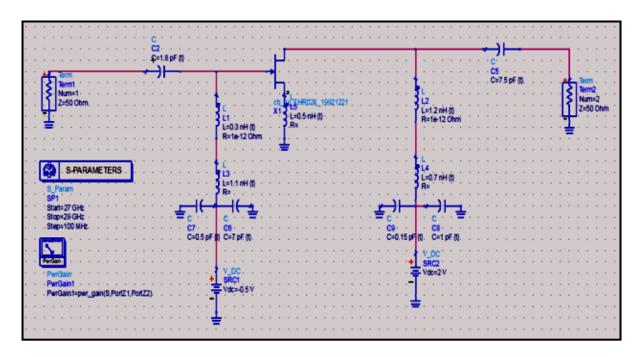


Fig. 7. Final LNA design

The matching is done to obtain 50 Ω impedance matchingfor both RF in and RF out. The circuit is tuning to get the best values of $S_{11},\ S_{22}$ and $S_{21}.$ Fig. 7 shows the complete matching network, with biasing network to bias the transistor of the LNA. The simulation results will be next section. The third phase of this project relates to layout design for fabrication process. In layout design, a GaAs pHEMT MMIC Low Noise Amplifier HMC519LC4 is used. The layout design starts with identifying all the pin details, including its dimensions. During the layout design process, the footprint of the chip is drawn based on the dimensions from the datasheet. The footprint size must be accurate and any error in the dimension should be avoided as we are handling the chip in millimeter size. This is necessary to ensure that the MMIC can be placed on the PCB perfectly. Next, two 50 Ω microstrip transmission lines are integrated into the footprint of the design at RF in and RF out pads. The width of the transmission lines is calculated by using LineCalc tool in ADS. From the LineCalc tool, the dimension of length, L and width, W of themicrostrip transmission line are 2.147510 mm and 3.964080 mm respectively. Next, the input and output return losses of the transmission lines are checked to ensure that both parameters meet the required specifications. Fig. 8 shows how to measure input and output return losses from the calculated transmission line.

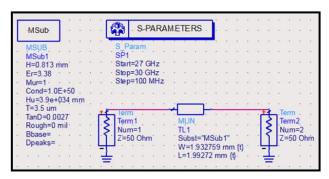


Fig. 8.Matching network of the transmission lines

The microstrip lines are connected to pin 3 and pin 16 by tapers to reduce the discontinuity effect that is associated with a step width junction. Pin 19, 21 and 23 are directly connected to the microstrip lines, but the end of each line is set to be wider to ease the wire soldering process. The unused pins are removed from the design to avoid any overlapping during the fabrication process. In addition, a good via structure below the ground pad is essential for a good RF and thermal performance. Hence, grids holes are with radius 0.3 mm are placed around the ground pad. Fig. 9 shows the final LNA layout design.

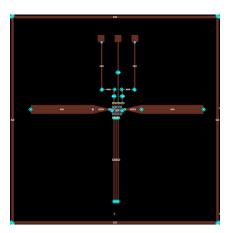


Fig. 9.Final LNA layout design

This final design is converted into a Gerber file and sent to PCB laboratory for fabrication process. Fig. 10 shows the fabricated LNA layout on the Rogers RO4003C board. After fabrication process, the MMIC and connectors are soldered to the board. The components should be properly soldered to ensure that the performance of the LNA is not affected. Then, the board is placed in an aluminium box to reduce losses during measurement.



Fig. 11 shows a complete fabricated LNA in the aluminium box.

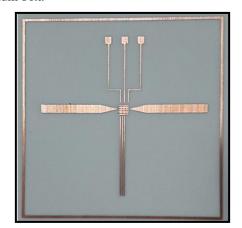


Fig. 10. Fabricated LNA on Rogers board

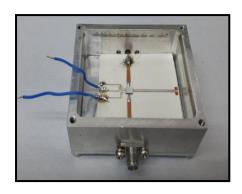


Fig. 11.A complete fabricated LNA

An analog signal generator and a signal analyser are used in determining the power gain of the LNA. Since this project is done at higher frequency which is 28 GHz, the cable loss should be considered. One end of the cable is directly connected to a signal generator and the other one is connected to signal analyser. After that, the RF in of the LNA is connected to the analog signal generator and the RF out is connected to the signal analyser. The power supplies are connected to pin 19, 21 and 23. Fig. 12 shows the LNA set up for the power gain measurement.

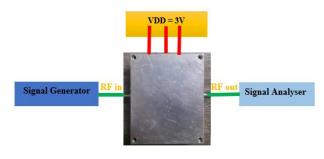


Fig. 12. LNA set up for power measurement

A network analyser is used to measure the input and output return losses. Before measurement is taken, it needs to be calibrated first. After calibration, the network analyser is ready to be used to measure the S-parameter performances of the testing LNA. The complete fabricated MMIC Low Noise Amplifier module is evaluated using the (PNA-X N5246A) Microwave Network Analyzer.

IV. RESULT AND DISCUSSION

A. Stability of the Transistor

Fig. 13 and 14 show the K and mag_delta ($|\Delta|$) values of the transistor. Since both values show K > 1 and ($|\Delta|$) <1, hence the device is unconditionally stable.



Fig. 13.K value of transistor at 28 GHz

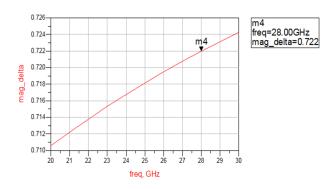


Fig. 14.($|\Delta|$) value of transistor at 28 GHz

B. Biasing Points of the Transistor

The biasing points are determined to ensure that the transistor is always working in the ohmic region. Fig. 15 shows the I-V curve of the working transistor.

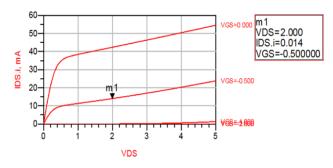


Fig. 15.I -V curve of the transistor

C. Input and Output matching

Fig. 16 shows the comparison between S_{11} values from simulation and hardware measurement. The S_{11} value of hardware measurement is slightly bigger than – 10 dB. This might happen due the external factors such as human errors and the properties of the Rogers Board itself. During soldering process, the K connectors may be improperly soldered to the board.



Even though Rogers Board is the best material to be used in high frequency, yet its electrical performance is moderate which contributes to higher losses.

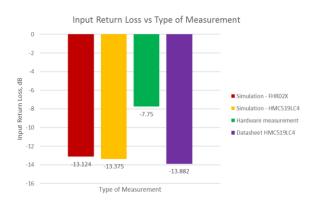


Fig. 16. LNA set up for power measurement

Fig. 17 shows the comparison between output return loss, S_{22} . All measurements able to meet the output return loss requirement in this project, $S_{22} < -10$ dB. The simulation and fabricated LNA have input return loss quite closed to the given value in datasheet. Thus, the LNA transmission line has a good output matching design.

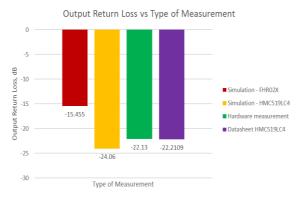


Fig. 17. Comparison between S_{22} values

D. Power Gain of the LNA

Fig. 18 shows the comparison between power gain in this project. The power gain is also known as S_{21} . The targeted power gain of this project was $S_{21} > 10$ dB. From Fig. 18, only simulation of FHR02X did not meet the targeted power gain. This is due to the capability of the transistor itself. The transistor is unable to produce gain more than 10 dB at 28 GHz. To do that, the design can be modified by adding number of stages. The power gain from hardware measurement is comparable with the value given in datasheet. It is slightly lower than datasheet value, but still within the specified limit.

E. Noise Figure

Noise figure, *NF* is one of the parameters needs to be specified to determine the performance of the LNA. The noise figure should be as low as possible in a good LNA design. Fig. 19illustrates the noise figure of the final LNA design of this project. In this design, the noise figure is 3.840 dB. By using common-source stage with source inductive degeneration topology in the design, thenoise figure shows an

attractive performance at 28 GHz frequency. This design achieves the targeted noise figure, which is less than 5 dB.

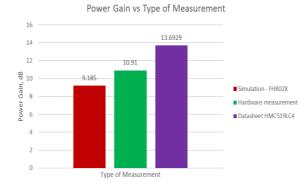


Fig. 18. Power gain comparison



Fig. 19. Noise Figure of the final LNA design

F. Comparison between This Work with Previous Work

The performances of the simulated and fabricated LNA from this project are compared with related work from other researchers (Table 2).

V. CONCLUSION

Throughout this project, an LNA working at 28 GHz for the 5G wireless system is designed and simulated. Two different transistors have been used in simulation and fabrication processes. A Fujitsu FHR02X transistor is used in the simulation process while a GaAs pHEMT MMIC HMC519LC4 LNA is used in the fabrication process. From simulation process, both S_{11} and S_{22} are -13.124 dB and-15.455 dB respectively. Even though the LNA uses FHR02X; show good performance in terms of input and output return losses, however it suffers in term of power gain. The LNA design unable to meet the insertion gain (S_{21}) specification which is >10 dB. The power gain can be improved by using cascade LNA design, but the transistor packaging itself is conservative to be used in recent technology. Recently, SMT transistor is preferable as it is smaller, does not need the drilling holes which increase cost and time and can be mounted on both sides of the PCB. The

layout for an off-the-shelf GaAs pHEMT MMIC HMC519LC4 LNA is successfully designed in this project. The width of the transmission lines need to be calculated first so that the transmission losses could be minimized. Despite the fact that the S_{11} value should be zero so that all the injected powers have been utilized by the load,





it is impossible to diminish all losses from the design. In the layout design, the LNA achieves the targeted power gain at the frequency of interest, 28 GHz. The power gain, S_{21} is -10.91 dB while the input return loss, S_{11} and output return loss, S_{22} are -7.75 dB and -22.13 dB respectively. Although the return loss (S_{11}) value ishigher than -10 dB, but the LNA still able to obtain gain more than 10 dB. The input power

loss might happen due to improper soldering of the K-connectors at the transmission lines. Hence, it is very important to ensure that the connectors are properly soldered to the board. Overall, the fabricated 28 GHz LNA meets a realistic agreement against the simulation and practically excellent to be served as a subsystem for 5G technology transceiver system.

Table 2. Comparison between LNAs performance

Performance Matrices	This work		M. Arsalan et.al	Kamil Pongot et.	Eren Curuk et.	Jeffery Curtis et.
	Simulation	Fabrication	(2014)	al (2016)	al (2016)	al (2016)
Frequency (GHz)	28		1.9 - 2.4	5.8	28	28
S11 (dB)	-13.124	-7.75	-16.089	-12.41	< -10	< -15
S22 (dB)	-15.455	-22.13	-14.174	-13.88	< -10	< -10
S21 (dB)	10.803	10.91	12.850	66.38	2.0 ± 0.5	18 ± 0.5
Noise Figure (dB)	3.840	-	0.588	0.60	0.95	3.0 ± 0.5
Topology	Common-Source with inductive degeneration	-	Cascode	Cascode with inductive drain feedback	Cascode	Common Source
Number of Stage	1	1	2	2	2	3
Type of Transistor	GaAs HEMT	GaAs pHEMT	GaAs pHEMT	GaAs pHEMT	HJ - FET	GaAs pHEMT
Application	5G	5G	4G LTE	WiMAX	VSAT System	5G

ACKNOWLEDGMENT

The authors would like to thank School of Electrical &Electronic Engineering, UniversitiSains Malaysia for the lab facilities. This research was funded under Research University Short Term Grant No. 304/PELECT/6315067 by UniversitiSains Malaysia.

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