

# High-Speed FIR Filter Design using Decision Tree Algorithm with FPGA Debugging

Murali Anumothu, Kakarla Harikishore



**Abstract:** In recent years, the filter is one of the key elements in signal processing applications to remove unwanted information. However, traditional FIR filters have been consumed more resources due to complex multiplier design. Mostly the complexity of the FIR filter is dominated by multiplier design. The conventional multipliers can be realized by Single Constant Multiplication (SCM) and Multiple Constant Multiplication (MCM) algorithms using shift and add/subtract operations. In this paper, a hybrid state decision tree algorithm is introduced to reduce hardware utilization (area) and increase speed in filter tap cells of FIR. The proposed scheme generates a decision tree to perform shift & addition and accumulation based on the combined SCM/MCM approach. The proposed FIR filter was implemented in Xilinx Field Programmable Gate Array (FPGA) platform by using Verilog language. The experimental results of the DTG-FIR filter were averagely reduced the 48.259% of LUTs, 51.567 % of flip flops and 44.497 % of slices at 183.122 MHz of operating frequency on the Virtex-5 than existing VP-FIR.

**Keywords:** FIR filter, Digital Signal Processing, Large Scale Integration, Power-area product, Multiple Constant Multiplication, Low power.

## I. INTRODUCTION

The filtering process is the essential operation in DSP applications such as audio processing, wired/wireless communication, image, and video processing architectures [1], [2]. Digital filters play a vital role in DSP applications due to their significant performance in filtering/de-noising in mobile phones, television, the Internet etc. In general, filters are used for signal separation and restoration from noisy sources transmitted through the channel. Signal extraction must require when the signal has been affected by interference, noise or other signals source exhibits with the original signal. This problem can occur on either analog signals or digital signals transmission. Analog filters are fast, cheap in production and process the signal that has interfered with noise in both frequency and amplitude whereas digital filters processes various kinds of signals with different frequency range and bandwidth.

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For analog filters, different kinds of parameter considerations must require to maintain the accuracy, operating range and stability of the resistors and capacitors. In contrast, digital filters are having better performance in maintaining accuracy, stability and restoration with compact hardware utilization. The constraints shift the properties of the degraded signals and the theoretical issues related to their properties [3]. For an efficient filter design, optimization should be done in architecture to improve filter performances by power consumption, area and delay which can be achieved by proper selection of multiplier and adder techniques [4]. The fixed coefficient FIR can be designed with either SCM or MCM schemes. The computational analysis showed that transposed structure and derived flow graph of the FIR filter has reduced register complexity. Though, the mathematical analysis is complex for the MCM scheme [5]. A 4-tap parallel FIR filter is designed using a top-down hierarchical approach with VHDL on a Virtex-5 FPGA platform. The design consumes a minimum area overhead in FPGA that leaving large device utilization for some other parallel processors on a similar device [6]. Optimization of a basic path for the Transposed Direct Form (TDF) structure-based FIR filter assessed by looking at the coefficient duplication and postponement of a tap [7]. The vast majority of the work on structure and usage of the FIR channel so far spotlight on the enhancement of MCM squares [8], [9]. But, the critical path needs more help from the product-accumulation section. So, control optimization of an MCM module does not affect the FIR filters' speed and error-resilient techniques for voltage scaling [10].

In this research, the analysis of speed and area has been taken to design an effective FIR filter structure. In this paper, a hybrid state decision tree algorithm was proposed to reduce hardware utilization (area) and increase speed in filter tap cells. The proposed scheme generates a decision tree to perform shift & addition and accumulation based on the combined SCM and MCM algorithm.

This proposed research work is composed as follows: analyzed some significant FIR filter designs in section-II. In section-III, presents briefly described of proposed filter design. Comparative experimental results of an existing and proposed FIR filter designs in section-IV. The conclusion of this research work is made in section-V.

## II. LITERATURE WORKS

Recently, the researchers have been suggested several ideas for FIR filter implementation. Among these, some significant FIR filter design is presented in this section.



P.C. Bhaskar et al. [11] proposed a FIR filter using Distributed Arithmetic (DA) in the Xilinx tool. The structure produces efficient signal noise ratio and means square error. The high heat dissipation and chip signal interference should be reduced to a greater level.

Z. Szadkowski and D. Glas [12] introduced adaptive linear predictor FIR filter on the cyclone V FPGA with HPS to minimize the narrowband RFI in radio detection of cosmic rays. Refreshment time for coefficient during adaption is very low. The adaptive low pass filter uses soft-core processors with adaptive filtering that requires more coefficient area for memory storage.

S. Ramanathan et al [13] proposed a low power adaptive FIR channel configuration dependent on the DA calculation. The Least Mean Square (LMS) algorithm was utilized to decrease the exchanging movement and power consumption. The DA utilized convey for FIR filter architecture, it has involved more zone in the FIR filter structure.

Mittal et al. [14] proposed a different multiplication approach based 16<sup>th</sup> order FIR filter. This method was optimized filter area, power and delay based on approach such as FIR filter coefficient with FIR filter input. To reduce the complexity of the filter, the coefficient was represented in Conical Signed Digit Representation (CSDR) which was more efficient compared to existing binary representation. The FIR filter with Han Carlson Adder (HCA) consumed a minimum area. But, it provides more delay between adders.

Atul Kumar et al. [15] proposed a low power FIR filter design, which is implemented based on Hybrid Artificial Bee Colony (HABC) to reduce switched power consumption. It provides faster convergence than a conventional ant bee colony. Ant Bee optimization provides low power filtering but consumes more LUTs and Slices.

### III. PROPOSED METHODOLOGY

In this paper, a new decision tree making algorithm is proposed to design a digital FIR filter using variable partition hybrid form structures. An FIR filter structure, a MAC is a process of multiplying the input data with the coefficient and accruing the result. Normally one MAC per tap is needed for FIR filters. The FIR filter structure consists multiply-accumulate block which itself has multiplier, adder and accumulator blocks. In this approach, it is possible to reduce the number of delay registers required in tap cells that can reduce hardware resource utilization significantly, and also the delay and power will be reduced as compared to the existing FIR Filter architectures.

#### A. Low power multiplier for FIR Filter Design

An FIR filter, the order varies the stopband energy of the input signal designed for low power applications. Multiplications are significant tasks in FIR filters to perform coefficient multiplication that consumes the large area. Multipliers assume a significant job in the present computerized signal processing and different applications. Low power utilization is additionally a significant issue in the multiplier. To minimize power utilization, it is a great idea to diminish the number of tasks of an FIR filter that reduces significant power consumption. The architect for the most

part focuses on rapid and low power proficient circuit structure. The goal of a decent multiplier is to give a physically packed together, high speed and low power utilization unit. FIR assumes a significant job in numerous correspondence systems such as noise reduction, filter matching, removal of interference, channel balance and so for. The area, time and power utilization of an FIR channel are to a great extent overwhelmed by the difficulty of multiplication. A few endeavors have been made to diminish this difficulty by multiplier-less FIR filter execution, which are present in TDF and direct form.

Every multiplication process is acknowledged by SCM in shift and add an approach based direct form channel. To get the final output, the partial product has been added by adder-tree. Then again, in a TDF channel, the present information test is increased by every one of the coefficients and the Structural Adder Block (SAB) to deliver the channel results. Multiplication operations are used for this type of situation are acknowledged by the MCM approach. The interest of high-speed processing has been expanding because of extending computer and DSP applications.

#### B. Existing Variable Size Partitioning Approach

The VSP is used as a Fixed-size Partitioning (FP) approach based on the Single Constant Multiplication (SCM) and Multiple Constant Multiplication.

- The feasible values of the partitioning parameter (L) in fixed hybrid channels increments with the order of filter (N). Then various estimations of L bring about various FA and register complexities, the structure choices in the FP-Hybrid filters are exceptionally huge. A particular estimation of L is determined by an experimentation technique and along these lines, the subsequent architecture line used for the chose estimation of L might be distant away from the ideal plan.
- The methodology utilizes just fixed-size MCM blocks to actualize a given coefficient set. We see that MCM tasks in every one of these partitions are not used in an effective manner. To illustrate, let this research take a 16-tap filter including the coefficient sequence  $h(n) = \{2, 2, -2, -5, 0, 10, 8, -12, -26, 0, 68, 128, 128, 68, \dots, 2, 2\}$  and consider  $L = 2, 6$  and  $12$ . The fixed-size MCM divisions are used for the consistent of L values. Subsequently, the sub-structure design sharing in MCM blocks relies upon the qualities of the channel coefficients. The fundamental goal of the VP is used to expel the requirement for choosing a particular benefit of minimizing factors and complexity of the arithmetic logic operation and hardware device utilization. In this way, in view of the above assumptions, two calculations are proposed to get proficient move and-include based DTG structure FIR filters, to be specific, (i) SCM- based VP Hybrid (SBVH) calculation and (ii) MCM based VP Hybrid (MBVH) calculation.

### (i) SCM-Oriented SOVH approach

This research is taken 16-tap filter including the coefficient sequence  $h(n) = \{2, 2, -2, -5, 0, 10, 8, -12, -26, 0, 68, 128, 128, 68, \dots, 2, 2\}$ .

The proposed research uses the 2-progressive coefficients to detect the importance of VSP, which is attained by utilizing the SCM-oriented hybrid form structure FIR filter. The breakdown of every division is found employing the H-hub algorithm and also corresponding shift and add topology. This existing work considers the 8-bits as an input word length. This analyze the SBCH formation structure saves ninety-six D Flip Flops (DFFs) in the delay line of input, fifty Full Adders (FAs) in multiplier module, 115 FAs in the Pre-Structural Adder (PSA) module, 50 DFFs & 52 FAs in the SAM module when the filter structure has eight DFFs in delay line of input, 34-FAs in the multiplier module, 96 FAs and 188 DFFs in the SAB AND 62 FAs in the PSA module. In order to increase the complexity of the existing filter architecture design, the SBVH scheme used to generate more

SCM modules. It has been widely mitigated adder size and complexity of the registers, which is mostly considered for low power applications.

### (ii) MCM-Oriented VP-Hybrid (MOVH) scheme:

This research paper proposed the SBVH scheme to implement the existing MBVH scheme [16], where the degree of general sub-expression sharing has been observed employing the Hcub approach. The work [16] finds that the divisions generated by the MBVH scheme are identical to that of the SBVH scheme. The MBVH scheme has reduced the complexity of FA and normal fan-out of the nodes in the multiplier module, it can be reduced the critical path delay of the filter design. Hence, the usage of the MBVH filter is efficiently suitable for high-speed FIR filter implementations of various nodes. Further, to reduce the area requirement and increase the speed of FIR filter design by DTG algorithm.

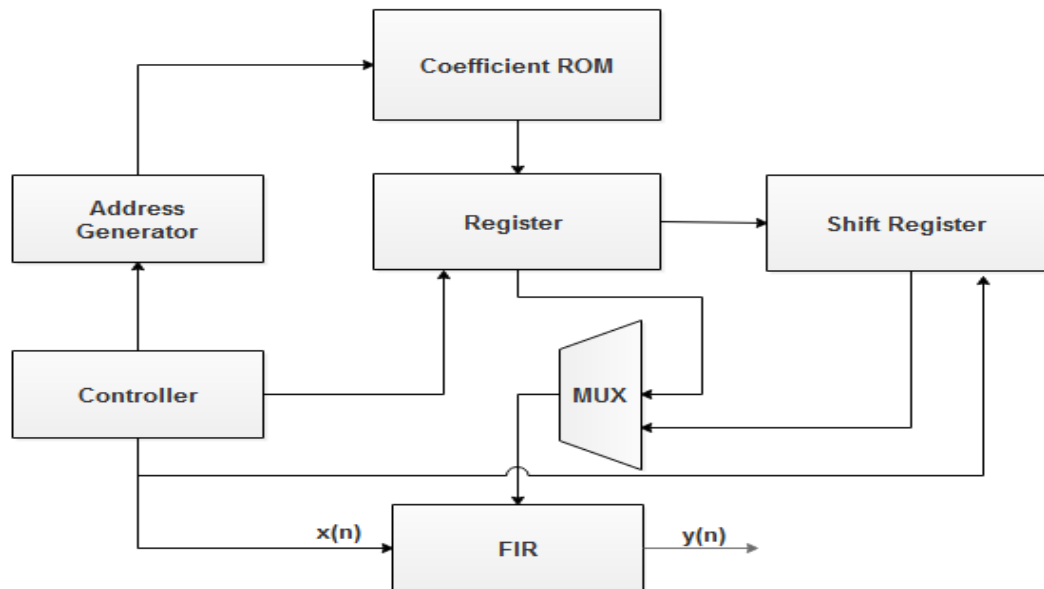


Fig. 1. Block diagram of the DTG- FIR filter architecture

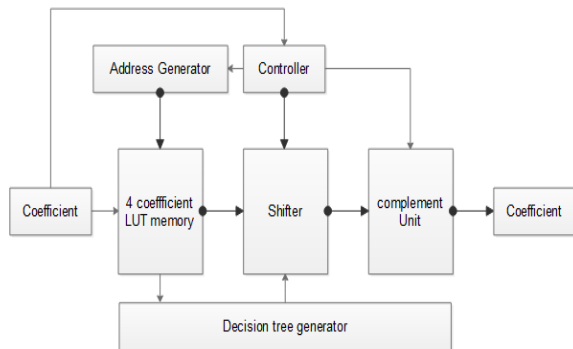
Fig. 1, explains the overall proposed architecture. The address generator, register, FIR and Shift register is controlled by the controller. One input of MUX is given to FIR and output to register and shift register. FIR channels, for the most part, need a single MAC for each tap. The structure of the FIR filter consists of multiply-accumulate block, which including adders, multiplier and accumulator modules. In this approach, it is possible to reduce the number of delay registers required in tap cells that can reduce hardware resource utilization and also the delay and power has been reduced than other FIR filter design works. The filter coefficients are used fixed-point, it can be reduced the complexity of truncation and computation in filter tap cells. The coefficients ( $h = \{3, 6, 0, -16, -19, 12, 76, 128, 128, 76, \dots, 6, 3\}$ ) are loaded into coefficient ROM of size 16. Controller unit controls register and shifter based decision tree will be generated based on the number of shift and add operation required for multiplication and accumulation to perform filtering. For each cycle, an instruction will be loaded from the decision tree unit to

evaluate a number of shifts required for that particular cycle. This proposed approach can avoid a number of intermediate delay registers between tap cells and uses a decision tree to execute tap cell operation. This proposed architecture will be implemented in Xilinx ISE and tested in Xilinx Virtex/ZED FPGA boards.

### (iii) Working principle of the proposed algorithm:

In FIR design, costly multipliers are avoided by using LUT based SCM/MCM for hardware implementations in previous research. The LUT based FIR filter store coefficients in ROM and SCM/MCM based shift and addition are performed in each tap cell according to variable partition algorithm (VPA). In the VSP approach, an important design issue is the optimization of LUT for the filter coefficient, which has direct impacts on the area cost of arithmetic units and registers.

In this research, the Decision Tree Generation algorithm (DTG) is introduced to reduce the LUT size to 40% of the conventional LUT in VP approach. In Figure.2, shows the block diagram of DTGA based FIR filter structure by using coefficient LUT optimization techniques.



**Fig. 2. Block diagram of the Coefficient LUT**

The DTG algorithm technique for LUT memory optimization with VP- FIR filter is explained in this section. The architecture is implemented based on the 16 taps direct form structure.

**Table- I: General 16-bit Coefficient LUT table for 16tap**

Address(C1)	Coefficient(C2)	Address(C3)	Coefficient(C4)
0000	A	1000	15A
0001	2A	1001	14A
0010	3A	1010	13A
0011	4A	1011	12A
0100	5A	1100	11A
0101	6A	1101	10A
0110	7A	1110	9A
0111	8A	1111	16A

**Table- II: Decision Tree for Variable partition FIR**

ROM Address	Coefficient(C1)	No of shifts	Result
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**Table- III: Comparative analysis of FPGA performance for existing and DTG-FIR filter design**

Target Devices	Methodology/Tap	LUTs	Flip-flops	Slices	Frequency (MHz)	Number of IOB
Virtex4 xc4vfx12	VP-FIR [16]	745/10944	287/10944	476/5472	71.163	34/240
	DTG-FIR	383/10944	139/10944	225/5472	169.173	25/240
Virtex5 xc5v1x20T	VP-FIR [16]	632/12480	287/12480	209/3120	82.70	34/172
	DTG-FIR	327/12480	139/12480	116/3120	186.822	58/172
Spartan6 Xc6slx4	VP-FIR [16]	645/2400	287/4800	235/600	73.633	34/102
	DTG-FIR	274/2400	135/4800	114/600	183.122	58/240

In this paper, the existing filter also implemented on the FPGA platform for performance comparison purposes. The performance of LUT optimized DTG-FIR and VP-FIR filter are presented in Table.1. A much suitable platform for digital filter design through the FPGA implementation for low complexity architectures such as LUTs, slices, flip-flops, frequency and Input-Output Block (IOB) are analyzed. The FPGA in VLSI offers a configurable architecture finished an array of modifiable arithmetic logic design in which programmable routing resources by the number of IOB are interconnected. The performance of the existing and proposed DTG-FIR filter is analyzed in FPGA Virtex-4, Virtex-5 and spartan-6 device. The FPGA performance of the DTG-FIR filter is evaluated on Virtex-4, Virtex-5 and Spartan-6 because these are high configuration devices. The DTG-FIR filter has been averagely reduced the 57.054% of LUTs, 52.911 % of flip flops and 51.489 % of slices at operating

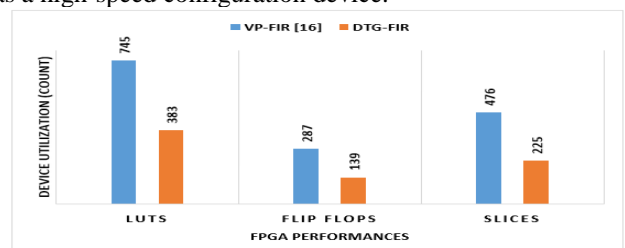
0000	1 x A	0001 << 1	2 x A(SCM)
		0001 << 2	4 x A(SCM)
		0001 << 3	8 x A(SCM)
		0001 << 4	16 x A(SCM)
0010	3A	0011 << 1	6A(SCM/MCM)
		0011 << 2	12A(SCM/MCM)
0100	5A	0101 << 1	0A(SCM/MCM)
0110	7A	0111 << 1	14A(SCM/MCM)

The 16 coefficients order of the VP-FIR filter is tabulated in Table.1. It is clear that for every coefficient in the fourth column (C4) of Table (1) of each row can be determined by 2's complement of coefficient in the C2 column of corresponding rows. The 2's complement of every coefficient on the second column of the same row showing negative mirror symmetry other than 8A and 16A. Based on the above symmetry property of the coefficients of every two columns reduces LUT size. The storing coefficient of C4 can be generated from C2. In table.2, the only 4 coefficients from odd positions are stored in LUT memory. The coefficients 2A, 4A, 8A and 16A can be generated by shifting 1A, 6A from 3A, 10A from 5A. The 16 number of stored LUT is reduced to 4-LUT memory by the approach. The reduction of 16 numbers of stored LUT to 4-LUT memory is given in this approach. If the coefficient loaded to taps are belongs to address '0', SCM is performed and for the remaining coefficients, combined SCM/MCM technique is performed. From previous work found that the proposed DTA based FIR design involves comparable area reduction than existing work.

## IV. RESULTS AND DISCUSSION

The VP shift and add based FIR filter with the LUT optimization technique are done in the FPGA Xilinx tool by employing Verilog code and performances are verified with different Virtex devices: Virtex-4 and Virtex-5, Spartan-6 by analyzing FPGA performance, which is explained in Table 3.

frequency of 183.122 MHz on the Spartan-6 than VP-FIR [16]. The Spartan-6 device is provided less device utilization compared to the Virtex-4 and Spartan-6, hence is considered as a high-speed configuration device.



**Fig. 3. Comparison graph of Virtex-4 performance for existing and DTG -FIR filter designs**

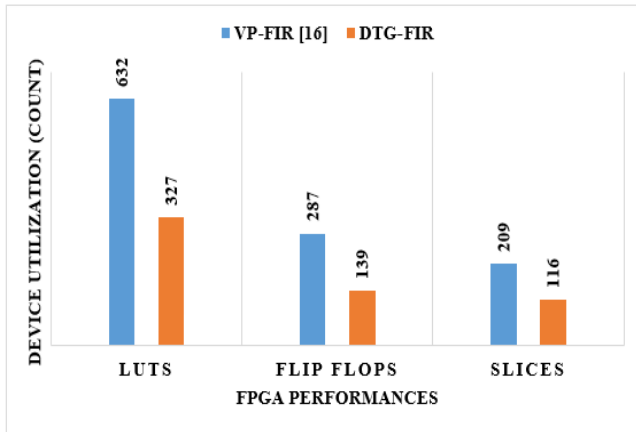


Fig. 4. Comparison graph of Virtex-5 performance for existing and DTG -FIR filter designs

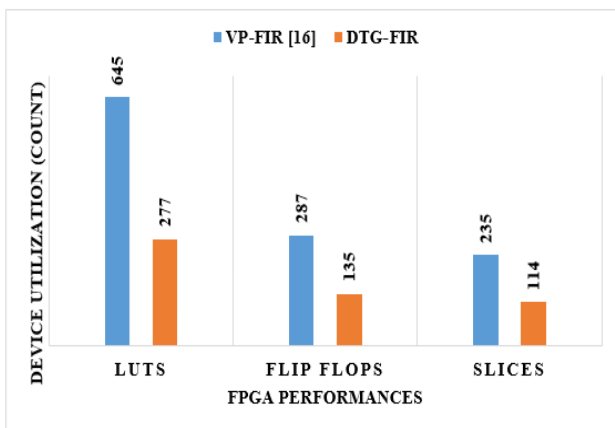


Fig. 5. Comparison graph of Spartan-6 performance for existing and DTG -FIR filter designs

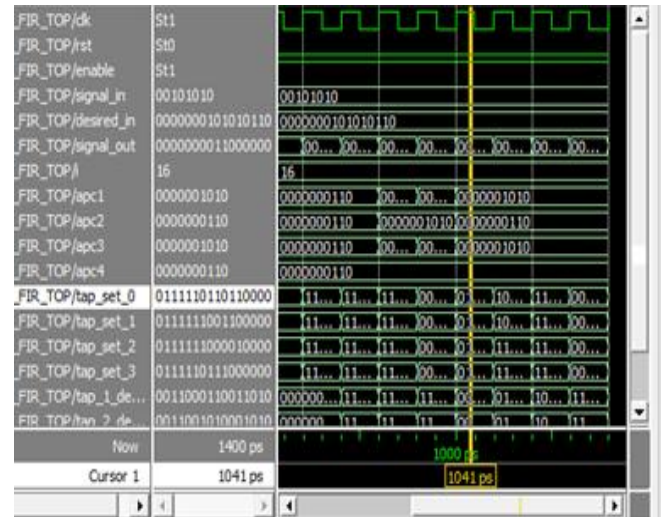


Fig. 6. The output waveform of the proposed DTG-FIR filter design

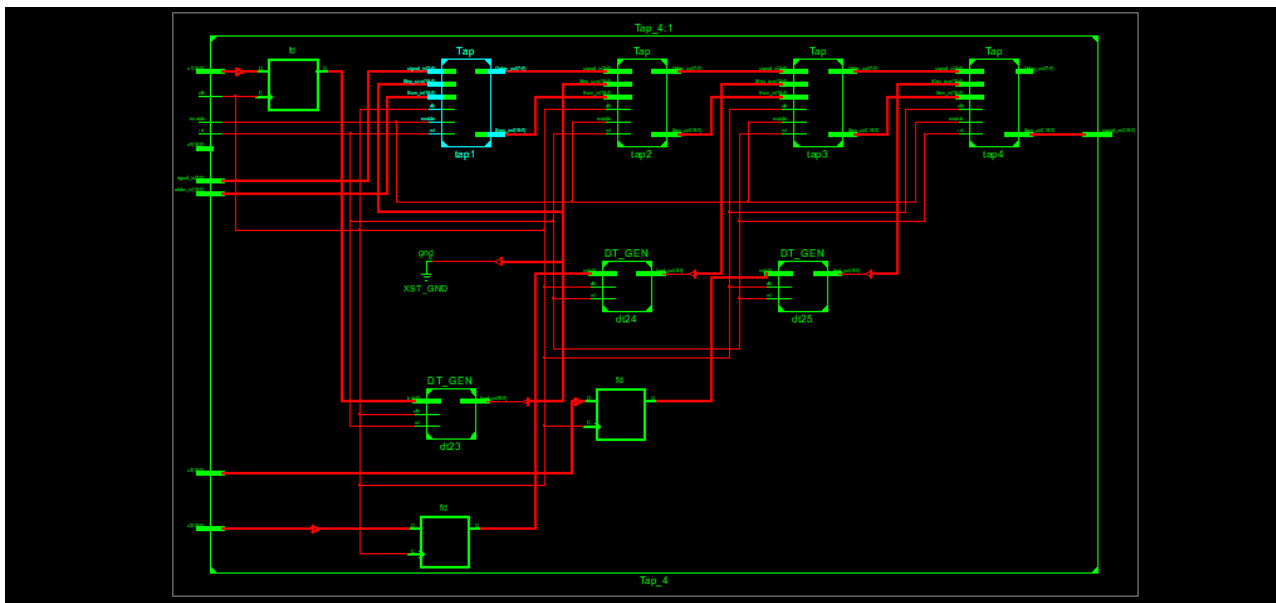


Fig. 7. RTL View of DTG-FIR filter

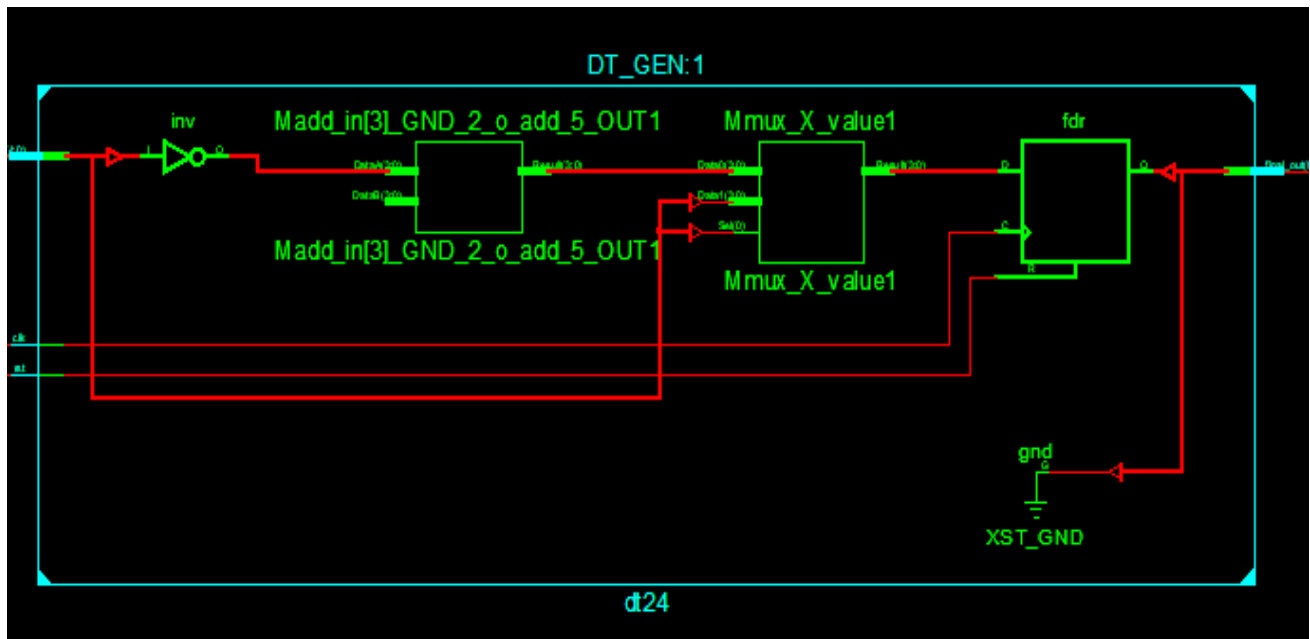


Fig. 8. RTL View of DTG algorithm

The DTG FIR filter design of the output waveform is shown in Fig.6. The correctness of the proposed FIR filter design validates the correctness of the design, which is simulated in the ModelSim software. The signal is randomly generated in the Random Access Memory (RAM) module, which values are multiplied with the coefficient. The RAM generates the signal in value, which is multiplied with the coefficient. To perform FIR filter operation instead of the normal multiplier, the shift and add method is used in DTG-FIR. The filter input data is multiplied with the filter coefficient, which gives the initial value and it is stored in the register y and accumulator contains zero which is added with y register. The clock cycle accumulator is used to store the result. The optimization of LUT by the DTG algorithm reduces the overall area of the filter. The overall architecture is synthesized in Xilinx for netlist conversion. The RTL netlist view of the proposed FIR filter design and DTG algorithm is shown in Fig.7 and 8 respectively. The entire device utilization of the proposed FIR filter architecture is superior compared to the existing filter design [16]. Hence, this proposed DTG-FIR is much suitable for the noise removal scheme in the DSP.

## V. CONCLUSION

Design of low power, low- area and high-speed FIR filter is always a difficult and challenging task for DSP applications. In previous research, the performance optimization of the FIR filter was done by using variable portioned SCM/MCM that provides high speed and low area architecture. In this research, along with the VP FIR filter, a novel method called decision tree generation algorithm is proposed using symmetric and shifting property of coefficients in LUT memory. The proposed DTG-FIR filter was designed in the FPGA Xilinx tool by using Verilog HDL. The proposed method reduced overall LUT memory size where only 4 coefficient LUT storage is required to design a 16 tap FIR filter. In the 16-tap Spartan-6 performance analysis, 57.054%

of the LUTs, 52.911 % of the flip-flops, 51.489 % of the slices is reduced compared to the VP-CLA FIR filter design. In this research, the FPGA performance was analyzed in three different Virtex devices, compared to these three device results the Spartan-6 has provided better results than the other two devices. Experimental results show that the proposed DTG-FIR filter design is much suitable for DSP applications because of LUT optimization. The FIR filter will be designed with debugging architecture to overcome testing complexity and to recover error logic in the future using Xilinx Zed board FPGA.

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