Design of Low Power Adders in Digital Circuits Suitable for Power Reduction in Multipliers

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Abstract*: Wireless devices are being evolved at an exponential rate. This evolution is focussing on the development of digital circuits which are incorporated into the processors. The evolutionary process involves individually or a combination of three main objectives namely

i) Reduction in size
ii) Reduction in power
iii) Increase in speed.

There is always a trade-off among the above said objectives. In specific multiplying operation inside a processor is one of the core areas where much power is being consumed. On the other hand adders are an integral part in the multiplier circuit. So this work concentrates on designing and analyzing power consumption of five adders namely conventional full adder, 3-transistor XOR based full adder, Gate Diffusion Input (GDI) based full adder, Static Energy Recovery Full (SERF) Adder and full adder using modified XOR gate and finding a resultant low power adder which when implemented for the addition process in multiplier will lead to a reduction in power consumption of multiplier. This in turn reduce the overall power consumption of the processor. The adders are designed using LTSPICE XVII in 180nm technology. The resultant Full Adder using modified XOR gate achieves 61.79% less power compared to conventional full adder and is suitable for multipliers.

Keywords: Full Adder, GDI, Power consumption, SERF, XOR gate.

I. INTRODUCTION

Power is an important resource in handheld wireless devices. This is due to the requirement of a large battery life of the device. Today the processors are of high level of integration and the processing speed is increased. So processors are consuming enormous amount of battery life for its applications[1].

To overcome the above issue the battery's capacity can be increased but it would make the battery size larger which resonates with the size of the device. Different researches are going on to find the supplement for the currently used lithium ion batteries. The other way to improve the battery life is by designing the appropriate low power circuits which can be used in the processor. A processor is made up of connections between large numbers of transistors to provide various digital operations. Thus the power aspect of these circuits made up of transistors can be improved by targeting one of the following two approaches:

i) Reduction in power consumption
ii) Reduction in power dissipation

A. Power Consumption Reduction

Power consumption is the amount of power required to do the arithmetic, logic and other types of operations in a processor. This is due to the switching of transistors between on and off state. Larger the operation, larger the power consumption would be and is due to more number of switching operations.

B. Power dissipation reduction

Power dissipation refers to the leakage of power. There are two variants of power dissipation namely static and dynamic power dissipation respectively. Nowadays static power dissipation is reduced to a larger extent, but a lot more can be done in dynamic power dissipation. This is because dynamic power dissipation is caused by a large number of factors such as parasitic capacitance, overlap capacitance, sub threshold conduction, junction leakage, etc.

In this paper we concentrate on power consumption reduction rather than reduction in power dissipation. The reduction in power dissipation involves large number of factors and that too resulting in minimum improvement in power. So we have decided to improve the performance by reducing the power consumption.

C. Need for choosing multiplier as a final target circuit

Multiplier operations are an integral part in all the processors. It is an essential function involving arithmetic and logic operations. Various types of multipliers such as array multiplier, vedic multiplier, wallace multiplier, etc are available and a common operation connecting all these multipliers is an addition operation. So our objective is to design a suitable low power adder which will fit into all of these multipliers. The paper comprises of five subsections each explaining the design and operation of each adder of interest. In the last subsection the summary of results is given in conclusion and the limitations can be carried as future work.

II. CONVENTIONAL FULL ADDER

The conventional full adder comprises of two XOR gates to complete the sum operation

and a combination of AND and OR gates to generate the carry [4]. It is a three input adder and each input consists of a single bit. The gates used in this paper are predominantly two input gates and are constructed

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using PMOS and NMOS transistors. The equations for a conventional full adder are

$$Sum = in1 \oplus in2 \oplus in3 \quad (1)$$

$$Carry = (in1 \,\&\, in2) + in3(in1 + in2) \quad (2)$$

The XOR circuit constructed for this adder is shown in Fig. 1

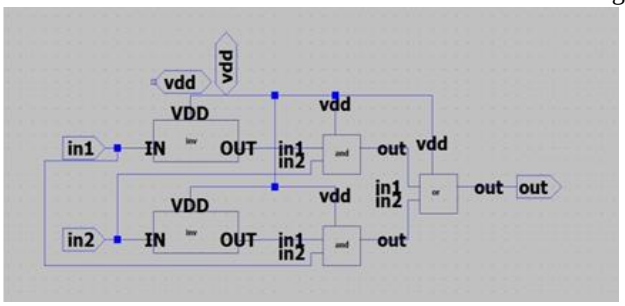

Fig. 1.Conventional XOR gate

The full adder circuit constructed using the above XOR gate and its subsequent symbol is shown in Fig. 2 and Fig. 3 respectively.

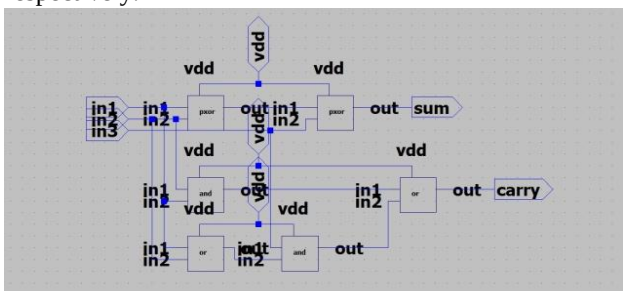

Fig. 2.Conventional Full Adder

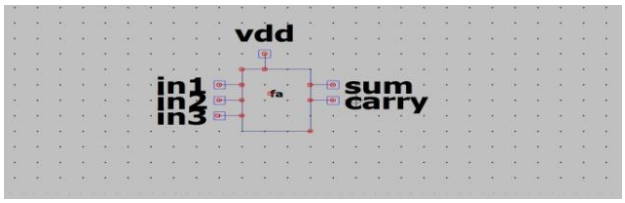

Fig. 3. Conventional Full Adder Symbol

The power consumption is calculated for the following cases for all the adders in this paper.

(i)All possible input combinations
(ii)Single input combination (111)

The test circuit for case i) is simulated and shown in Fig. 4 and it consists of three voltages pulses acting as inputs. The Von and Voff values are chosen as 1.8 V and 0 V respectively. The time period is chosen as 10ns, 20ns and 30ns respectively such that all the possible input combinations would be present for the adder. The circuit is having a power supply of 1.8V.

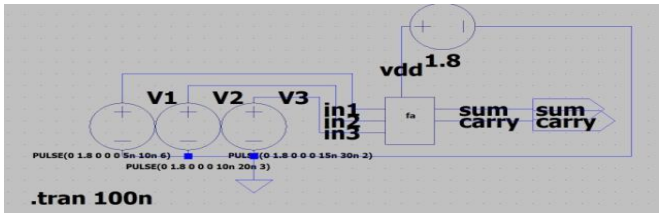

Fig. 4.Test Circuit I

The test circuit for case ii) is simulated and shown in Fig. 5. It is similar to the above test circuit in construction but the pulse inputs are replaced by a single DC voltage value of 1.8 V.

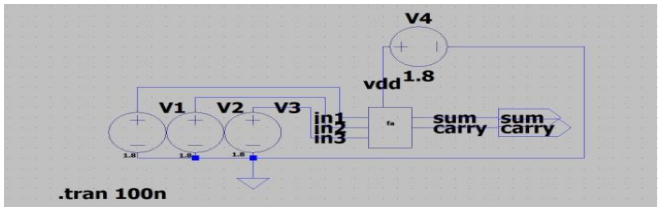

Fig. 5.Test Circuit II

The output waveform and the resultant power are shown in Fig. 6 to Fig. 8.

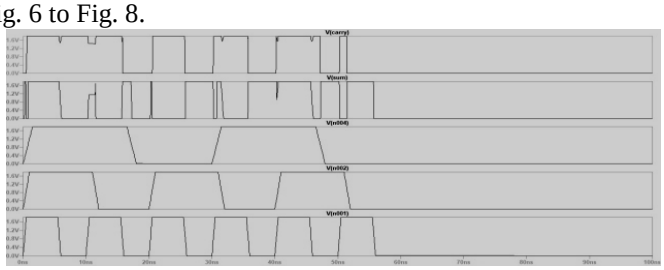

Fig. 6. Conventional Full Adder output for all input combination

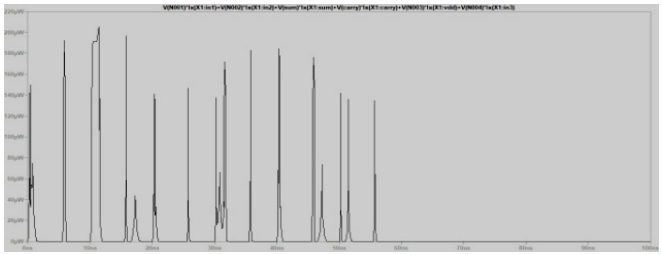

Fig. 7. Conventional Full Adder power output for all input combination

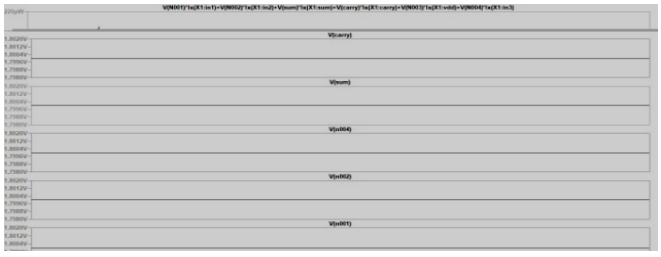

Fig. 8. Conventional Full Adder output for 111 input combination

The average power calculated for all input combination is 6.4384uW and for 111 input combination is 172.22pW respectively.

III. FULL ADDER USING 3 TRANSISTOR XOR GATE

The approach which uses the concept of three transistor XOR gate is simulated shown in Fig. 9. It is evident from the structure that this gate is one of the least complicated structures in terms of transistor count. It does

not require a separate supply and instead uses the input to the gate and source terminal.

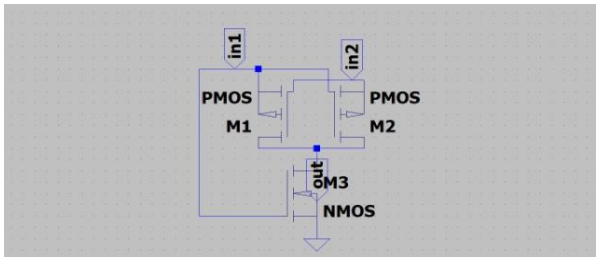

Fig. 9. 3-Transistor XOR Gate

The full adder is constructed using the 3-transistor XOR gate. The full adder constructed using the 3-transistor XOR gate and its symbol is simulated and shown in Fig. 10 and Fig. 11 respectively.

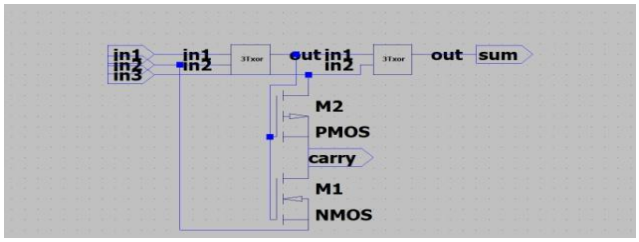

Fig. 10. 3-T XOR based Full Adder

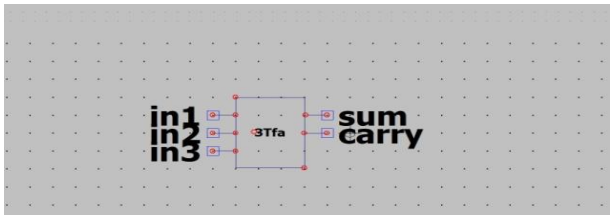

Fig. 11. 3-T XOR based Full Adder Symbol

The circuit is tested using the test circuits similar to Fig. 4 and Fig. 5 and only difference is the power source VDD is removed. The modified test circuits are simulated and shown in Fig. 12 and Fig. 13 respectively.

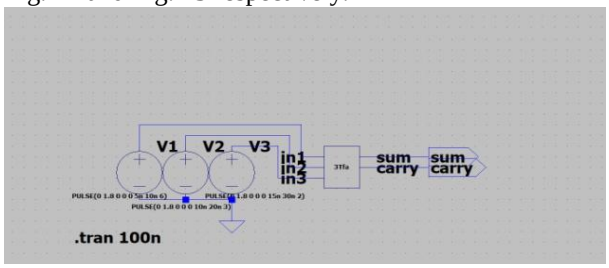

Fig. 12. 3-T based Full Adder Test Circuit I

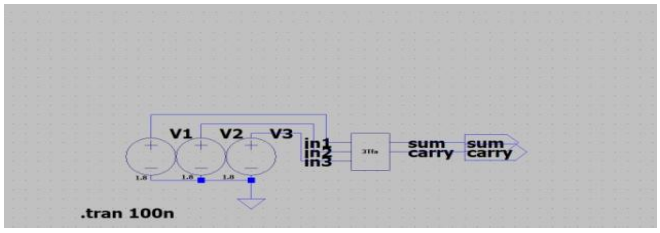

Fig. 13. 3-T based Full Adder Test Circuit II

The average power calculated for all input combination is 2.9623W and for 111 input combination is 28.198uW respectively.

IV. GDI XOR GATE BASED FULL ADDER

The Gate-Diffusion-Input full adder is aimed at constructing an adder with reduced number of transistors and subsequently the power consumption[2],[3]. It is done with the help of constructing a GDI based XOR gate. In brief GDI is similar to an inverter in structure but instead of a separate power supply source, it consists of three inputs connecting to gate, source/drain of PMOS and source/drain of NMOS respectively [4],[5] as shown in Fig. 14.

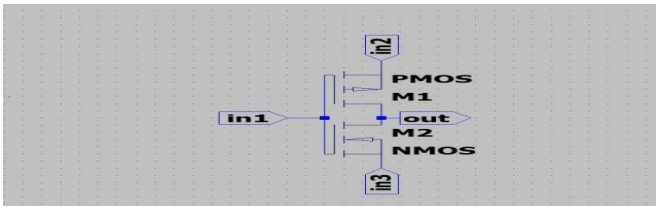

Fig. 14. Basic GDI PMOS & NMOS Circuit

By using different combinations of inputs, various outputs can be realized. The XOR gate realized using GDI is simulated and shown in the Fig. 15. This uses only 4 transistors which will lead to a reduction in power consumption.

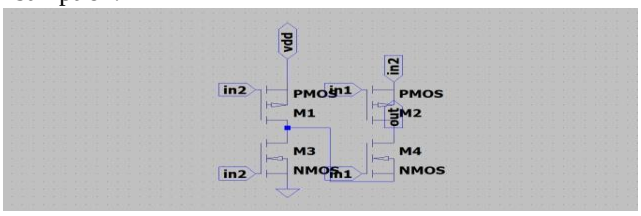

Fig. 15. GDI XOR Gate

By using the GDI based XOR gate, the full adder and its symbol are simulated and shown in Fig. 16 and Fig. 17 respectively.

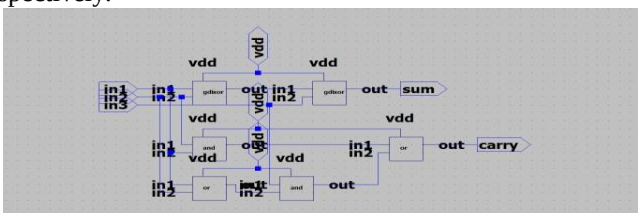

Fig. 16. GDI based Full Adder

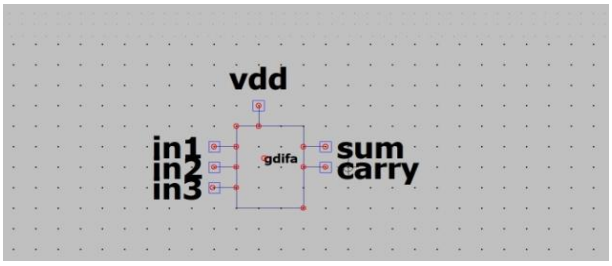

Fig. 17. GDI based Full Adder Symbol

The full adder is tested using the circuits in Fig. 4 and Fig. 5

for all input combinations and single input (111) combination. The output waveform and resultant power are shown in Fig. 18 to Fig. 20.

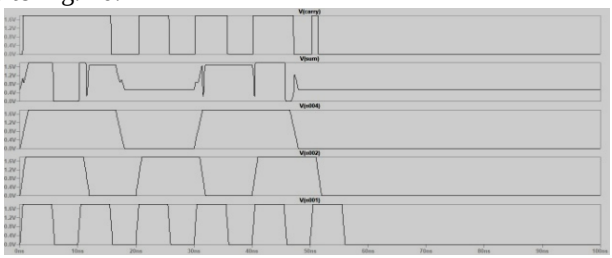

Fig. 18. GDI based Full Adder output for all input combination

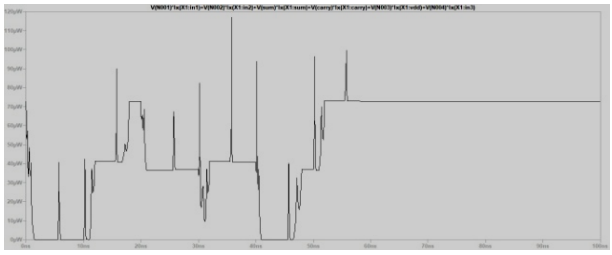

Fig. 19. GDI based Full Adder Power output

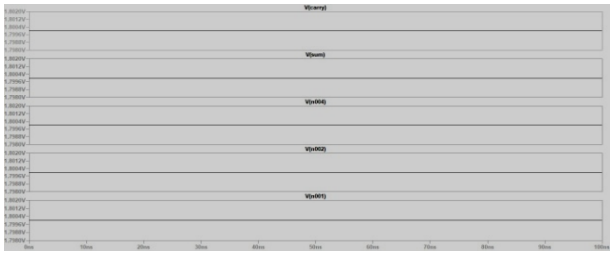

Fig. 20. GDI based Full Adder output for 111 input combination

The average powers calculated for all input combination is 49.686uW and for 111 input combination is 84.492pW respectively.

V. SER BASED FULL ADDER

The Static Energy Recovery Full (SERF) adder is one of the low power consuming full adder circuits [6]. SER based full adder design requires 10 transistors for its implementation. The principle of this design mainly attributes in eliminating the power supply and ground in the entire circuit. This is achieved by connecting the inputs to the gate, source and drain terminals. The SER based full adder is simulated and shown in Fig. 21.

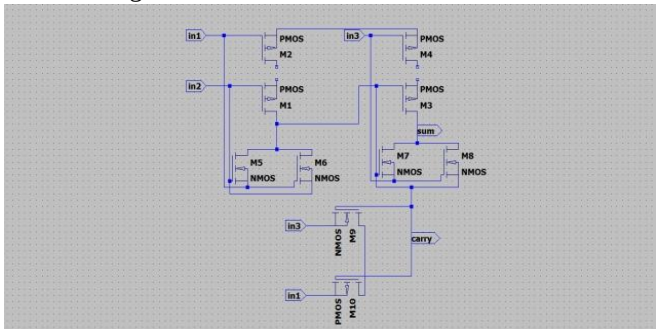

Fig. 21. SER based Full Adder

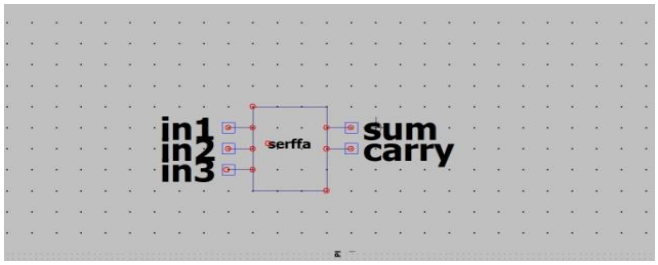

Fig. 22. SER based Full Adder Symbol

The symbol for the SER based full adder is created and shown in Fig. 22. The adder is checked for all input combinations and single input (111) combination using the test circuits in Fig. 12 and Fig. 13. The output waveform and the resultant power are shown in Fig. 23 to Fig. 25.

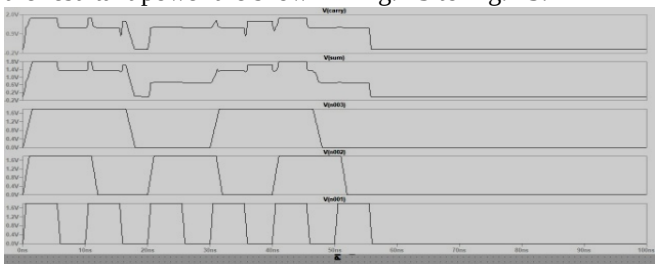

Fig. 23. SERF Output for all input combination

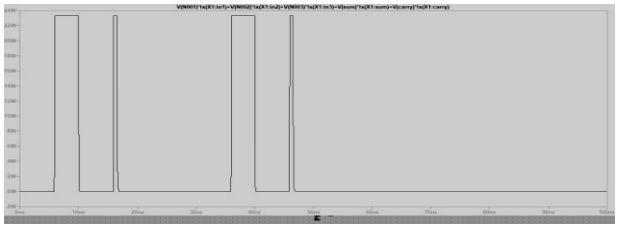

Fig. 24. SERF Power Output

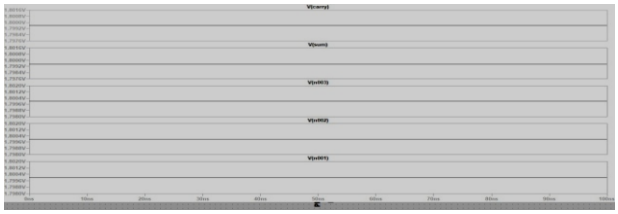

Fig. 25. SERF Output for 111 input combination

The average power for all input combination is 2.163W and 111 input combination is 6.0139pW respectively.

VI. FULL ADDER USING MODIFIED XOR GATE

The XOR gate is created using four NAND gates. It is a logic restructuring activity resulting in the same expression for XOR gate which is given in (3).

out = ((in1&(in1&in2)')'&(in2&(in1&in2)')')' (3)

The XOR circuit simulated and shown in Fig. 26.

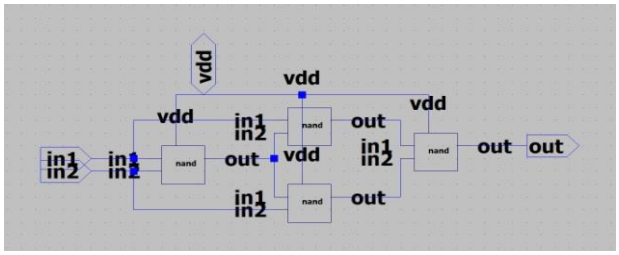

Fig. 26. Modified XOR gate

A full adder structure is simulated using the modified XOR gate. The simulated circuit structure and symbol are shown in Fig. 27 and Fig. 28 respectively.

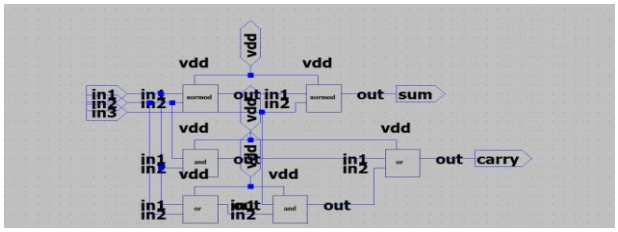

Fig. 27. Modified XOR based Full Adder

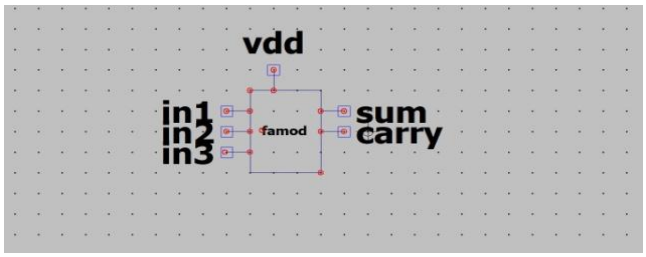

Fig. 28. Modified XOR based Full Adder symbol

The test circuits in Fig. 4 and Fig. 5 are used for calculating power for all the input combinations and selectively for input combination 111. The output waveform and the resultant power are shown in Fig. 29 to Fig. 31 respectively.

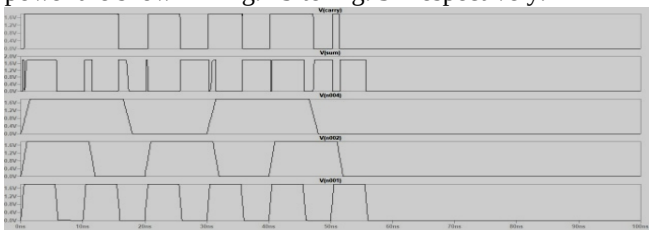

Fig. 29. Modified XOR based full adder output for all input combination

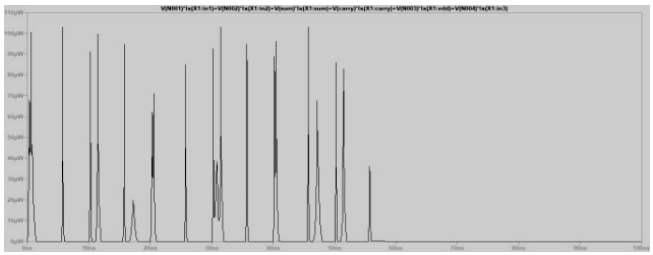

Fig. 30. Modified XOR based full adder power output

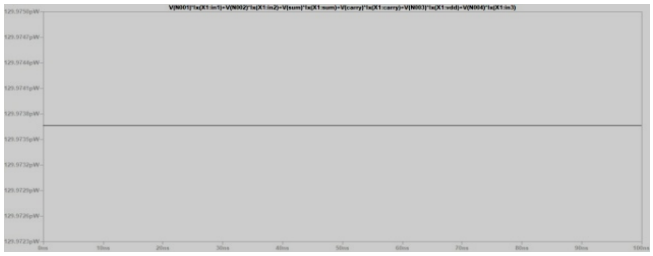

Fig. 31. Modified XOR based full adder output for 111 input combination

The average power for all input combination is 2.4604uW and for 111 input combination is 129.97pW respectively.

VII. RESULTS

The average power consumption for all input combinations and single input (111) combination and transistor count for various implementations of full adders are summarized in the table I.

Table I: Power Consumption table for Adders

Adder	Power consumption for all input combination (watts)	Power consumption for single input (111) combination(watts)	Transistor count
Conventional full adder	6.4384uW	172.22pW	68
Full adder using 3 transistor XOR gate	2.9623 W	28.198uW	8
GDI XOR gate based full adder	49.686uW	84.492pW	28
SERF based full adder	2.163W	6.0139pW	10
Full adder using modified XOR gate	2.4604uW	129.97pW	56

The conventional full adder is not a good choice for multiplier as it requires 68 transistors. The large number of transistors make the power consumption large due to large number of switching operations. From the power values of 3-transistor XOR based full adder, it can be seen that the power consumption for both the cases is high when compared to all other adders. This variation is attributed to the working of NMOS and PMOS transistor. NMOS transistor is a strong 0 and a weak 1 device and PMOS transistor is vice versa. Due to this there would be more power consumption and also there is a possibility of direct connection between source and

ground due to the propagation delay caused by different input combinations. These factors contribute to high power consumption.

The tabulated values for GDI and SER based full adder shows that power consumed for a single input (111) combination is less compared to conventional full adder. Whereas when the power is calculated for overall input combinations, the power is higher. It due to the working of NMOS and PMOS transistor that is NMOS transistor is a strong 0 and a weak 1 device and PMOS transistor is vice versa. In modified XOR gate based full adder the power consumption for all input cases are less when compared to the all other adders designed in this paper. This indicates that the

threshold issues associated with 3-Transistor XOR based adder, GDI XOR based adder and SERF is not affecting this circuit. But the power consumption of input case 111 is higher when compared to GDI XOR based adder and SERF.

VIII. CONCLUSION

Thus for a multiplier design, out of the five adders designed modified XOR based full adder can be a best choice. This is attributed to the fact that it has least average power consumption in the case of different input combinations used. It also ensures no or minimal loss in the input to output transition. For these adders other parameters such as propagation delay and speed may be compared in future and the power consumption can be improved.

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