International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-3, January 2020

Impact of Variation of Device Parameters on the Electrical Characteristics of Double-Gate Mosfets

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Abstract: ***Very large scale integrated circuits (VLSI) have been possible owing to the shrinking of metal-oxide semiconductor field-effect transistors (MOSFETs). By reducing the dimensions of the device it is possible to have high density on the chip. This increases the number of logical functions that can be implemented on a given dimension of the chip. Along with the advantages associated with the shrinking of the devices, it also has certain drawbacks commonly known as short-channel effects. Due to these effects, device characteristics deviate from its expected values. There are many techniques through which these deviations can be minimized. One of the promising and highly researched techniques these days is the use of Multi-gate (MG) transistors in VLSI. Double-gate (DG) transistor is one among MG transistors. In DG MOSFET, substrate is surrounded by gates from two opposite sides. This leads to more control over the channel electrons by the gate terminals. In this paper, the consequence of change of various device constraints on the electrical characteristics of the DG MOSFETs will be investigated. Through the results, one can know to what extent the electrical properties changes when the dimensions and/or material properties are changed. This will be very helpful in determining the maximum current associated with those dimensions of DG MOSFETs.***

Keywords: Double-gate, Drain current, MOSFET, Threshold voltage, VLSI.

I. INTRODUCTION

In conventional bulk metal-oxide semiconductor FET (MOSFET), there is unique gate as shown in Fig. 1(a). For increasing the compactness of the transistors on a single chip, the physical dimensions of the MOSFET is reduced. By following this method, the number of transistors has increased in a circuit over the last four decades. This increase in transistors is led by the law proposed by Moore which projected that the amounts of transistors on a single chip will be doubling itself after every approximately two years.

Revised Manuscript Received on January 30, 2020.
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This law virtually forced the researchers and the industry to come out with newer ways to raise the concentration of transistors on a particular chip.

Previously only the channel length was reduced but when it started showing certain limitations, other methods like reducing the oxide thickness and channel width

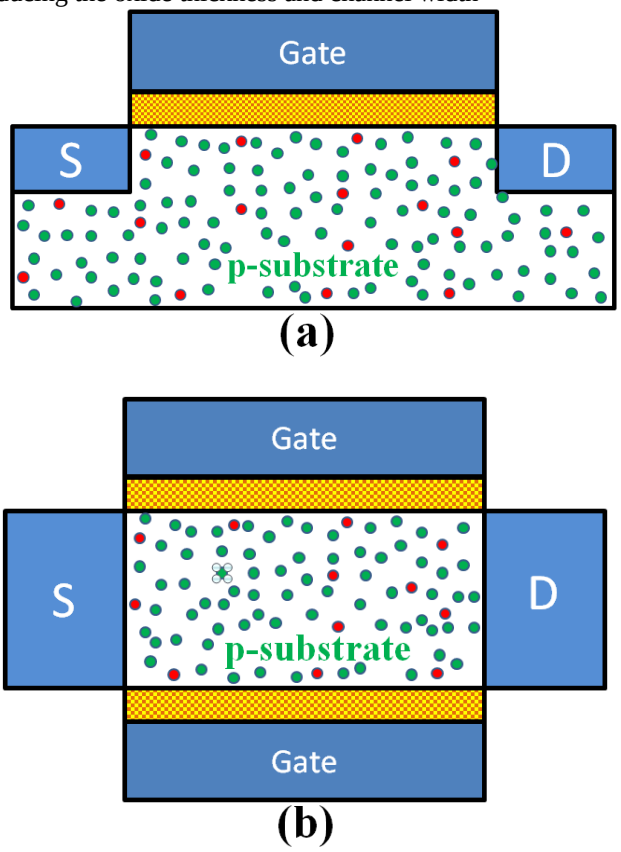

Fig. 1. Cross-sectional views of the (a) Conventional Single-gate n-MOSFET and (b) Double-gate n-MOSFET

were also incorporated. The limitations are the short-channel effects which come to picture when the dimensions are such that the source/drain fields start influencing the channel electrons. This affects the electrical behaviour of the MOSFET and it deviates from its intended characteristics.

II. LITERATURE REVIEW

In figure 1(a), the view corresponding to cross-sectional projection of conventional bulk n-MOS is shown. Under suitable terminal voltage conditions,

the conducting electrons form very thin layer of charge carrier layer near the gate and much of the substrate volume is of no use for the conduction. Therefore many techniques have been proposed in the literature [1−5] for the scaling of conventional MOSFETs.

In [6, 7], to have high equivalent gate-oxide thickness, high-K oxide materials as gate materials have been studied. Gate capacitance increases through this technique. In [8], strain has been used to increase the transport properties of the carriers (electrons/holes). By retaining the same dimensions, strained MOSFETs show better electrical properties.

Apart from these, there are reports of the use of multi-gate (MG) MOSFET architectures to follow the path of device miniaturization. There are various types of MG MOSFETs [9, 10] Gate controls the channel electrons and therefore the number of gate affects the electrical properties of the device.

Double-gate (DG) structure MOSFET is as depicted in figure 1(b). In DG devices, the substrate has two layers of gate due to which the substrate electrons are controlled more properly by the gate voltage. In the present work the electrical characteristics of DG MOSFETs have been investigated when their device dimensions have been varied. Firstly the effect of variation of device dimensions, doping concentrations and metal-gate layer work functions on the device threshold voltage of DG MOSFET have been evaluated and then their effects on the drain current have been analyzed.

III. THEORETICAL DETAILS

Poisson's equation relates the charge present in the MOSFET channel and its associated potential and is given as in

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon_{Si}} n_i e^{q(\varphi - V)/kT} \tag{1}$$

where, the symbol φ represents the electrical potential of the channel, V refers to quasi-Fermi level potential, q represents charge due to electrons, n_i denotes intrinsic channel concentration, k and T are Boltzmann constant and temperature. By applying following boundary conditions [11], solution of the above equation is found.

$$\frac{q\left(V_g - \Delta\phi - V\right)}{2kT} - ln\left[\frac{2}{t_{Si}}\sqrt{\frac{2\varepsilon_{Si}kT}{q^2 n_i}}\right] \tag{2}$$

$$= ln\beta \;\; -\ln[\cos\beta] + \frac{2\varepsilon_{Si}t_{ox}}{\varepsilon_{ox}t_{Si}}\beta\tan\beta$$

Using Pao-Sah's integration, the expression for drain current is

$$I_{ds} = \mu\frac{W}{L}\int_0^{V_{ds}} Q_i(V)dV \tag{3}$$

The analytical solution of the above equation gives current which, in linear and saturation regions are given as [11]

$$I_{ds,Lin} = 2\mu C_{ox}\frac{W}{L}\left(V_g - V_t - \frac{V_{ds}}{2}\right)V_{ds} \tag{4}$$

$$I_{ds,Sat} = \mu C_{ox}\frac{W}{L}\left((V_g - V_t)^2 - \frac{8rk^2T^2}{q^2}e^{\frac{q\left(V_g - V_0 - V_{ds}\right)}{kT}}\right) \tag{5}$$

here V_t corresponds to associated with MOSFET threshold voltage being given as [11]

$$V_t = \Delta\phi + \frac{2kT}{q}ln\left[\frac{2}{t_{Si}}\sqrt{\frac{2\varepsilon_{Si}kT}{q^2 n_i}}\right] + \frac{2kT}{q}ln\left[q\frac{\left(V_g - V_0\right)}{4rkT}\right] \tag{6}$$

where, $\Delta\phi$ is the metal semiconductor work function difference, kT/q denotes thermal voltage, t_{Si} represents silicon thickness, r symbolizes the structural parameter and other symbols have their usual meanings.

IV. RESULTS AND DISCUSSION

The computational results for DG MOSFETs are shown in figures 2−8. In the Fig.1, the bearing of doping profile concentration on the device threshold potential for various oxide-thicknesses has been computed. This figure indicates that by changing the doping concentrations in increasing order the threshold voltage decreases.

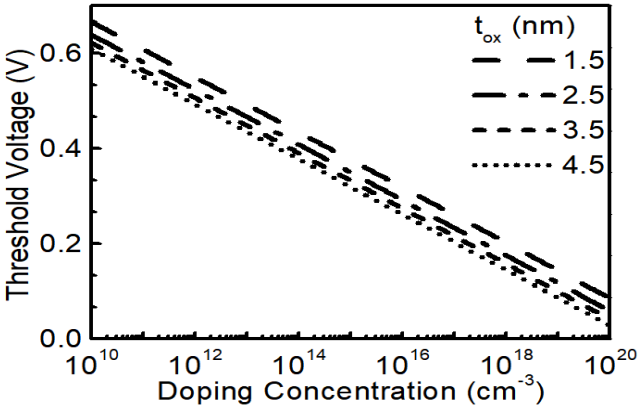

Fig. 2. Effect of variation of doping concentrations on the threshold voltage of DG MOSFET

Fig. 3 shows the change of threshold voltage with the variation in metal gate work function. When metal gate work functions are increased then the energy gap increases due to which lesser number of conducting electrons are able to cross the barrier and hence more gate voltage is required for the device to conduct.

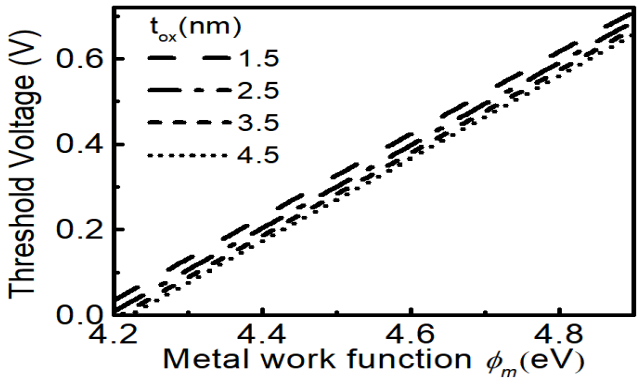

Fig. 3. Effect of variation of doping concentrations on the device threshold voltage (V_t) of the DG MOSFET

By the adjustment of device parameters, threshold voltages changes and this affects the drain current of MOSFET device. These effects on the drain current are shown in the following figures. In Fig. 4, drain current of the device as a relation of drain terminal potential has been plotted for a number of oxide thicknesses.

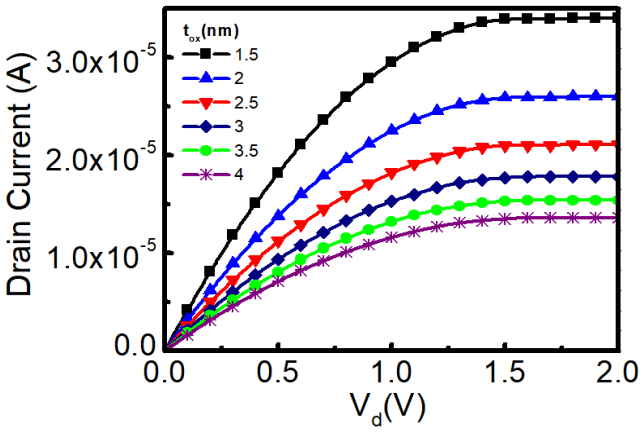

Fig. 4. Plots of drain current versus drain voltage for various oxide-thickness.

The effect of change in metal work function on the device drain current is as displayed in figure 5. As discussed earlier in this section, with the increase in work function property of metal gate, the energy barrier increases and therefore drain current decreases. To have more drain current, the metal work function should be less. But we cannot go for too less work function also since then the threshold voltage will decrease and will become very less and gate could be triggered by the surrounding noise voltages. Therefore the selection of appropriate metal gate is necessary for optimum performance of the device.

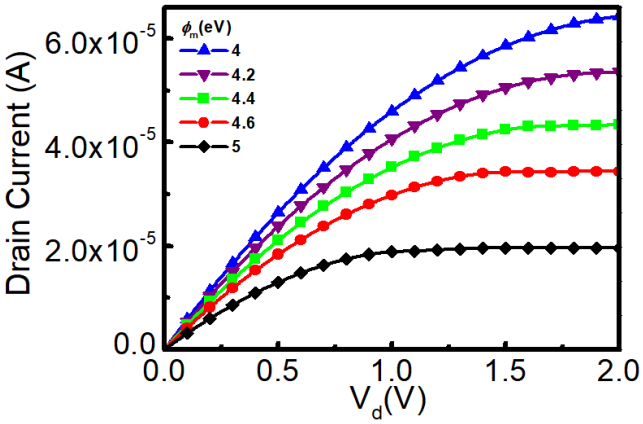

Fig. 5. Variations of drain current for varying metal work functions.

The effect of the variation of doping concentration the drain current of DG MOSFET is shown in figure 6. With the increase in doping the charge carriers increases. To increase the drain current, another technique that is used is the high-*K* dielectrics. These dielectrics increase the oxide capacitance and therefore the drain current increases. Along with the reduction of MOSFET dimensions, the oxide thickness also reduces. But there is a problem with the shrinkage in oxide thickness beyond a certain limit. If the device's oxide thickness is near the nanometer regime, the chance of quantum-effect increases. This is an undesirable thing and due to this the expected performance of the device will deviate from the error free state. Therefore instead of reducing the oxide thickness, if high-*K* dielectric is used then it will give better drain current characteristics as depicted in figure 7.

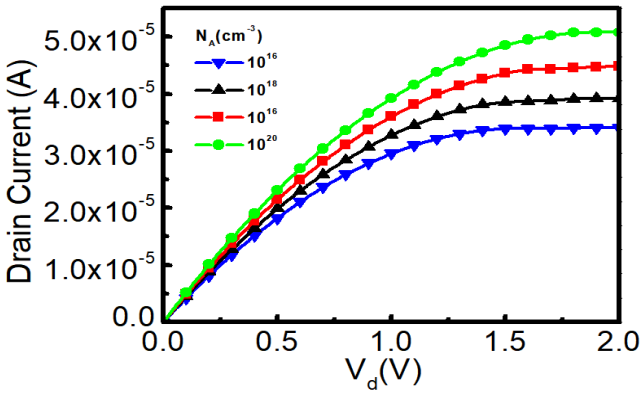

Fig. 6. Variations of the drain currents for different doping concentrations.

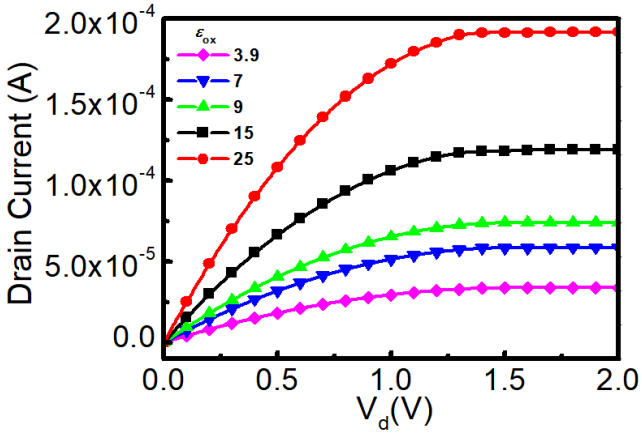

Fig. 7. Variations of the drain current of MOSFET for several gate-dielectrics.

V. CONCLUSION

The device parameters of DG MOSFETs have been varied and their effects on the various electrical characteristics have been analyzed. By changing the doping concentration, dielectric constant, metal work-function etc. the required threshold voltage and drain current can be achieved. From these analysis we can see the trade-offs involved in the selection of parameters for optimum characteristics. The maximum current for a given dimension can also be computed and compared for different device parameters. These results can help in choosing the suitable dimensions of the components of the VLSI related circuits.

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