

A Three-Phase Hybrid Cascaded Multilevel Inverter with Multicarrier PWM technique

Snehansu Panda, Santosh Sonar



Abstract: Multilevel voltage source inverter has drawn tremendous importance in the area of high power applications. This paper presents a three-phase modified hybrid cascaded multilevel inverter incorporating a standard three-leg inverter with H-bridge cells in series with each leg. The switching scheme with the multicarrier level shifted sinusoidal PWM is implemented to produce the five-level voltage at the output. Simulations have been performed using MATLAB to study voltage levels, modulation scheme, and THD. Finally, the possibilities of future works are addressed.

Keywords- Cascaded H-Bridge, Multilevel Inverter, , multicarrier PWM, power quality, THD

I. INTRODUCTION

The class of power converter that produce AC power from DC power is known as the inverter. Due to high total harmonic distortion and power losses of the regular square-wave and semi-square wave inverters, mark them unacceptable for high power applications such as AC power supplies, FACTS devices and drive system [1]. Multilevel inverters produce output voltages nearer to the pure sine wave. Therefore, it would minimize harmonics in the output voltage and improves the power quality. Apart from that, multilevel inverters produce low common mode voltage, less dv/dt across switches and low electromagnetic interference [2]. But it requires more than one isolated DC supply which makes system bulky and expensive to design. As the number of levels in output voltage achieves infinite then the THD approaches to zero. But the production of possible voltage levels is restricted by voltage unbalancing problem, packaging, and clamping problems [3]- [5]. The MLI is largely classified into three types (i) Diode clamped ;(ii) Flying capacitor;(iii) Cascaded topologies [6]. Cascaded model has advantages over diode clamped and Flying capacitor multilevel inverter. It has improved circuit design and packaging, results them suitable for industrial applications. It uses no extra clamping diode and capacitors [7]- [12]. There are different modulation scheme and control strategies have been implemented for multilevel inverter like sinusoidal pulse width modulation (SPWM), selective harmonic elimination(SHE-PWM), and state vector modulation (SVM) [13]- [16].

In this paper, a three-phase hybrid modified cascaded MLI is suggested incorporating standard three leg inverters with H-bridge cell in series with each leg [17,18].

The control scheme with level shifted multicarrier SPWM is implemented to produce five- level at the output voltage waveform. The technique also permits to maintain balanced voltage across capacitors of the half bridge inverter during load changing. Section II comprises the configuration and modelling of the proposed inverter. The multicarrier SPWM method is explained in section III. Simulations have been performed using MATLAB to validate the competence of the modified CHB MLI. The simulations results are presented and discussed in section IV. Section V concludes this paper.

II. CONFIGURATION AND MODELLING OF PROPOSED CONVERTER

A. Three-Phase Modified Hybrid Cascaded Multilevel Inverter

Fig.1. Presents the three-phase hybrid CHB multilevel inverter comprises of a conventional 3-leg inverter and H-bridge inverters in cascading with each inverter leg.

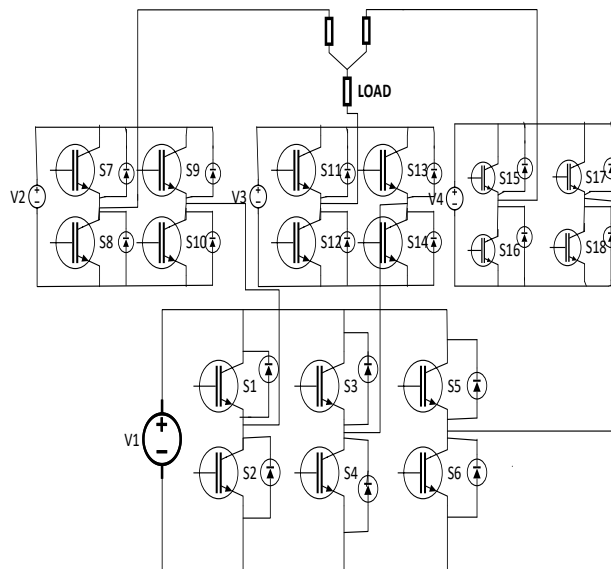


Fig. 1. Three-phase modified hybrid cascaded multilevel inverter

The proposed model will produce five level in per phase output voltage and nine level in line to line voltage waveform. The mathematical analysis is similar to single phase hybrid topology presented in Fig.2. Here the single phase hybrid CHB MLI is implemented by cascading of half-bridge and full-bridge inverters.

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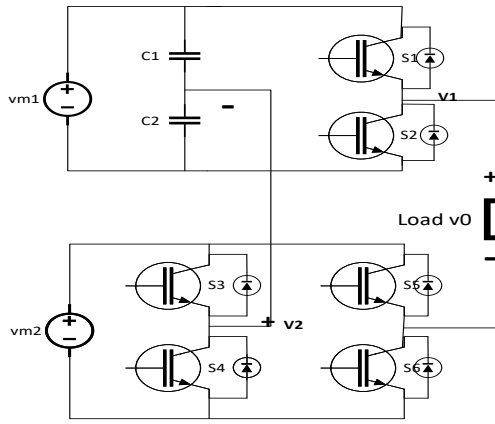


Fig. 2. Single-phase hybrid five-level cascaded multilevel inverter

This connection will generate the preferred levels at the output voltage waveform. It is found that, during switching only one of the DC supply is in contact with the load. So the half-bridge inverter model can be realized by using one isolated DC supply with two capacitors connected in series.

$$\text{Output load voltage } v_0 = v_1 + v_2 \quad (1)$$

Where v_1, v_2 are cell voltages

Here suppose $v_{m1} = 2E = v_{c1} + v_{c2}$ and $v_{m2} = E = v_2$.

v_{c1}, v_{c2} are capacitor voltages

Then the half bridge inverter will yield $\pm E$ and full-bridge inverter will produce $\pm E, 0$. So the five level output wave will be generated like $\pm 2E, \pm E, 0$.

The switching function is implemented below:

$$\begin{cases} S_i = 0 \text{ or } 1, \text{ if } S_i \text{ is off or on,} \\ \text{where } i = 1, 2, 3, \dots, 6 \end{cases} \quad (2)$$

Complementary switches can be realized as following:

Where S_i is any switch.

Complementary switches can be realized as following

$$s_2 = \bar{s}_1 = 1 - s_1 \quad (3)$$

Applying KVL law to single phase hybrid model and assuming:

$$v_{c1} = v_{c2} = E$$

$$v_1 = s_1 v_{c1} - s_2 v_{c2} = (2s_1 - 1)E \quad (4)$$

$$v_2 = s_3 E - s_5 E = (s_3 - s_5) \quad (5)$$

$$v_0 = v_1 + v_2$$

The corresponding six switching states of the proposed converters are presented in Table .1

Table 1 Switching States Of Hybrid Five Level Chb Mli Inverter

State	s_1	s_2	s_3	s_4	s_5	s_6	v_1	v_2	v_0
1	1	0	1	0	0	1	$+E$	$+E$	$+2E$
2	1	0	1	0	1	0	$+E$	0	$+E$
3	1	0	0	1	1	0	$+E$	$-E$	0
4	0	1	1	0	0	1	$-E$	$+E$	0
5	0	1	1	0	1	0	$-E$	0	$-E$
6	0	1	0	1	1	0	$-E$	$-E$	$-2E$

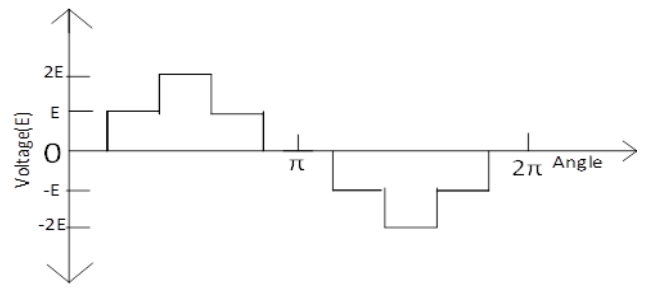


Fig. 3. Output waveform of single-phase hybrid CHB multilevel inverter

III. MULTICARRIER LEVEL-SHIFTED PWM TECHNIQUE

PWM is one of the most preferred methods of controlling the output voltage. It is implemented by adjusting the on or off period of switching pulses. It eliminates lower order harmonics. The higher order harmonics can be easily filtered out with the help of filter circuit. In order to generate m levels $m - 1$ carrier signals are upward shifted to one other. A level-shifted PWM can be classified as following types (i) Phase-disposition (PD); (ii) Phase opposite disposition (POD); (iii) Alternate phase opposite disposition (APOD). Here PD-PWM technique is implemented. In phase disposition all the carrier signals are in same phase.

$$\text{Modulation Index} = M = \frac{2V_{ref}}{(m-1)v_{tri}}$$

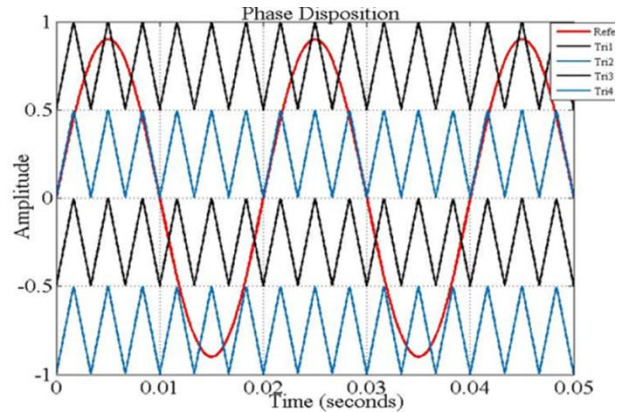


Fig. 4. Phase disposition PWM

In order to generate switching pulses high frequency triangular carrier signal v_{tri} is compared with V_{ref} , sinusoidal reference wave in a comparator. Mathematically can be represented as

$$\begin{cases} \text{if } V_{ref} \text{ is greater than or equal to } v_{tri} \text{ then } 1 \\ \text{else } 0 \end{cases}$$

Here V_{ref} = Peak value of reference signal and v_{tri} = amplitude of triangular signal.

In case of bipolar SPWM, if the $V_{ref} \geq v_{tri}$ then the top device of first leg is on else the bottom device. As the top and bottom switches of the same inverter leg are complementary in nature. But in case of unipolar SPWM two sinusoidal reference signals are required to produce switching pulses.

The reference signals are of same magnitude, frequency and 180° out of phase. In case of multicarrier technique, the carriers from maximum to minimum amplitude generates switching pulses related with highest possible voltage level to minimum. Fig.5. presents the switching pulses for five level hybrid MLI. Here four level shifted carrier waves ($C_{r1}, C_{r2}, C_{r3}, C_{r4}$) are compared with sinusoidal reference signal to generate the switching pulses. From fig.5. the level 1 switching pulses are fired to switches (S_1, S_3, S_6) to generate voltage $+2E$.

Similarly level 2 is responsible to produce voltage $+E$. Then pulse levels (3,4,5) produce voltage $0, -E, -2E$ at the output respectively. Here $TPWM = v_{ref} \times T_{tri}$, $0 \leq v_{ref} \leq 1$ $TPWM$ = Width of PWM signal, T_{tri} = Period of Triangle wave. Here $N = f_{tri} / 2f$ = Pulses per half cycle. Where f = reference signal frequency and f_{tri} = frequency of carrier signal. If triangular wave matches with zero of reference signal then $N - 1$ pulses per half cycle.

Modulation index = $M = V_{ref} / v_{tri}$

Modulation index controls harmonics in output and fundamental voltage value in the MLI.

In designing the switching pattern, proper care is to be taken in accordance with voltage balancing of capacitors. It needs a thorough investigation of switching states which influence the voltage of capacitor. While capacitor C_1 is discharging through load then C_2 is getting charged by the DC source and vice-versa. The capacitors have equal voltage values to get symmetrical output in voltage waveform. The switching technique generates more number of control states to produce same output voltage. Redundancy in the control states are not shown in Table-1. and used for voltage balancing purpose.

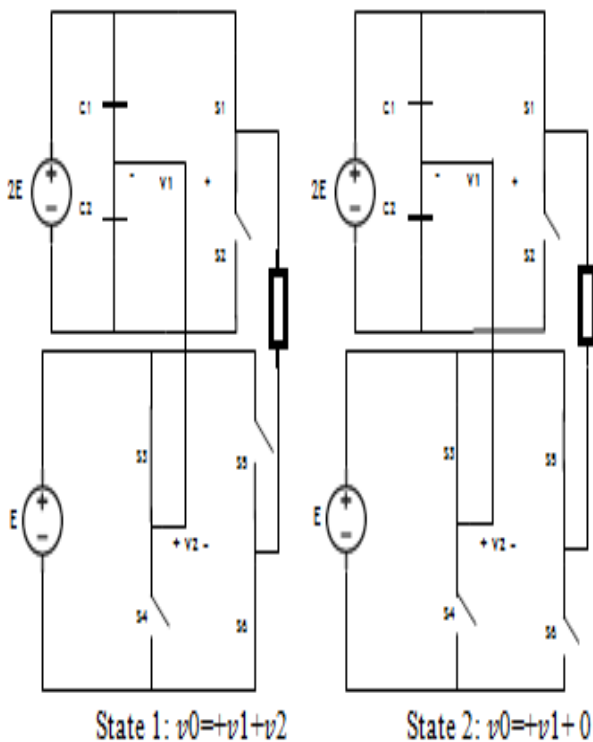


Fig. 6. Equivalent circuit of switching state1 and State2 listed in table 1

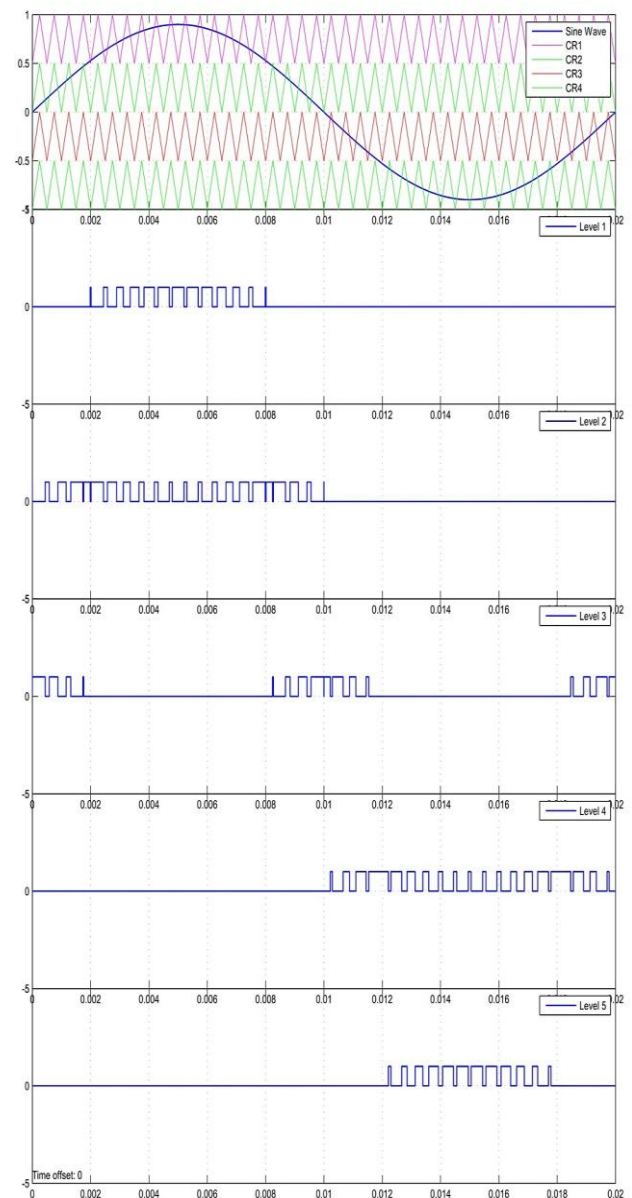


Fig. 5. Switching pulses for five level CHB multilevel inverter

IV. SIMULATIONS AND RESULTS DISCUSSIONS

The five-level hybrid CHB is simulated based on theoretical concept given in section III. The parameters used for simulation are listed in Table 2.

Table. 2. Simulation Parameters

Output Frequency	50Hz
Switching frequency	2 kHz
Capacitor values(C_1, C_2)	1 mF
DC voltage(E)	200 Volt
Load power	1kW
Modulation Index	0.9 (Phase disposition)

Fig. 7, Fig. 8 and Fig. 9 shows the load voltage, THD in voltage waveform and load current respectively. The simulation is performed with phase disposition PWM method.

The symmetrical levels in load voltage waveform justify the competence of the system. The THD of load voltage is shown in Fig.8. The dominant harmonic order

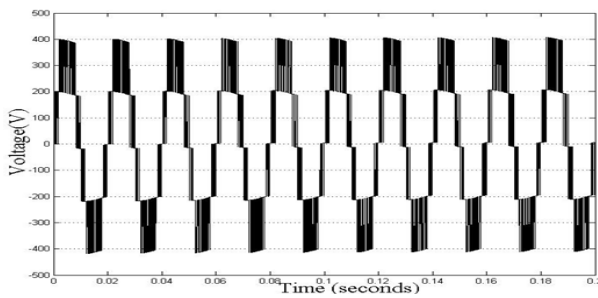


Fig. 7. Five-level load voltage

Present in switching frequency. The load current contains 1.96% THD. It is observed that while capacitor c_1 is discharging through load then c_2 is getting charged by the DC source and vice-versa.

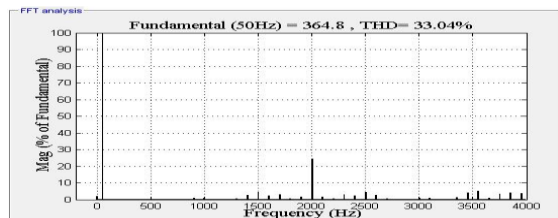


Fig. 8. Harmonic analysis of load voltage

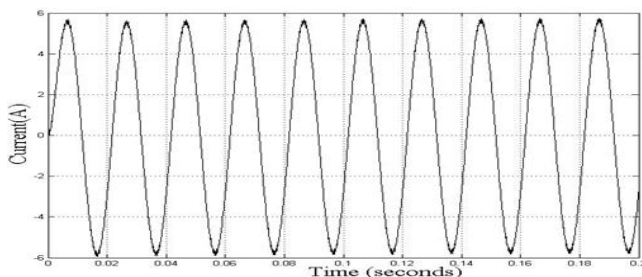


Fig. 9. Load current waveform

TABLE 3 Components Of One-Phase Of 5-Level Inverter

Type of multilevel inverter	Number of capacitors	Number of switches	Number of clamping diodes
Diode clamped	4	8	12
Flying capacitor	10	8	0
Cascaded H-bridge	0	8	0
Cascaded hybrid	2	6	0

V. CONCLUSION

In this paper, three phase modified hybrid CHB MLI has been proposed and simulated. Firstly, a single phase hybrid five level CHB is proposed using multicarrier level shifted SPWM. The symmetrical levels in load voltage waveform justify the voltage balancing of the system. It is observed that as the number of levels at output increases, THD decreases. Then a comparison between different MLI in

terms of component requirement is carried out. It is observed that modified CHB MLI is the most promising alternative for industry applications.

REFERENCES

1. J.-S. Lai And F. Zheng Peng, "Multilevel Converters A New Breed Of Power Converters," *Ieee Trans. Ind. Applicat.*, Vol. 32, No. 3, Pp. 509–517, May 1996.
2. F. Z. Peng, J. S. Lai, J.W. McKeever, And J. Vancovering, "A Multilevel Voltage-Source Inverter With Separate Dc Sources For Static Var Generation," *Ieee Trans. Ind. Applicat.*, Vol. 32, Pp. 1130–1138, Sept. 1996.
3. Y.-S. Lai And F.-S. Shyu, "Topology For Hybrid Multilevel Inverter," *Iee Proceedings-Electric Power Applications*, Vol. 149, Pp. 449–458, 2002.
4. J. Rodriguez, J. S. Lai, And F. Z. Peng, "Multilevel Inverters: A Survey Of Topologies, Controls, And Applications," *Industrial Electronics, Ieee Transactions On*, Vol. 49, Pp. 724–738, 2002.
5. J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, "Multilevel Voltage-Source-Converter Topologies For Industrial Medium-Voltage Drives", *Ieee Trans. Ind. Electron.*, Vol. 54, No. 6, Pp. 2930–2945, Dec. 2007.
6. Z. Du, L. M. Tolbert, B. Ozpineci, And J. N. Chiasson, "Fundamental Frequency Switching Strategies Of A Seven-Level Hybrid Cascadedhbridge Multilevel Inverter," *Ieee Trans. Power Electron.*, Vol. 24, No.1, Pp25–33, 2009
7. Z. Du, L. M. Tolbert, B. Ozpineci, And J. N. Chiasson, "Fundamental Frequency Switching Strategies Of A Seven-Level Hybrid Cascadedhbridge Multilevel Inverter," *Ieee Trans. Power Electron.*, Vol. 24, No.1, Pp. 25–33, 2009
8. J. Dixon, J. Pereda, C. Castillo, S. Bosch, "Asymmetrical Multilevel Inverter For Traction Drives Using Only One Dc Supply", *Ieee Trans. Veh. Technol.*, Vol. 59, No. 8, Pp. 3736–3743, Oct. 2010
9. S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, And J. I. Leon, "Recent Advances And Industrial Applications Of Multilevel Converters," *Industrial Electronics, Ieee Transactions On*, Vol. 57, Pp. 2553–2580, 2010
10. P. Roshankumar, P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, And L. G. Franquelo, "A Five-Level Inverter Topology With Single-Dc Supply By Cascading A Flying Capacitor Inverter And An Hbridge," *Ieee Trans. Power Electron.*, Vol. 27, No. 8, Pp. 3505–3512, 2012
11. M. F. Kangarlu And E. Babaei, "A Generalized Cascaded Multilevel Inverter Using Series Connection Of Submultilevel Inverters," *Ieee Trans. Power Electron.*, Vol. 28, No. 2, P. 625, 2013
12. H. Sepahvand, J. Liao, M. Ferdowsi, And K. A. Corzine, "Capacitor Voltage Regulation In Single-Dc-Source Cascaded H-Bridge Multilevel Converters Using Phase-Shift Modulation," *Ieee Trans. Ind. Electron.*, Vol. 60, No. 9, Pp. 3619–3626, 2013
13. B. P. McGrath, D. G. Holmes, "A Comparison Of Multicarrier Pwm Strategies For Cascaded And Neutral Point Clamped Multilevel Inverters", *Proc. Ieee Pesc*, Pp. 674–679, 2000
14. B. P. McGrath, D.G. Holmes, "Multicarrier Pwm Strategies For Multilevel Inverters", *Ieee Transactions On Industrial Electronics*, Vol. 49, No. 4, August, 2002
15. W. Yao, H. Hu, And Z. Lu, "Comparisons Of Space-Vector Modulation And Carrier-Based Modulation Of Multilevel Inverter," *Power Electronics, Ieee Transactions On*, Vol. 23, Pp. 45–51, 2018
16. M. Sharifzadeh, H. Vahedi, A. Sheikholeslami, P.-A. Labbé, And K. Al-Haddad, "Hybrid Shm-She Modulation Technique For Four-Leg Npc Inverter With Dc Capacitors Self-Voltage-Balancing," *Ieee Trans. Ind. Electron.*, Vol. 62, No. 8, Pp. 4890–4899, 2015
17. P. Rajeevan, K. Sivakumar, K. Gopakumar, C. Patel, And H. Abu-Rub, "A Nine-Level Inverter Topology For Medium-Voltage Induction Motor Drive With Open-End Stator Winding," *Ieee Trans. Ind. Electron.*, Vol. 60, No. 9, Pp. 3627–3636, Sep2013
18. V. Nair R, S. Pramanick, K. Gopakumar, And L. G. Franquelo, "Novel Symmetric Six-Phase Induction Motor Drive Using Stacked Multilevel Inverters With A Single Dc Link And Neutral Point Voltage Balancing", *Ieee Transactions On Industrial Electronics*, Vol. 64, No. 4, April, 2017

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Snehansu Panda was born in orissa, India in 1990. He received the graduation from BPUT, Orissa and master's degree in electrical engineering from Thapar Institute of Engineering and Technology, Patiala, India in 2011 and 2017 respectively. His research interests includes power converter, SMPS and AC-AC converter design. Presently working as Project Engineer in Power system installations of Indian Railway electrification Project.



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