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# Design a Full Adder Circuit using Modernized Full Sway Exclusive-Or and Exclusive-Nor Gates in 130nm Mentor Graphics

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***ABSTRACT:*** ***In this manuscript, new circuits for XOR/XNOR and concurrent XOR-XNOR purposes are designed. The designed trails are elevated lessened in expressions of the power usage and delay, which are appropriate to low harvest capacitance and low short-circuit power wastage. The designed new hybrid 1-bit full-adder (FA) trails related on the new full sway XOR-XNOR gates. Every designed circuit give their prospective advantages in period of speed, power usage, power delay product (PDP), and dynamic facility and so on. To know the performance of the intended designs, wide-ranging Mentor graphics simulations are carried out. The replications outcomes, supported on the 130-nm CMOS knowledge signify the intended intends have higher rapidity and power over supplementary FA devises. An innovative transistor sizing mode is accessed to reduce the PDP of the tracks. In the designed process, the algebraic working out particle swarm optimization module is utilized to obtain the preferred assessment for finest PDP with less iteration. The designed tracks are checked in times of dissimilarities of the supply, threshold voltages, input noise immunity and size of transistors.***

***Catalog Terms- Full adder (FA), noise, transistor sizing method, EXOR-EXNOR.***

## I. INTRODUCTION

Full adder is the basic adder design used to implement in digital signal processors and microprocessors. The new technologies are used to design the Full adder in spintronic equipment related to magnetic tunnel junction used to design the digital circuits. While the torque that is twist variation torque (STT) is achieved by help of twist-hall effect (SHE). And also the hybrid technology is used because the conventional CMOS has not giving the better performance in terms of power. The full adder is also designed by using 3T XOR and XNOR gates. Here the gate distribution technique contribution (GDI) and multiple verge voltage transistor is used and compared with the stagnant energy recovery Full (SERF) adder in addition with the occupied sway operation.

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In these days the ultra low voltage gives the low power consumption. Likewise the full adder with 8 bit additions are done by using the 1T1R resistive random access memory (RRAM) gives lesser number of computations. By the XOR and XNOR the one bit can be extended to 32 bit. The GPDK is also involved to reduce the number of transistors from 28 to 6.The MOS capacitors are also involved to minimize the power wastage, vicinity, impediment and Power delay Product (PDP). The above all technologies uses the Hspice, Cadence and virtuoso in CMOS and FinFET technologies with 32nm to 180nm are used and explained in [1]-[9]. The full adder is also designed by using the six hybrid EXOR and EXNOR circuits, addition and transmit are designed by using 13 transistors, the same EXOR and EXNOR designs the 8T full adder and compared the results with 10T and also SERF technology is used to design the Full adder using 45nm to 250 nm Tanner software is illustrated in [10]-[13]. The Quantum Dot cellular automata (QCAD) designer designs the decimal full adder with gates and not gate and sometimes these logic gates are replaced by partially utilized majority (PUM) gates based on the logic required. The magnetic QCA with hybrid technology is designed, NT and NTG reversible gates implemented in optical and quantum reversible designs for the reduction of area and cost are described in [14]-[16]. This paper projects the 3-bit adder design by minimizing the number of transistors from 12T to 6T by using the fundamental PMOS and NMOS logic are implemented in 130nm Mentor Graphics tool is discussed in [17].Some papers projects the plasmonic waveguides by laying the $sio_2$ film and uses the CMOS design to design the full adder justifies in [18]. The basic ternary logic is the technique used to design the simple circuits with low power consumption by ternary grapheme barristers are defined in [19].

## II. POWER REQUIREMENT FOR CMOS VLSI DESIGN

There are three basic points to be discussed intended for usage of the power in a switched CMOS VLSI design

a) Switching Power: the charge and discharge of the design capacitances while the transistor gets ON and OFF.
b) Short-circuit power: used because of short circuit current passed through VDD to ground at the time of transistor ON and OFF situations.
c) Static Power: used because of static and leakage current passing while the devise is in constant state.

The first two definitions situates that the dynamic power is used when the design is in transition stage.

Dynamic power gives the overall power used in switched CMOS design. It is relative to the input given to the design and makes the transistors to change their states or to continue with state. The third one is insignificant for a perfect CMOS course Design.

The overall power is given as:

$$P_{total} = V_{dd}.F_{clk}.\sum_i.V_{swing}.C_{load}.P_{i+} + V_{dd}.\sum_i.I_{isc} + V_{dd}.I_l$$

Where

$V_{dd}$ = Power supply voltage;

$V_{swing}$ = Voltage sway of the output which is perfectly equalto $V_{dd}$;

$C_{load}$ = Load capacitance at node i;

$F_{clk}$ = system clock frequency.

$P_i$ = switching activity at node I;

$I_{isc}$ = short circuit current at node I;

$I_l$ = leakage current

This addition gives node capacitances of the design.

## III. EXISTED EXCLUSIVE-OR AND EXCLUSIVE-NOR CIRCUIT

In this paper we presented an existed Exclusive-OR and Exclusive-NOR circuit with 10 transistors visualized in Figure 1(a). It works with a swaying method next to the productivity of the Exclusive-NOR applied for every effort combination and operates normally for the enter combinations A as logic'1' and B as logic'0'. This causes complexity for the circuit. So we had gone for the intended algorithm where this disadvantage is erased. As visualized in Figure 1(a) the circuit is given as logic'1' for B, then the PMOS transistor $M_2$, $M_3$ are in OFF condition and NMOS transistor $M_8$, $M_9$ are in ON condition. Then EXCLUSIVE-ORgives the output as complement of input A, while the EXCLUSIVE-NOR gives the output as input A logic.

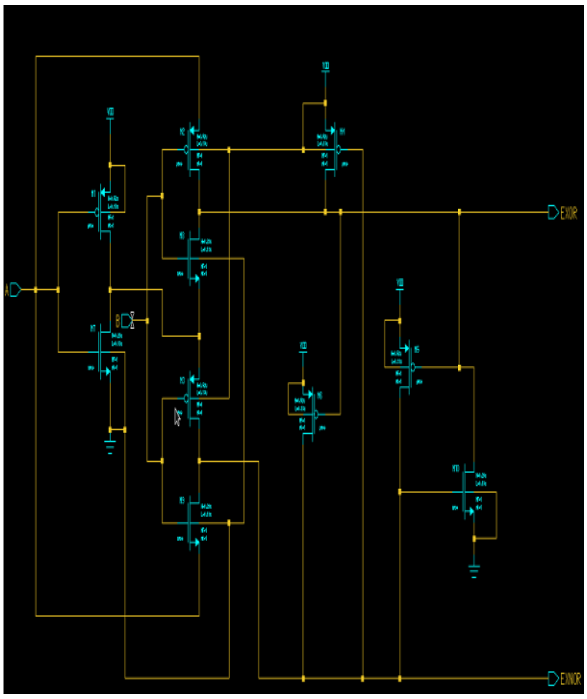


**Fig. 1(a): Existed EXCLUSIVE-ORand EXCLUSIVE-NOR Design**

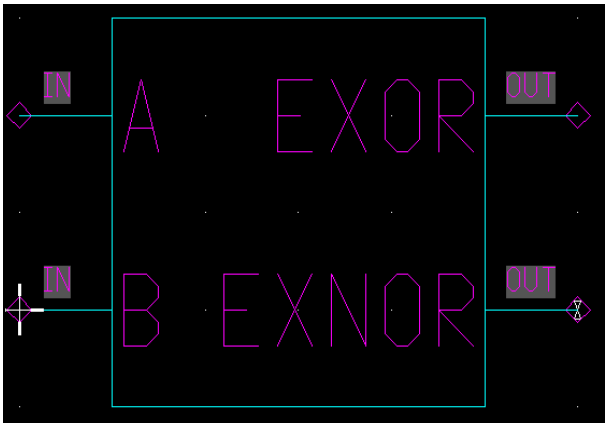


**Fig 1(b): Existed EXCLUSIVE-OR and EXCLUSIVE-NOR Symbol**

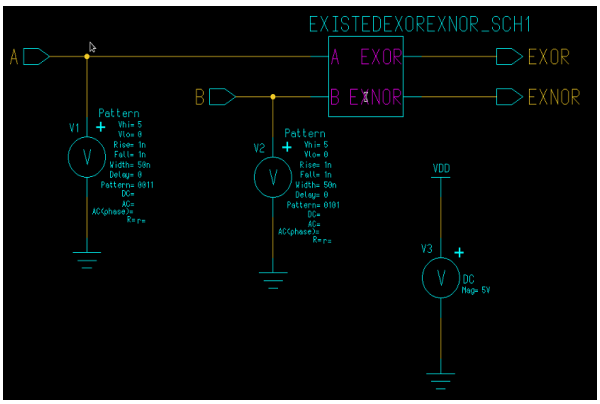


**Fig. 1(c): Simulated Schematic of Existed EXCLUSIVE-OR and EXCLUSIVE-NOR**

**Table (1) : Truth table for the Existed EXCLUSIVE-OR and EXCUSIVE-NOR Design**

| Key In | | Key Out | |
|---|---|---|---|
| Logic A | Logic B | EXCLUSIVE-NOR | Exclusive-OR |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 (swaying occurs) | 1 |
| 1 | 1 | 1 | 0 |

The Figure 1(b) represents the symbol for the Existed EXCLUSIVE-OR and EXCUSIVE-NOR schematic and Figure 1(c) represents the replicated schematic of existed EXCLUSIVE-OR and EXCUSIVE-NOR design. When the input A has given with '1' and B as '0' then EXCUSIVE-NOR results as complement of A, since PMOS transistor $M_3$ is in ON state and NMOS transistor $M_9$ is in OFF state. And the EXCLUSIVE-OR results as input logic A given since PMOS transistor $M_2$ is in ON condition and NMOS transistor $M_8$ is in OFF condition. But it suffers with swaying operation in voltage.

## IV. INTENDED EXCLUSIVE-OR AND EXCLUSIVE-NOR DESIGN

The novel intended EXCLUSIVE-OR and EXCUSIVE-NOR is design visualized in Figure 2(a).

This does not overcome the problems a raised in existed EXCLUSIVE-OR and EXCUSIVE-NOR design that is swaying operation designed for the keys A as '1' and B as'0. This problem is overcome by using the restitution response loop by the transistors $M_5$ and $M_{10}$. In the intended design the inputs are given A and B as logic '0' then $M_2$ and $M_3$ transistors are in ON state then EXCLUSIVE-OR gives outcome as '0' and EXCUSIVE-NOR as product'1'. But this logic '0' output for EXCLUSIVE-OR is in BAD condition. Then the restitution response loop is arranged with the help of $M_4$ and $M_6$ transistors. Then the other efforts A as'0' and B as '1' then $M_8$ and $M_9$ transistors are in ON condition. Then logic'1' results at EXCLUSIVE-OR but this is in swaying situation while the EXCLUSIVE-OR results logic'0'. This swaying situation overcomes by restitution loop.

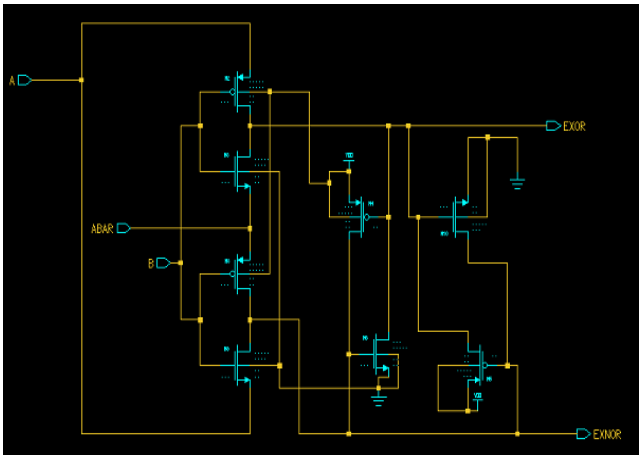


**Fig 2(a): Intended EXCLUSIVE-OR and EXCUSIVE-NOR Design**

**Table (2): Truth table for the Intended EXCLUSIVE-OR and EXCUSIVE-NOR Design**

| Key In | | Key Out | |
|---|---|---|---|
| Logic A | Logic B | Exclusive-Nor | Exclusive-Or |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 (Swaying overcomes through restitution loop) | 1 |
| 1 | 1 | 1 | 0 |

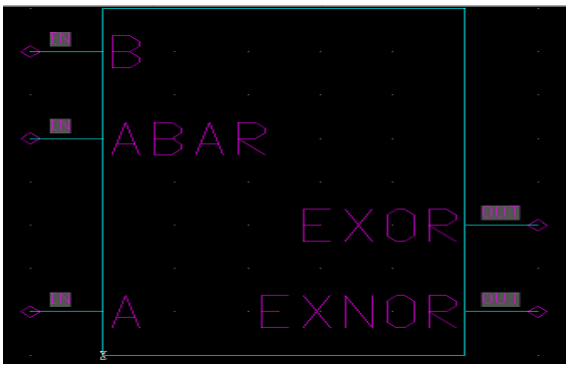


**Fig. 2(b): Intended EXCLUSIVE-OR and EXCUSIVE-NOR Symbol**

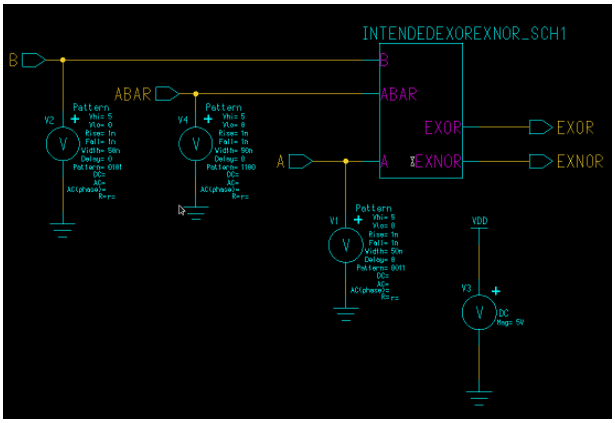


**Fig. 2(c): Simulated Schematic of Intended EXCLUSIVE-OR and EXCUSIVE-NOR**

The Figure 2(b) represents the symbol for the Intended EXCLUSIVE-OR and EXCUSIVE-NOR schematic and Figure 2(c) represents the replicated schematic of intended EXCLUSIVE-OR and EXCUSIVE-NOR design. Then the contributions given A as'1' and B as'0' then $M_2$ and $M_3$ transistors are in ON condition, the logic'1' results at EXCLUSIVE-OR and logic'0' at EXCUSIVE-NOR but the EXCUSIVE-NOR result faces swaying, this overcomes by restitution of $M_{10}$ and $M_5$ transistors. And the keys given both A and B as '1' then $M_8$and $M_9$ are in ON condition then logic'0' results at EXCLUSIVE-OR and logic'1' at EXCUSIVE-NOR which suffers with swaying then $M_4$ and $M_6$ transistors are used for restitution loop. The logic A is taken by the stationary CMOS inverter. This intended EXCLUSIVE-OR and EXCUSIVE-NOR design gives reliable swaying result for all the inputs given. This is shown in Table (1)I.

## V. INTENDED 18T FULLADDER DESIGN USING A NOVEL 8T EXCLUSIVE-ORAND EXCUSIVE-NORDESIGN

This implemented Full adder circuit is designed by using 8T EXCLUSIVE-OR and EXCUSIVE-NOR circuit and additional eight more transistors. The designed Full adder logic has written in the below equation:

SUM = (A XOR B) ($C_{in}$ BAR) + (A XNOR B) $C_{in}$.

$C_{out}$ (carry out) = $C_{in}$ (A XOR B) + B(A XNOR B)

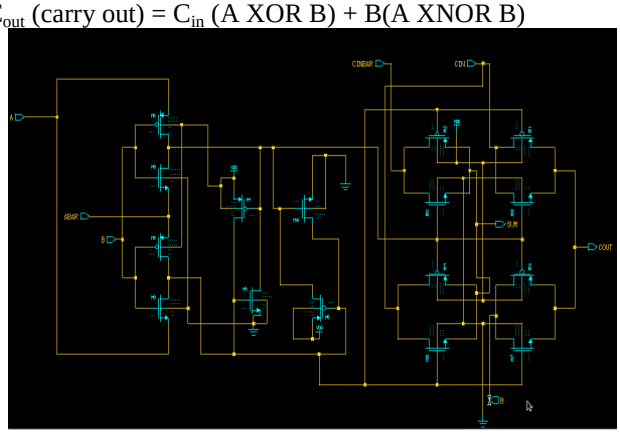


**Figure 3(a): Intended FULLADDER Design**

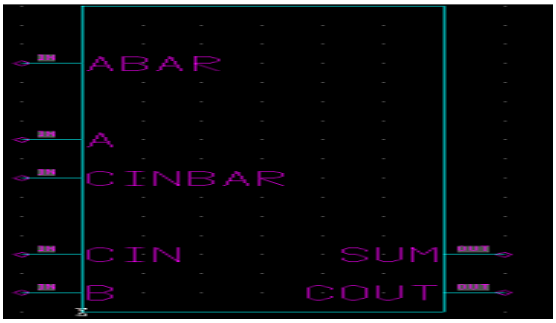


**Fig. 3(b): Intended FULLADDER Symbol**

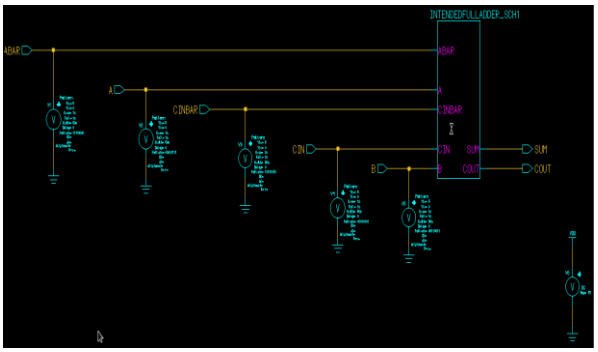

**Fig. 3(c): Simulated Schematic of Intended FULLADDER**

The Figure 3(b) represents the symbol for the Intended Full adder schematic and Figure 3(c) represents the simulated schematic of intended Full adder design. For attaining the total resultant voltage sway for SUM and $C_{out}$ resultants and additional transistors like $M_{11}$, $M_{12}$, M13, $M_{14}$, $M_{15}$, $M_{16}$, $M_{17}$ and $M_{18}$ are utilized. The result of SUM is attained by combining $M_{12}$, $M_{14}$, $M_{15}$ and $M_{16}$ additional gates to EXCLUSIVE-OR and EXCUSIVE-NOR design. The result of $C_{out}$ is attained by using $M_{11}$, $M_{13}$, $M_{17}$ and $M_{18}$ transistors are taken from EXCLUSIVE-OR and EXCUSIVE-NOR design. In this $M_{11}$, $M_{12}$, $M_{13}$ and $M_{14}$ are PMOS transistors and the SUM result for this design is illustrated as given below. If EXCLUSIVE-OR is'1' and EXCUSIVE-NOR is '0', then $M_9$ and $M_{10}$ gets ON and $M_{14}$ and $M_{15}$ gets OFF so the result attained for SUM is invert of $C_{in}$ ($C_{in}$BAR).For suppose if EXCLUSIVE-OR is'0' and EXCUSIVE-NOR is '1' .Then $M_{12}$ and $M_{16}$ gets OFF and $M_{14}$and $M_{15}$ gets ON then the result attained for SUM is $C_{in}$. Likewise for the carry out ($C_{out}$) the first case we have taken is EXCLUSIVE-OR as '1' and EXCUSIVE-NOR as'0' then $M_{12}$ and $M_{16}$ gets OFF and $M_{11}$and $M_{12}$ gets ON then the result attained for carry out ($C_{out}$) is carry in ($C_{in}$). For suppose if EXCLUSIVE-OR is'0' and EXCUSIVE-NOR is '1' then $M_{11}$ and $M_{18}$ gets OFF and $M_{13}$ and $M_{17}$ gets ON then the result attained for carry out($C_{out}$) is input B.

## VI. RESULTS

Figure (4) visualizes the pretend output of EXCLUSIVE-OR and EXCUSIVE-NOR design as revealed in previous Figure 1(a). The Figure (4) below shows that there is a output as logic'0' in bad condition for the keys A as'1' and B as'0' this problem gets overcome by the intended EXCLUSIVE-OR and EXCUSIVE-NOR design which is visualized in Figure 2(a) and the output waveforms are shown in Figure(5), while the Figure 6(a) visualizes the input-output waveform for the intended full adder design which is publicized in Figure 3(a).

And the attained outcome has voltage swing for any input logic applied. Figure 6(b) visualizes the input-output waveform of the Standard full adder design. So in this paper we considered the transistors utilized, delay, power wastage and Power Delay Product (PDP) of the EXCLUSIVE-OR and EXCUSIVE-NOR are designs visualized in Table (3). This Table visualizes the delay, power wastage and PDP of the intended EXCLUSIVE-OR and EXCUSIVE-NOR is design less significant than that existed EXCLUSIVE-OR and EXCUSIVE-NOR design. The Standard CMOS Full adder and the intended Full adder are differentiated in Table (4). Accordingly the Table (4) differentiates the parameters like transistors count, impediment, power wastage and PDP. These all parameters are reliable to intended Full adder design.

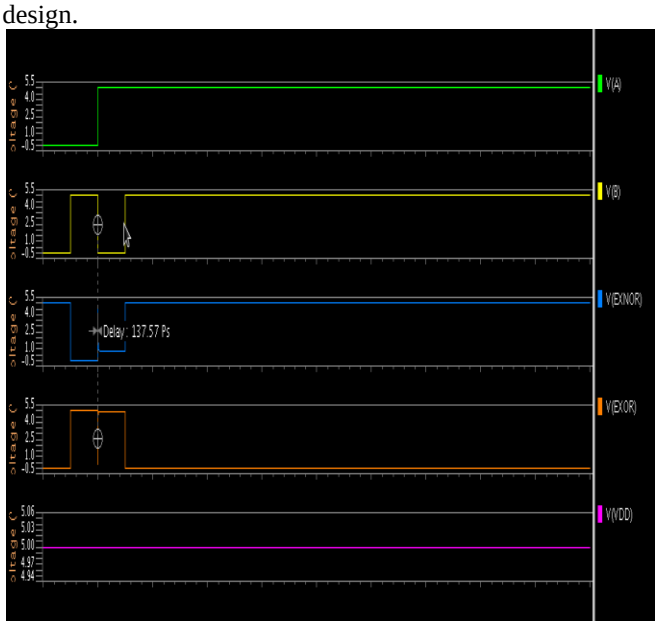


**Fig. 4: Transient outcome regarding Existed EXCLUSIVE-OR and EXCUSIVE-NOR (as shown if Figure 1(a))**

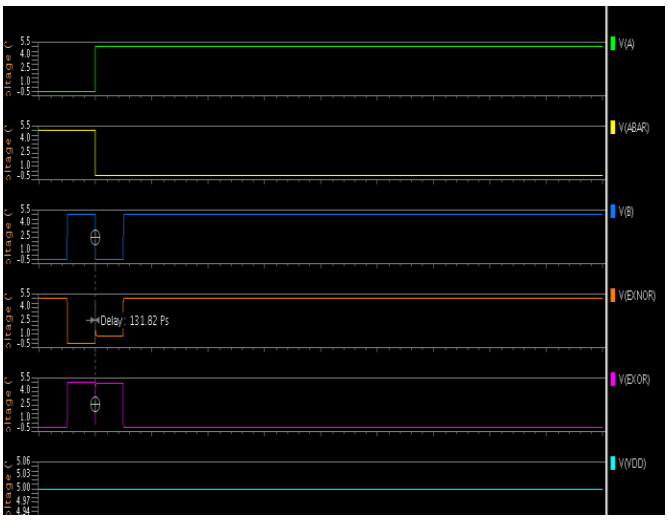


**Fig. 5: Transient outcome of Intended EXCLUSIVE-OR and EXCUSIVE-NOR(as shown if Figure 2(a))**

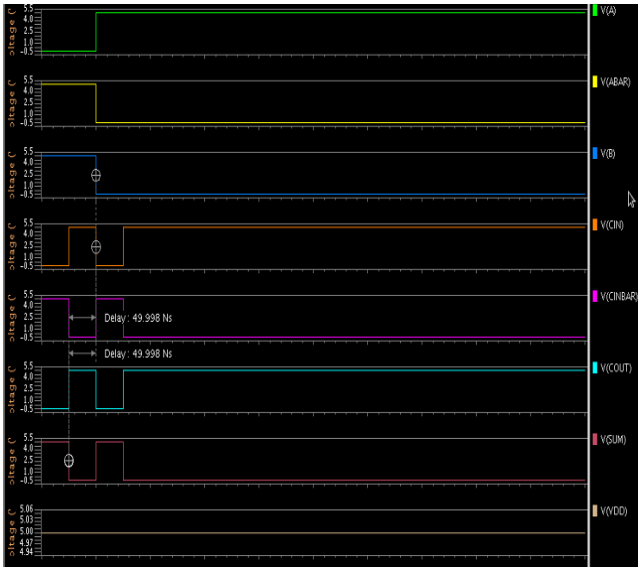


**Fig. 6 (a): Transient outcome regarding Intended FULLADDER (as shown if Figure 3(a))**

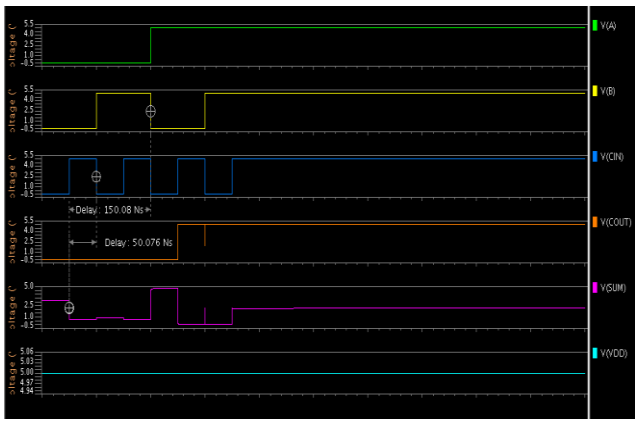


**Fig. 6 (b): Transient outcome regarding Standard CMOS FULLADDER**

Accordingly, the transient analysis of Intended Full adder design and Standard Full adder design are compared and those are visualized in Figure 6(a) and Figure 6(b). The transient characteristics of the existed and intended EXCLUSIVE-OR and EXCUSIVE-NOR design is illustrated and the intended Full adder is also illustrated. This is executed with 130nm expertise in MENTOR GRAPHICS tool.

**Table (3): Measurable Evaluation of EXCLUSIVE-OR and EXCUSIVE-NOR Design @ 5V**

| limitation | Existed EXCLUSIVE-OR and EXCLUSIVE-NOR | Existed EXCLUSIVE-OR and EXCLUSIVE-NOR |
|---|---|---|
| Transistor count | 10 | 10 |
| Delay (pS) | 137.57 | 131.82 |
| Power (nW) | 202.32 | 195.07 |
| Power Delay Product (aJ) | 27.83 | 25.71 |

**Table (4): Measurable Evaluation of Full adder Design @5V**

| limitation | Standard CMOS Full adder | Intended Full adder |
|---|---|---|
| Transistor count | 28 | 18 |
| Delay (nS) | 50.08 | 49.99 |
| Power (nW) | 1053.63 | 379.99 |
| Power Delay Product (fJ) | 52.76 | 18.99 |

## VII. CONCLUSION

This literature Session gives a novel EXCLUSIVE-OR and EXCUSIVE-NOR is circuit implemented to eliminate the voltage sway quandary in the previously implemented EXCLUSIVE-OR and EXCUSIVE-NOR design. An intended Full adder is designed with a novel intended EXCLUSIVE-OR and EXCUSIVE-NOR design. Taken from the attained outcome the intended EXCLUSIVE-OR and EXCUSIVE-NOR circuit as well as intended full adder design approaches good running potential, soaring rapidity and less power wastage . So, this can be utilized where there is a requirement of less area, high speed and good driving ability. The Existed EXCLUSIVE-OR and EXCUSIVE-NOR intend has Power Delay Product of 27.83 atto Joules. And the intended EXCLUSIVE-OR and EXCUSIVE-NOR devise has Power Delay Product of 25.71 atto Joules. While coming to the Full adder, the standard Full adder contains Power Delay Product of 52.76 femto Joules. And the intended Full adder contains Power Delay Product of 18.99 femto Joules.

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**Venkata Yashwanth Goduguluri,** received his B.Tech degree from Vignans Engineering college, Vadlamudi and M.tech from Sathyabama University, Chennai. And have 7 years of teaching experience as an Assistant professor in Various engineering colleges, currently working in KKR&KSR Institute of Technology and Sciences, Vinjanampadu, Guntur(D.t). Totally 3 publications are there in various journals Areas of interests are VLSI, Signal Processing, and Wireless Communication**.**