Design and Implementation of 802.15.4 Transceiver for Wireless Personal Area Networks (WPANs) on FPGA

Guruprasad S.P, Chandrasekar B.S

Abstract*: The IEEE 802.15.4 standard provides mainly accessing, monitoring, and controlling capability of the Wireless devices. This standard supports short-range wireless communications and Low Rate (LR) - Wireless Personal Area Networks (WPANs). This manuscript presents the fully integrated digital 802.15.4 Transceiver, which suitable to ZigBee Device Standard at 2.4GHz range. The 802.15.4 Transceiver design includes an 8-bit input data sequence mapped to lower and Upper Symbols followed by Chip-sequence conversion as per the IEEE standard. The chip sequences are mapped separately as even and odd sequences used for the Offset-QPSK Modulation. The chip synchronization achieved by using a proper clocking mechanism on the receiver side. The 802.15.4 Transceiver design is implemented on Artix-7 FPGA using Xilinx Environment. The hardware constraints like Area (Slices), Frequency, and Power are analyzed. The proposed work also compared with existing similar approaches with more significant improvements in chip area and Power.

Keywords: FPGA, IEEE 802.15.4, O-QPSK, Transceiver, WPANs, ZigBee Device,

I. INTRODUCTION

Wireless PANs play a significant role in short-range wireless communications, especially for Internet of Things (IoT) devices. Different wireless standards are available like IEEE 802.15.1 (Bluetooth), IEEE 802.11 (Wi-Fi), IEEE 802.15.4 for ZigBee, and many more. These wireless standards work at different frequency ranges and for different applications. Nowadays, these wireless standards are adopted in IoT environments for different applications like Home automation, Smart city, medical care, industrial control systems, and agriculture field [1-2]. The wireless standards have different bandwidth requirements based on the applications. The larger bandwidth consumes more network constraints and more power utilization.

The low-cost, small size wireless devices, low power consumption devices are commonly known as Low Rate (LR)-WPANs as per IEEE 802.15.4 standard. This standard supports a low data rate (250Kbps) for several diverse applications and best suited to wireless sensor nodes (WSNs). The Physical (PHY) layer and Medium access control (MAC) layer defined by the IEEE 802.15.4 standard as lower layers.

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Similarly, the Application layer and Network layer along with security are defined by the ZigBee Alliance as upper layers for the formation of ZigBee Stack [1][3-4] and represented in Figure 1. The application layer provides complete functionality of the device, and the network layer provides configuration, routing, and network manipulation information. These Upper Layers are connected through

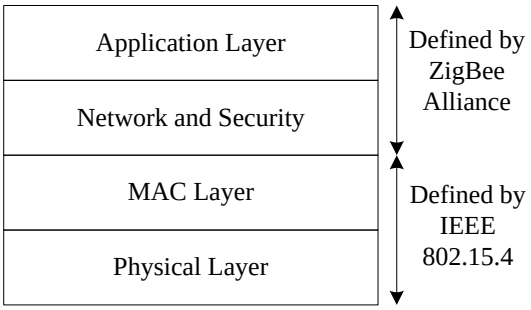

Fig. 1.ZigBee Stack

IEEE 802.2 logic link Controller (LLC) for accessing the lower layers like MAC and PHY Layer. The Physical layer provides data and management services. The data services provide the transmission and reception of the PHY protocol data unit (PPDU) through a radio channel. The channel supports 868 MHz, 915MHz, and 2400MHz unlicensed bands. The MAC layer also provides data and management services across PHY data. The MAC layer supports Carrier sense and collision detection mechanisms to improve successful packet delivery.

The 802.15.4 standard supports Direct sequence (DS) spreading mechanism along with Offset QQPSK for Modulation with half sine-pulse shaping for 2.4GHz for low-cost implementation and high performance [5-6]. The ZigBee- Alliance and IEEE 802.15.4 group are integrated for the new network modules for a Short-range of frequencies with different applications like home, industrial, medical, and also in MANET, VANET applications [7-8].

In this manuscript, the 802.15.4 transceiver architecture is designed and implemented on Artix-7 FPGA with prototyping. This 802.15.4 architecture is suitable for the ZigBee device as part of Wireless–PAN applications. Section II describes the present works related to 802.15.4 architectures for ZigBee devices and other devices using different modulation techniques and also for other applications. The proposed

802.15.4 Transceiver hardware architecture is presented in section III. Section IV explains the results and discussion, along with a comparison with existing approaches. Finally, it concludes the overall work with improvements along with future scope in section V.

II. RELATED WORKS

This section elaborates on the existing 802.15.4 approaches for different applications with research findings. Elmiligi et al. [9] present the Binary PSK modem in physical layer IEEE 802.15.4 for ZigBee devices under the 868 MHz band. The BPSK modem designed using multiplier less architecture to improve the chip area. The BPSK demodulator designed using carrier recovery with a symbol synchronization unit for decision the binary data. Jalalifar et al. [10] present the Quadrature Voltage controller Oscillator (Q-VCO) design for 802.15.4 architectures with ultra-low power utilization. This module works at 2.4 GHz- band and supports the ISM band. The complete module is designed under 0.13µm CMOS technology. The Q-VCO eliminates the disturbances using indicators and noise filtering with better phase noise.

FPGA based ZigBee baseband modem designed by muni et al. [11] as per IEEE 802.15.4 standard. The design includes a transmitter with half-sine pulse shaping along with Receiver. The even and odd sample detection generates the In-phase and Quadrature phase, with addition followed by the chip to symbol mapping for the last output generation. The design consumes a larger chip area along with more power utilization. The Digital ZigBee Receiver for 2.4 GHz applications is presented by Ahmad et al. [12] on the FPGA Platform. The Receiver uses the Direct-sequence spread spectrum (DSSS) technique with O-QPSK demodulator for the chip to symbol to bit Mapping with chip synchronization and dispreading. The simulation results mean established hardware and suitable for real-time scenarios.

The 2.4 GHz ZigBee modem is presented by Gil et al. [13] for healthcare and biomedical applications using the 90nm- CMOS platform. The complete modem integrated into SoC implementation. The modem is analyzed using a spectrum analyzer for transmitter and receiver output signals, along with the Interface rejection ratio by concerning the Frequency. Wang et al. [14] present the Wireless ECG acquisition SoC for ZigBee applications, which includes ECG acquisition node, transmitter – Baseband, RF transmitter followed by RF receiver, Receiver-baseband with ECG display monitoring unit. The ZigBee baseband transmitter and Receiver works based 802.15.4 standard. Supare et al. [15] presented the Digital QAM based ZigBee modem design using HDL. They implemented on FPGA, which includes FIR filter, SIPO-PISO converters, up-down samplers, and Chip encoder-decoders. The wireless channel CC2500 module used receiving and transmitting the Channel packets. Oliveira et al. [16] present the Multi-regional (MR)-FSK modem for Smart Metering Utility Networks (SUN) applications. The modem is implemented and analyzed in both FPGA and 65-nm ASIC for resource analysis. The design is suitable for 802.15.4g IEEE standards.

Gomes et al. [17] present the Customizable and trustable End device (CUTE) for IoT applications, which includes heterogeneous architecture with the combination of a microcontroller unit (MCU) and reconfigurable computing unit (RCU). The design supports for low-end devices with fast FPGA accelerators along with IoT operating system. The Gomes et al. [18] present the 6LoWPAN accelerators for IoT devices, which include filters with IPv6, accelerator interface with 802.15.4 frame buffer, and logic unit, followed by Bus interface with ARM Cortex-M3 (IoT Stack. This designs support DoS and handling data securities in

6LoWPAN with detailed thread evaluation. Nain et al. [19] present the IEEE 802.15.4 modem with secure-phase encryption using the RC4 algorithm. The phase encryption and decryption, along with the key generation of RC4, works at the 1Mbps data rate. The frame synchronization and detection unit work-based clock scheduling algorithm with a secure header generator. The design analyzes the force search attack, along with integrity, data freshness, traffic analysis attack, and energy depletion attacks. Zolfaghari et al. [20] present the multi-mode W-PAN SoC for IoT devices on the 40-nm CMOS platform. The multi-mode includes Bluetooth, IEEE 802.15.4, and Bluetooth low energy (BLE) as a W-PAN device used in low power IoT applications. The work analyzes the TX-constellation and spectrum for the Enhanced data rate (EDR). The IEEE 802.15.4 based MAC layer is presented by Rajesh et al. [21], which is the combination of hardware and software approaches, which includes ZigBee Stack layers and Tiny OS-components. The MAC- layer has carrier sense and collision signals along with frame check sequence using CRC for error control.

Most of the existing approaches are designed using CMOS- technology rather than the FPGA platform for most of the W-PAN applications. Very few FPGA implementations are presented for the 802.15.4 transceiver model with a lack of resource constraints problems. The proposed model overcomes the drawbacks of the above problems with optimized solutions.

III. 802.15.4 TRANSCEIVER MODULE

The IEEE 802.15.4 Transceiver works at an operating frequency of 2.4 GHz, and the data rate is fixed to 250Kbps along with a chip rate of 2Mbps. Direct Sequence (DS) is used as a Spread spectrum (SS) analysis with the help of Offset-Quadrature Phase shift keying (O-QPSK) modulation. The IEEE 802.15.4 Transceiver is suitable for ZigBee devices and works at low Rate (LR)-WPANs. The complete 802.15.4 Transceiver architecture is represented in Figure 2. It mainly contains bits to symbols (B2S) and Symbol to bits (S2B) mapping, Symbols to chips (S2C), and chips to Symbols (C2S) conversion, Even-odd Mapping (EOM) and inverse EOM, O-QPSK Modulation and demodulation. The IEEE 802.15.4 Transceiver has transmitter and receiver modules along with the channel.

A. Transmitter Module

The 802.15.4 transmitter module mainly contains bits to symbols (B2S) Mapping, Symbols to chips (S2C) conversion, Even-odd Mapping (EOM), and O-QPSK Modulation. The input bits are 8-bit at 250 Kbps data rate and are in the form of either ‘0’ or ‘1’. The B2S Mapping, map these 8-bit inputs into two parts for symbols creation. The LSB side input bits [3:0] are lower Symbol ($S_3S_2S_1S_0$), and MSB side input bits [7:4] are upper Symbol

($S_7S_6S_5S_4$) are represented in Figure 3. The 4-bits are represented as 1 symbol as per IEEE standards. The Symbol to chip (S2C) conversion will perform based on DS-SS baseband modulation to reduce the loss of baseband in the transmitter. The 4-bit (1-symbol) are mapped to a 32-random sequence or (PN) data sequence as per Table I.

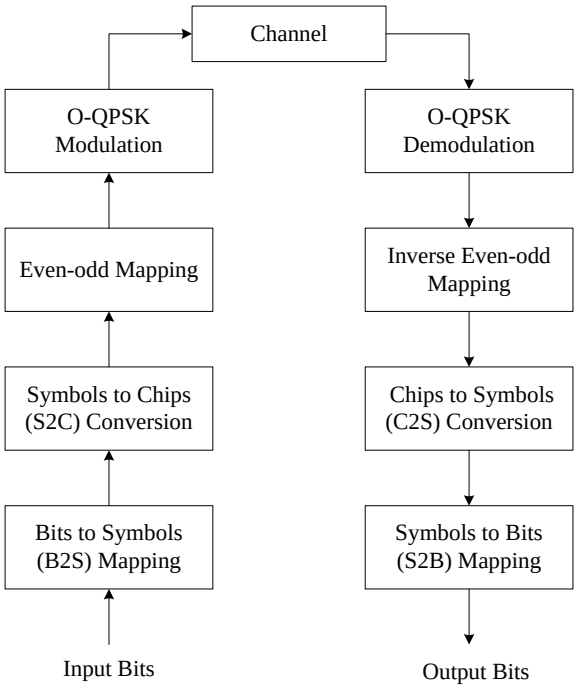

Fig. 2.Block diagram of 802.15.4 Transceiver

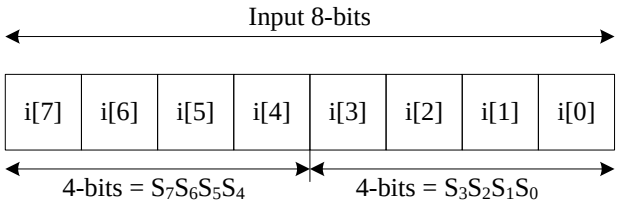

Fig. 3.B2S Mapping

Table I: Symbols to Chip sequence conversion Table

Symbols	Chip Sequence	Symbols	Chip Sequence
0000	D9C3522E	1000	8C96077B
0001	ED9C3522	1001	B8C96077
0010	2ED9C352	1010	7B8C9607
0011	22ED9C35	1011	77B8C960
0100	522ED9C3	1100	77B8C96
0101	3522ED9C	1101	6077B8C9
0110	C3522ED9	1110	F00BF8E
0111	9C3522ED	1111	14233F2C

The 4-bit supports up to 16 different chip sequences of 32-bit data as represented in Table I. The chips rate is at 2 Mbps for the data conversion. The 4-bit symbol value is replaced with corresponding 32-bit chip sequence data. The 32-bit chip sequence is in the form of unipolar and converts to the bi-polar sequence. The even and odd chip sequence bits have separated by using EOM to process the Modulation. The even- chip sequence C_0, C_2, C_4... C_{30} and odd chip sequence C_1, C_3, C_5... C_{31} are concatenated separately to form 16-bit sequence as a modulated data. The even sequences used for an In-phase and odd-chip sequence used for Quadrature phase data for O-QPSK Modulation.

The O-QPSK Modulation is an offset form of QPSK modulation, and it generates the In-phase and quadrature-phase data using even and odd data sequences. The Carrier signals are generates using Digital frequency synthesizer (DFS). The two DFS modules are used for the generation of the sine and cosine signals as carrier data, which are multiplied with even and odd data sequences for the formation of In-phase and quadrature-phase Modulation. The quadrature-phase data is delayed by the 2-bit period than the In-phase data for the offset formation. The In-phase and quadrature-phase data are added for the formation of 802.15.4 modulated data. The channel receives the modulation data and adds noisy bits and generates the corrupted data to the Receiver.

B. Receiver Module

The Receiver 802.15.4 module has the inverse process of the transmitter module. It mainly contains O-QPSK demodulation, Inverse EOM, chips to Symbols (C2S) conversion, and symbols to Bits (S2B) mapping. The corrupted data received by the Receiver and sends for O-QPSK demodulation. First, it divides in-phase and quadrature-phase data for Modulation. The carrier signal data are generated by using DFS for the sine and cosine generation and are multiplied with in-phase and quadrature-phase data. The demodulated data generates Even and odd data signals for Inverse EOM. The inverse EOM concatenates the 16-bit even and odd sequences one after that serially for the generation of even and odd chip sequences. The de-spreading chip sequences are synchronized using the proper clocking mechanism.

The Chip to symbols (C2S) conversion performs separately for the even and odd chip sequences, for symbols creation at 2Mbps chip rate. The two 4-bits symbols are used for the formation of 8-bit recovered data bits at 250Kbps using Symbols to Bits (S2B) Mapping.

The 802.15.4 Transceiver is digital transceiver architecture and performs the data bits transaction at 2.4GHz as per IEEE standards. The proposed 802.15.4 transceiver architecture suitable for LR-WPANs applications, and it meets the ZigBee Device standard specifications. The design is also applicable to any short-range wireless communication system for data transmission.

IV. RESULTS AND DISCUSSION

The 802.15.4 Transceiver module is designed and implemented on Atrix-7 FPGA with prototyping. The Verilog-HDL is used on Xilinx–ISE Environment for synthesis, and Modelsim 6.5f Simulation is used for simulation analysis. The hardware constraints like area, Time, and Power are analyzed. The transceiver module includes both transmitter and receiver

modules that are synthesized and implemented on Artix-7 FPGA, and its resource utilization is tabulated in Table II. A graphical representation is shown in Figure 4. The Transceiver module utilizes 224 slice registers, 428 Slice-LUTs, and 179 LUT-FF pairs as a chip area in Artix-7. The 802.15.4 Transceiver module works at 270.1 MHz operating Frequency with a minimum period of 3.64 ns.

Table-II: Resource utilization of 802.15.4 Transceiver on Artix-7 FPGA

Resources	Transmitter	Receiver	Transceiver
Chip Area (on Artix-7)			
Slice Registers	164	109	224
Slice LUTs	264	193	428
LUT-FF pairs	122	69	179
Time			
Minimum Time (ns)	3.742	2.899	3.64
Max.Frequency (MHz)	267.247	344.994	270.1
Power			
Dynamic Power (W)	0.05	0.039	0.089
Total Power (W)	0.132	0.121	0.171

The power utilization is analyzed using the X-Power analyzer at a fixed clock frequency of 100MHz. The 802.15.4 Transceiver consumes 0.171W total Power, which includes 0.089W dynamic power and 0.82W static Power.

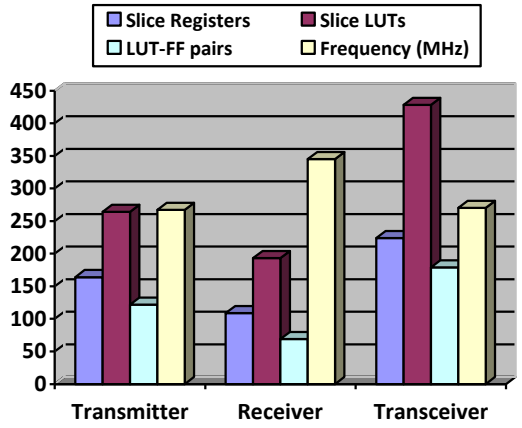

Fig. 4.Graphical representation of Transceiver Module for Chip Resources on Artix-7 FPGA

The transmitter and receiver resource utilization also tabulated. The 802.15.4 Transceiver utilizes fewer resources around 1% of chip area (slices) in Artix-7 and works at a high speed of 270.1 MHz and consumes less Power of 0.171W. These hardware constraints are suitable for wireless-PAN applications in real-time scenarios.

The proposed 802.15.4 Module is compared with similar existing approaches with improvements, and it is tabulated in Table III. The proposed work is compared with Ref [11] with the same O-QPSK Modulation, and for Zigbee applications, around 76% slice registers and 64% slice LUT's chip area overhead along with 21% total power improvements. Similarly, The Ref [16] uses the Cyclone FPGA device and uses the Multi-regional Frequency Shift-keying (MR-FSR) modulation technique for Smart Metering Utility Networks (SUN) applications. The Ref [16] utilizes more chip area and Power than the proposed work.

Table-III: Comparative Analysis of proposed work with recent works

Resources	Proposed	Ref [11]	Ref [16]
Device	Artix-7	Virtex-5	Cyclone-V
Modulation	O-QPSK	O-QPSK	MR-FSK
Applications	Zigbee	Zigbee	SUN
Slice Registers	224	973	3251
Slice LUTs	428	1179	2218
BUFG/BUFGCTRLs	1	10	NA
Total Power (mW)	0.171	0.216	0.439

V. CONCLUSION AND FUTURE WORK

The Fully integrated 802.15.4 Transceiver architecture is designed in this manuscript. The design is implemented on Artix-7 FPGA with prototyping. The 802.15.4 Transceiver Meets the ZigBee device IEEE Standards. The 802.15.4 Transceiver supports Low-Rate WPANs applications along with short-range wireless communication devices. The 802.15.4 Transceiver hardware constraints include Area, Time, and Power are tabulated. The Complete design works at 270.1MHz on Artix-7 FPGA. The present work is compared with existing similar approaches with significant improvement in Chip area and Power. In the future, a suitable security algorithm is incorporated to 802.15.4 Transceiver to improve the security and privacy of LR-WPANs devices.

REFERENCES

1. IEEE 802 Working Group: IEEE Standard for Local and Metropolitan Area Networks—Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs).IEEE Std, vol. 802, 4-2011.
2. Perez, J. J., J. Pelegri, and A. Menendez. "Preamble sampling MAC protocol for low power wireless sensor networks with IEEE 802.15. 4. Transceivers." In 2006 IEEE Instrumentation and Measurement Technology Conference Proceedings, pp. 1543-1546. IEEE, 2006.
3. Wang, Chua-Chin, Chi-Chun Huang, Jian-Ming Huang, Chih-Yi Chang, and Chih-Peng Li. "ZigBee 868/915-MHz modulator/demodulator for wireless personal area network." IEEE Transactions on very large scale integration (VLSI) systems 16, no. 7 (2008): 936-939.
4. Pešović, Uroš, Dušan Gliech, Peter Planinšič, Zoran Stamenkovic, and Siniša Ranđić. "Implementation of IEEE 802.15. 4 transceiver on software defined radio platform." In 2012 20th Telecommunications Forum (TELFOR), pp. 376-379. IEEE, 2012.
5. Yin, Shouyi, Jianwei Cui, Ao Luo, Leibo Liu, and Shaojun Wei. "A high efficient baseband transceiver for IEEE 802.15. 4 LR-WPAN systems." In 2011 9th IEEE International Conference on ASIC, pp. 224-227. IEEE, 2011.
6. Ahmad, Rafidah, Othman Sidek, Wan Mohd Hafizi Wan Hassin, and Shukri Korakkottil Kunhi Mohd. "Implementation of IEEE 802.15. 4-based OQPSK-pulse-shaping block on FPGA." In 2011 IEEE International Conference on Computer Applications and Industrial Electronics (ICCAIE), pp. 459-464. IEEE, 2011.
7. Wang, Sishan, Airong Huang, and Tao Zhang. "Performance Evaluation of IEEE 802.15. 4 for V2V Communication in VANET." In 2013 International Conference on Computational and Information Sciences, pp. 1603-1606. IEEE, 2013.
8. Cho, Hyuntae, Hyunsung Jang, and Yunju Baek. "Multi-phase correlator-based realistic clock synchronization for IEEE 802.15. 4 networks." Telecommunication Systems 55, no. 3 (2014): 377-386.

9. Elmiligi, Haytham, M. Watheq El-Kharashi, and Fayez Gebal. "Design and implementation of BPSK MODEM for IEEE 802.15. 4/ZigBee devices." In 2016 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE), pp. 1-5. IEEE, 2016.
10. Jalalifar, M., and G-S. Byun. "Ultra-low-power quadrature VCO for 2.4 GHz-band IEEE 802.15. 4 standard." Electronics Letters 50, no. 16 (2014): 1168-1169.
11. Muni, Bijaya Kumar, and Sarat Kumar Patra. "FPGA implementation of ZigBee baseband transceiver system for IEEE 802.15. 4." In International Conference on Advances in Computing, Communication and Control, pp. 465-474. Springer, Berlin, Heidelberg, 2013.
12. Ahmad, Rafidah, Othman Sidek, and Shukri Korakkottil Kunhi Mohd. "Implementation of a verilog-based digital receiver for 2.4 GHz Zigbee applications on FPGA." Journal of Engineering Science and Technology 9, no. 1 (2014): 136-153.
13. Gil, Joonho, Ji-Hoon Kim, Chun Suk Kim, Chulhyun Park, Jungsu Park, Hyejin Park, Hyeji Lee et al. "A fully integrated low-power high-coexistence 2.4-GHz ZigBee transceiver for biomedical and healthcare applications." IEEE transactions on microwave theory and techniques 62, no. 9 (2014): 1879-1889.
14. Wang, Liang-Hung, Tsung-Yen Chen, Kuang-Hao Lin, Qiang Fang, and Shuenn-Yuh Lee. "Implementation of a wireless ECG acquisition SoC for IEEE 802.15. 4 (ZigBee) applications." IEEE journal of biomedical and health informatics 19, no. 1 (2014): 247-255.
15. Supare, Vivek P., Bharati B. Sayankar, and Pankaj Agrawal. "Design & implementation of MQAM based IEEE 802.15. 4/ZigBee Tranceiver using HDL." In 2015 International Conference on Smart Technologies and Management for Computing, Communication, Controls, Energy and Materials (ICSTM), pp. 455-458. IEEE, 2015.
16. de Oliveira, Jessica AJ, Augusto FR Queiroz, Eduardo R. de Lima, and J. Mertes. "An MR-FSK transceiver compliant to IEEE802. 15.4 g for smart metering utility applications: FPGA implementation and ASIC resource estimation." In 2015 7th IEEE Latin-American Conference on Communications (LATINCOM), pp. 1-4. IEEE, 2015.
17. Gomes, Tiago, Filipe Salgado, Adriano Tavares, and Jorge Cabral. "CUTE Mote, A Customizable and Trustable End-Device for the Internet of Things." IEEE Sensors Journal 17, no. 20 (2017): 6816-6824.
18. Gomes, Tiago, Filipe Salgado, Sandro Pinto, Jorge Cabral, and Adriano Tavares. "A 6LoWPAN accelerator for Internet of Things endpoint devices." IEEE Internet of Things Journal 5, no. 1 (2017): 371-377.
19. Nain, Ajay Kumar, Jagadish Bandaru, Mohammed Abdullah Zubair, and Rajalakshmi Pachamuthu. "A secure phase-encrypted IEEE 802.15. 4 transceiver design." IEEE Transactions on Computers 66, no. 8 (2017): 1421-1427.
20. Zolfaghari, Alireza, Mohamed El Said, Michael Youssef, Gang Zhang, Tom Tong Liu, Federico Cattivelli, Yannis Ioannis Syllaios et al. "A multi-mode WPAN (Bluetooth, BLE, IEEE 802.15. 4) SoC for low-power and IoT applications." In 2017 Symposium on VLSI Circuits, pp. C74-C75. IEEE, 2017.
21. Rajesh, Ammu Lakshmy, Sanket V. Kadam, and Rajendra Patrikar. "A Complete Hardware Advent on IEEE 802.15. 4 Based Mac Layer and a Comparison with Open-ZB." In International Symposium on VLSI Design and Test, pp. 682-694. Springer, Singapore, 2018.