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Fixed off Time Based Power-Factor Correction for AC-DC Converter

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Abstract: ***The conversion of A.C to D.C determines the distortion of the mains current A.C., which degrades the input power factor. The main reason for a poor power factor is the non-linear nature of the circuit. In this paper power factor is improved by using a basic boost converter and a control technique based on the fixed off time(FOT) approach .The traditional approach to the correction of the power factor in the boost converter is the continuous conduction mode with fixed frequency (FF-CCM) and the transition mode (TM) PWM (fixed connection time, variable frequency). In the first mode, the inductor operates in continuous conduction mode (CCM) and uses the average current-mode control mode; a complex technique involves a considerable number of components. The second method uses the more complex control technique of the peak current mode that makes the inductor work between continuous and discontinuous mode, which uses fewer components, unstable greater than 50% duty cycle and is more cost efficient. A third approach, the fixed off time (FOT) is gaining popularity which is conditionally stable for a duty cycle of over 50% and does not need compensation. The paper work carried out to use the power factor correction (PFC) based on DC-DC Flyback converter. To verify the design and operation of the circuit, the simulation is performed in PSIM .A prototype is developed and results are presented.***

Keywords: -Fixed-Frequency continuous conduction mode (FF-CCM), Transition mode (TM), Fixed OFF Time (FOT), Power factor correction (PFC)

I. INTRODUCTION

Power factor correction (PFC) circuit is used to shape the input current based on the rectified half sinusoid voltage sensed at the output of bridge rectifier. The PFC circuit helps in maximizing the amount of real power drawn from ac mains and to minimize the harmonic stress caused by current harmonics on AC system .The electrical equipment connected to the ac mains circuit should exhibit pure resistor behaviour ,but due to the non linear nature of equipment connected with the AC mains the current drawn from the AC mains is not exact replica of AC voltage as some amount deviation in terms of phase difference is present between input voltage and current. Thus, PFC is needed to achieve the near unity power factor which in turn will help in mitigation of input current harmonics.

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There are various drawbacks associated with poor power factor such as High input current harmonics, Low rectifier efficiency due to the large value of rms current I, Distortion in the input AC voltage because of the peak currents. Without PFC, input power factor at the input side is found as 0.6 and requires large inductor for high input power factor[1].One of the other reason of adopting the PFC circuit is to follow the international standards like IEC 61000-3-2. The harmonics present in the ac line current has to be removed to meet the international standards. The work of standardization starts in early 1982.The standard IEC 555-2 was published by International Electro technical committee(IEC) which was later adopted by 1987 as the European standard EN 60555-2 by European Committee for Electro technical Standardization (CENELEC).IEC 555-2 standard was later replaced in 1995 by the IEC 1000-3-2 standard and subsequently adopted by CENELEC as the European standard EN i61000-3-2.The standard is applied to equipment with 16A RMS per phase and which is connected to the 50Hz, single-phase or 400V three-phase mains network [2-3]. Harmonic limit for different classes are presented in [4]. In paper [3-4], the harmonic present in the AC line current is removed to meet international standards, such as IEC 6100-3-2.The standard applies to equipment with 16A RMS per phase connected to the 50 Hz three-phase network, single-phase or 400V.The equipment is classified into four groups, Class A, Class B, Class C and Class D. [5], peak current and average current control are used to model the current of the input power grid. The peak current is unstable for the duty cycle above 50%. In the peak current control, the inductor operates in continuous conduction mode (CCM). The control of the average current mode is unconditionally stable for duty cycles exceeding 50%. [6] Presents the advantages and limitations of the boost and buck converter. [7], proposes a small signal model for controlling the current mode of PWM converters (pulse width modulation) with constant on time, constant off-time control of and discontinuous conduction mode. Peak current mode control when used with the Fixed on Time or Fixed Off time becomes unconditionally stable. [8] Used the Fix Off Time concept to couple the simplicity and affordability of the Transition (TM) mode with high current capacity of the Fixed-Frequency continuous mode resulting in peak current mode control with fixed OFF time (FOT control). Switch-off time (FOT control). In the proposed technique, the switch-on time is modulated maintaining the switch-off time constant, which results in a large change in switching frequency. [9], the FOT technique is further modified. The change associated with the switching frequency is eliminated by modulating the switch-off time proportional to the voltage of the input line, which results in a constant switching frequency,

unless the converter works in CCM mode. [10], Proposes an adaptive on- time control system for DC-DC converters. The proposed technique can achieve rapid transient response without any change in switching frequency. The author has made the switching frequency fs ($f_s = \frac{1}{R_a C_a}$), regardless of the input voltage Vin and the output voltage, Vout can be easily evaluated by the passive components Ra and Ca. In paper [11], the author used bridgeless PFC based on the Fixed Off Time with zero voltage switching, which leads to the reduction of conduction loss. A yield increase of 2.7% is reported. [12], presents a monolithic fixed frequency DC-DC boost converter with a modified adaptive off time control (MAOF).

II. PROPOSED METHODOLOGY FOR POWER FACTOR CORRECTION

Power factor is defined as the ratio of real power (P) to apparent power(S) i.e.

$$cos\theta = \frac{\boldsymbol{Realpower\ i(Watt)}}{\boldsymbol{ApparentPower(VA)}} \quad (1)$$

Where Real power or true power is the actual measurement of amount of power used and is represented in watts while, Apparent Power is combination of Real power and Reactive ipower (measured in Volt-Amps-Reactive) and is represented in Volt-Amps (VA).Power factor gives the degree of utilisation of real power from the available power.The above definition of power factor is legitimate only if voltage and current are having similar shape i.e. sinusoidal which is possible only for linear loads (load which takes current proportionally to the voltage applied).
The input circuit of Switch mode power supply presents non linear load to ac mains. The input ac is given to the bridge rectifier, a capacitor is connected across the capacitor which maintains the voltage proportional to peak of ac input voltage as shown in Fig.1

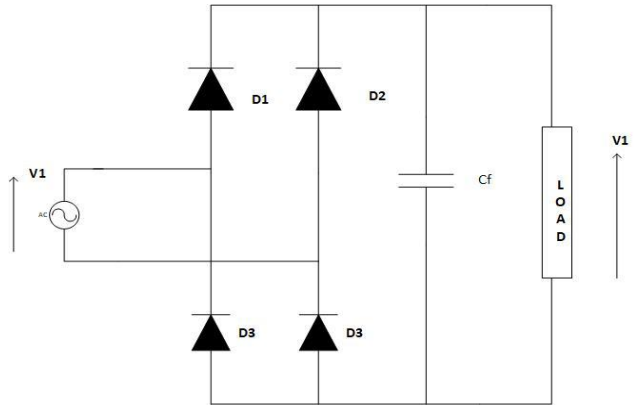


Fig. 1: Diode Bridge Rectifier

During each peak of ac input the capacitor gets charged.Thus, current is drawn only when the peak of input waveform and the pulse of current is large enough to sustain the load at the output till the next peak of waveform.It achieves that by dumping a large amount of charge in short interval of time.The duration of the current pulse is only 10% to 20% but the amplitude of current pulse is 5 ito 10 times the average current.The phenomenon is illustrated in Fig.2.

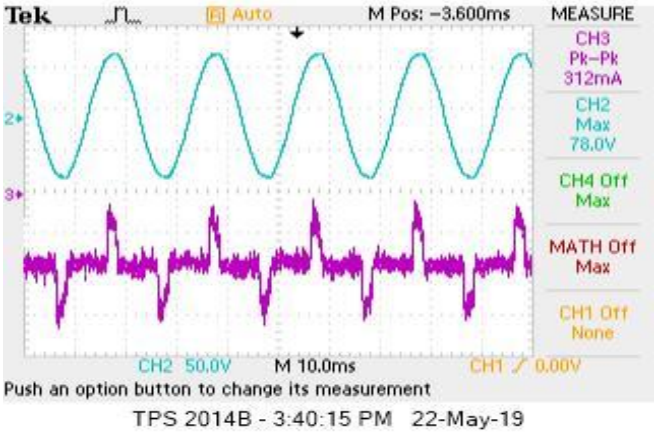
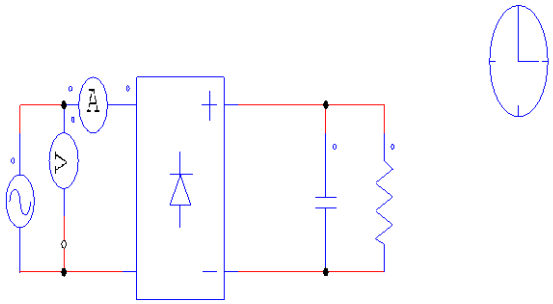
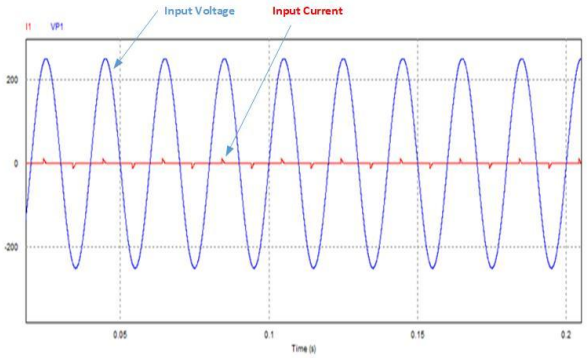


Fig. 2: Input current and voltage waveform of AC-DC converter without PFC

The duration of the current pulse taken from the AC grid is only 10% - 20%, but the amplitude of the current is 5 to 10 times the average current.The Fig.2 illustrates in phase current and voltage irrespective of severe distortion present in input side current. Fig. 3 shows the stimulated schematic and result. The input power factor of circuit is 0.4.



(a)



(b)

Fig,3:Simulation of bridge rectifier without PFC (a) Schematic (b) Input line voltage and Input line current with Vin=220V, R=500Ω and C =470µF

If the above definition of power factor is applied it would result in unity power factor so the above definition cannot be used everywhere. The definition of power factor is modified incase of non linear loads is termed as

$$pf = \frac{Vrms1}{Vrms}\frac{I_{rms1}}{I_{rms}}cos\theta \quad (2)$$

$$= \frac{I_{rms1}}{I_{rms}}cos\theta$$

$$= Kp * cos\theta$$

Where $Vrms1$:Fundamental component of voltage
I_{rms1}: Fundamental component of current

$cos\theta$: Displacement factor

θ =Phase angle between voltage and current

Kp $= \frac{I_{rms1}}{I_{rms}} = \frac{I_{rms1}}{\sqrt{I^2rms1+I^2rms2+I^2rms3+\cdots..+I^2nrms}}$ is the purity or distortion factor defined as the harmonic content of the current with respect to fundamental component of current.

Total harmonic distortion THD is defined as

$$\text{THD (\%)} = \frac{\sqrt{I^2rms1+I^2rms2+I^2rms3+\cdots..+I^2nrms}}{I^2rms1} \quad (3)$$

Hence

$$\text{Kp} = \sqrt{\frac{1}{1+(THD\ \%)^2}} \quad (4)$$

Thus, power factor and harmonic reduction are inter-related. The low harmonic content results in high power factor. For e.g. in AC-DC converter the displacement factor is usually unity. Thus power factor correction is usually the reduction of harmonic content .The reason for low power factor and high circulating currents generated by switch mode power supply is the discontinuous valued input filter charging current. The problem can be solved by increasing the conduction angle of rectifier circuit. There are two types of power factor correction, Passive and active power factor correction..In passive power factor correction, capacitor and inductors are iused.These are positioned at different location to improve the power factor.Simplest one is usage of inductor at the input side of bridge rectifier as shown in Fig.4 .The input power factor is 0.73 as simulated in PSIM i9.0.The advantages of passive power factor correction are simplicity in circuit design,reliable and efficient.But it has issues like bulky filter requirement,insufficient dynamic response, load dependent input current and poor voltage regulation below 200 watt design.Active ipower factor correction includes the shaping of input current using MOSFET and IGBT.Here the PFC stage is realised by using a bridge rectifier and DC-DC converter.To shape the input current any DC-DC converter can be used .It has advantages like low harmonic content in the input current,attains power factor greater then 0.95,small in size,more flexible and better control.Boost converter is shown in Fig.5.It is the most common topology used for power factor correction circuits. Here the output voltage is more than the input voltage. It operates in the continuous conduction mode (CCM) and Discontinuous conduction mode (DCM).

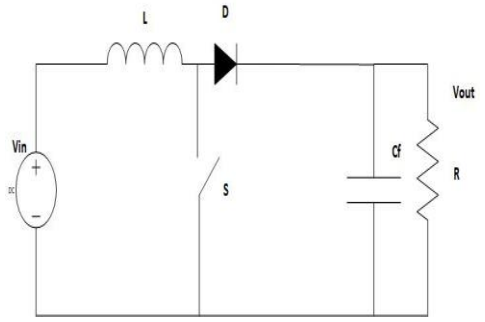


Fig 4 : Basic Boost converter topology

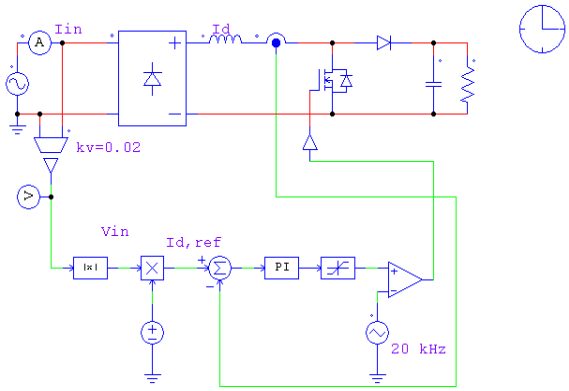


Fig 5: Boost PFC circuit- Schematic

The boost converter has inbuilt PFC property. The control technique used is simple PI controller. The controller output is compared with a high frequency triangular signal to generate PWM pulse is shown in Fig.6.

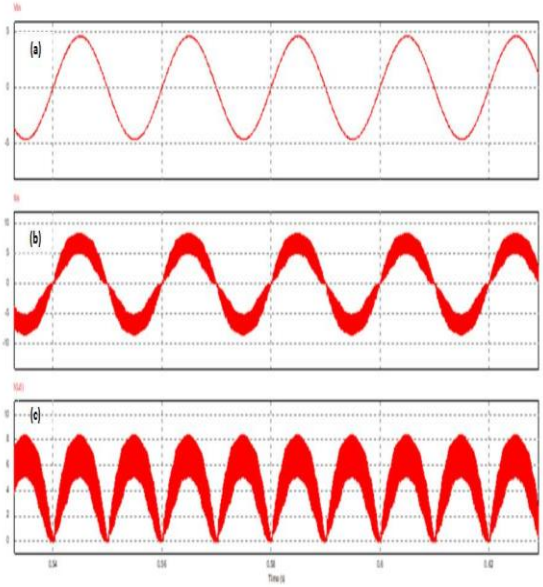


Fig. 6: Simulated output of PFC boost converter (a) Input voltage (b) Input current (c) Inductor current

Fig.6 represents the waveform of input voltage, input current and inductor current based on boost converter topology. It has advantages and limitations listed below.
Advantages:

- Low THD and best possible Power factor
- Due to high output voltage the size of storage capacitor is efficient
- Comparatively more holdup time
- The boost switch is easy to drive and current sensing is simple
- Due to direct path between input to output capacitor provides excellent surge management
- For boost PFC there are large number of control IC and design data

Limitations

- Output voltage should always be greater than the peak input instantaneous voltage
- Require isolation stage to step down the voltage
- Due to high bus voltage the common mode noise(a noise created by stray capacitance)is more
- No inrush current limitation at the startup
- The efficiency of the converter is low owing large conduction losses at low

To remove the limitations, a new concept fixed off time based is adopted in this paper. The concept of FOT (FIXED OFF TIME) is new and needs more exploration. The application of FOT as proposed in [9] in the field of bridgeless PFC, Interleaved PFC and more over in the use of FOT has not yet been fully explored with the flyback converter. The use of zero-voltage switching is still unexplored to reduce losses and increase efficiency.The Fixed frequency continuous conduction modei(FF-CCM) and the transition mode (TM) PWM (fixed on time, variable frequency) are the two methods used in the pre-regulators based on the boost converter.In the first mode, the inductor operates in continuous conduction mode (CCM) and uses a average current mode control, a complex technique that requires a considerable number of components. The second mode uses more complex peak current mode and makes the inductor work between continuous and discontinuous mode, which uses fewer components, it is unstable over 50% of the duty cycle and is more economical. The transition mode (TM) involves high peak current as compared to FF-CCM ..A third mode of operation in the pre-regulator based on boost converter is get popularity which is Fixed Off Time(FOT).Transition mode is suitable for low power application while FF-CCM is suitable for high power application. The FOT is conditionally stable for duty cycle greater than 50% and needs no compensation. The fixed frequency modulates the on and off times (ts sum is constant by definition) and the given converter operates in CCM or DCM. The same result can be achieved with the FOT approach.A FOT incorporates the conventional peak current control, in which the switch-on time T_{ON} of the switch is determined by the peak inductor that reaches the programmed value and T_{OFF} is determined by a special fixed-time modulator in such a way resulting in constant switching frequency as represented by Fig.7 and Fig.8.

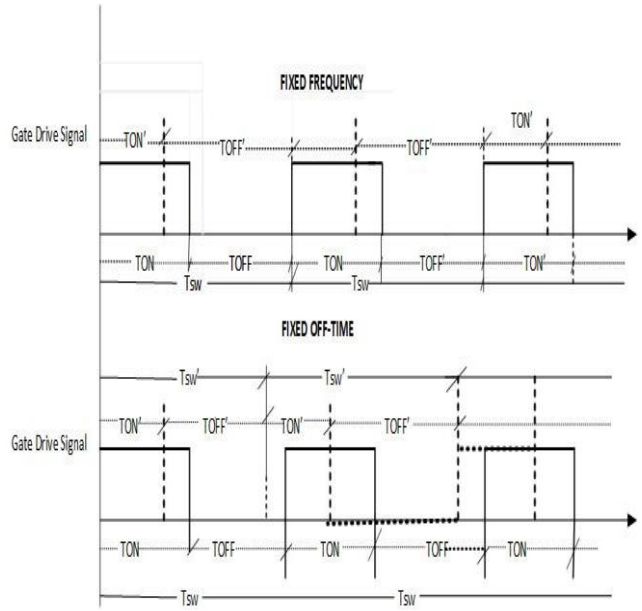


Fig.7: FF-PWM vs.FOT-PWM: Basic waveforms

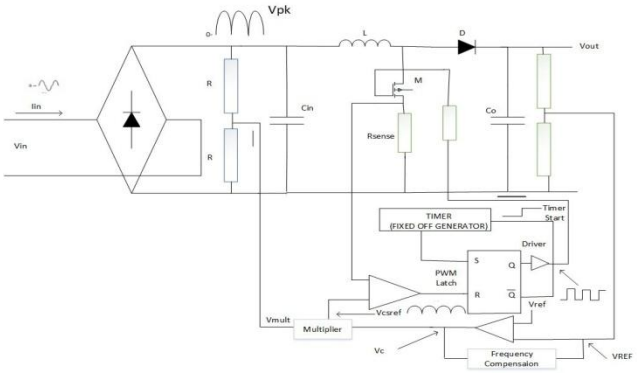


Fig.8: Circuit diagram of an FOT-controlled PFC preregulator

In FOT variable frequency is inherent, so to obtain fixed frequency system the OFF time of switch is modulated to obtains constant frequency system which is illustrated below mathematically.
Volt second balance equation for the boost inductor under the assumption of CCM operation

$$T\_ON\ Vpk\ i\sin\theta = T\_OFF\ (Vout\ i - Vpk\ i\sin\theta)$$

Where Vpk is the peak line voltage, $Vout$ the regulated output voltage and θ the instantaneous phase angle of the line voltage.Solving for T_{ON} we get

$$T_{ON} = \left\{\frac{V_{out}}{V_{pk}Sin\theta} - 1\right\} T_{OFF}$$

Then, the switching period $Tsw = iT_{ON} + T_{OFF}$ will be

$$T_{sw} = \left\{\frac{V_{out}}{V_{pk}Sin\theta} - 1\right\} T_{OFF} + T_{OFF}$$

$$= \frac{V_{out}}{V_{pk}Sin\theta} T_{OFF}$$

If $TOFF$ is changed proportionally to the instantaneous line voltage, i.e.if

$$T_{OFF}=KtVpksin\theta$$

$$T_{sw} = KtV_{out}$$

$$f_{sw}=\frac{1}{K_t V_{out}} \quad (10)$$

And, since $Vout$ is regulated by the voltage loop, also Tsw (and $fsw = 1/Tsw$) will be fixed.

III. DESIGN OF PFC CIRCUIT

The Power factor correction circuit employs the L4984D IC which incorporates the use of Fixed off Time (FOT). There are important feature and benefits with L4984D which are given in Table 1. Fig.9 represents the PFC regulator based on L4984D.Table.2 represents the input specifications of PFC circuit.

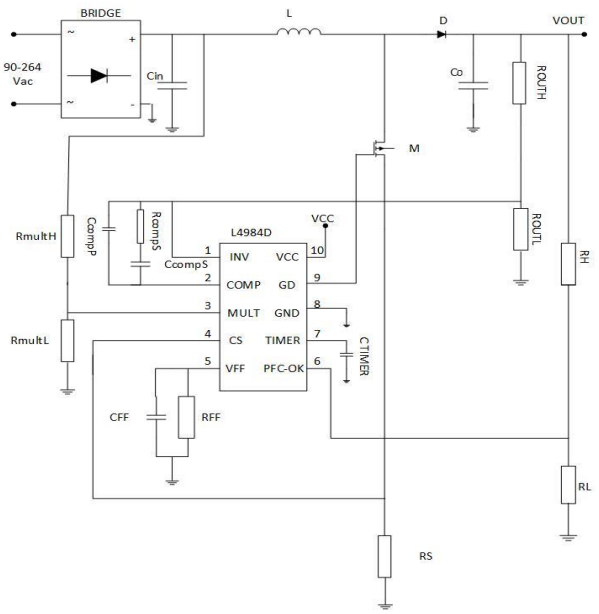


Fig. 9 PFC regulator based on L4984D IC

Table 1: Features and benefits of L4984D

FEATURE	BENIFIETS
Fixed frequency operation	Simple design and reduced BOM
Fast bidirectional input voltage feed forward($1/V^2$)	Mains drops and surge protection
Soft start	Inrush energy management
THD optimizer circuit	Improved performance
Protections embedded: • Feedback loop Failure • Overvoltage protection • Inductor saturation • Ac brown out	Avoid dc link capacitor burning and downstream converter damage More design reliability Avoid Mosfet damage Avoid bridge and inductor damage

Table 2: Input specifications of PFC circuit

PARAMETER	VALUE
Mains Input Voltage	100V to 300V
Minimum Mains Frequency	47-52 Hz
Rated Output Power (W)	140W
Regulated Dc Output Voltage (Vdc)	450V
Expected Efficiency (%)	92%
Expected Power Factor	0.99
Maximum Output Voltage (Vdc)	480V
Maximum Output Low Frequency Ripple (Peak-To-Peak)	22.5V
Minimum Output Voltage After Line Drop (Vdc)	350V
Hold-Up Time (ms)	15 ms
Ripple Factor(Kr)	0.3
Maximum Ambient Temperature (℃)	50℃
Switching Frequency(fsw)	50 kHz

IV. RESULTS AND DISSCUSION

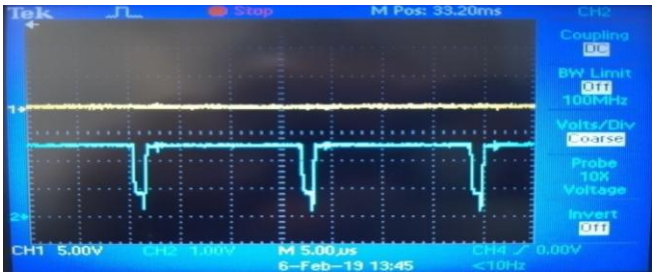
For proper working of IC L4984D there should be proper voltage on the pins. Incase voltage sensed is out of the range, the IC l4984d gets shutdown and in some cases in burst mode. Table 4.3 summarizes all the operating conditions that can cause device malfunction.

Table 3: Summary of L4984D redundant states

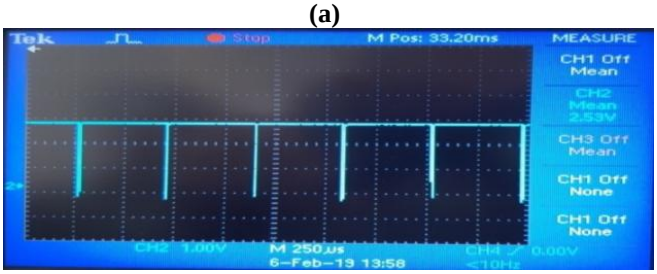
Condition	Caused	IC behavior	Restart Condition
UVLO	$V_{CC}<V_{CCOFF}$	Disabled	$V_{CC}>V_{CCOFF}$
AC brownout	$V_{PFC\_OK}<V_{PFC\_OK\_D}$	Stop switching	$V_{PFC\_OK}>V_{PFC\_OK\_D}$
AC brownout	$V_{VFF}<V_{DIS}$	Stop switching	$V_{VFF}>V_{EN}$
OVP	$V_{PFC\_OK}>V_{PFC\_OK\_S}$	Stop switching	$V_{PFC\_OK}<V_{PFC\_OK\_S}$
Feedback failure	$V_{PFC\_OK}>V_{PFC\_OK\_S}$ and $V_{INV} < 1.66V$	Latched-off	$V_{PFC\_OK}<V_{PFC\_OK\_S}$ and $V_{INV} > 1.66V$
Low consumption	V_{COMP}<2.4V	Burst mode	V_{COMP}>2.4V
Saturated boost inductor	$V_{CS} > V_{CS\_th}$	Stop switching	Aut start after 300s

Where V_{CCOFF} = 6V $V_{PFC\_OK\_D}$ = 0.27 V_{PFC_OK} =0.23v
V_{DIS} = 0.8v $V_{PFC\_OK\_S}$ = 2.5v V_{CS_th}=1.8V

Typical waveforms obtained from the prototype developed in the lab are given below.Waveforms across each pin in the open loop condition and Loaded condition are given

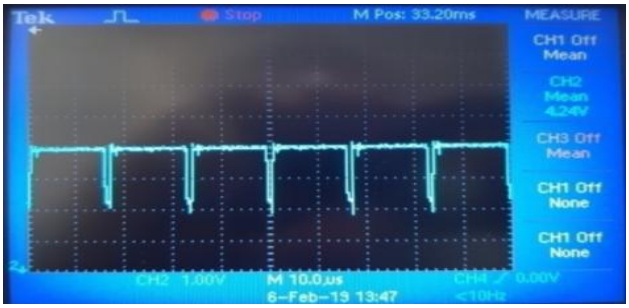


(a)

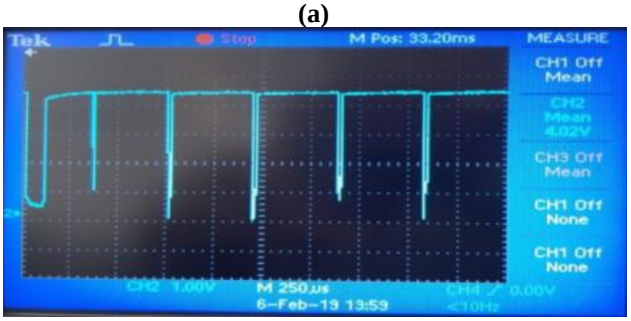


(b)

Fig. 10: INV pin waveform (a) loaded condition (b) no load condition

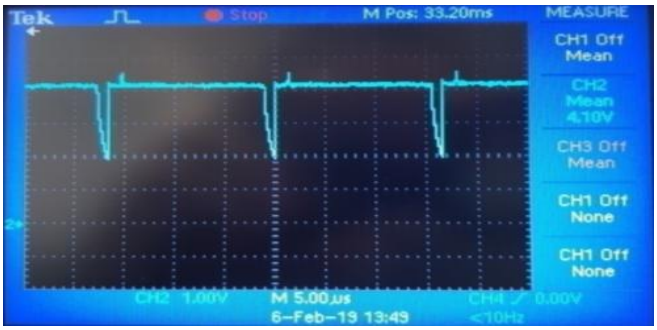


(a)



(b)

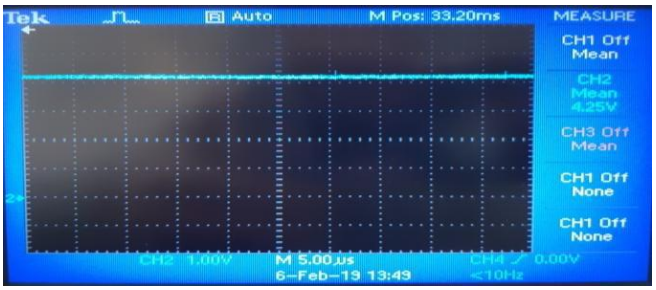
Fig. 11: COMP pin waveform (a) loaded condition (b)no load condition



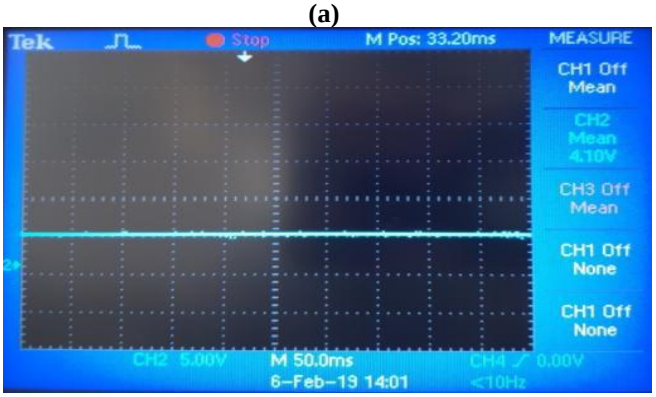
(a)

(b)

Fig. 12: MULT Pin waveform (a) loaded condition (b) no load condition



(a)



(b)

Fig. 13: VFF Pinwaveform (a) loaded condition (b) no load condition

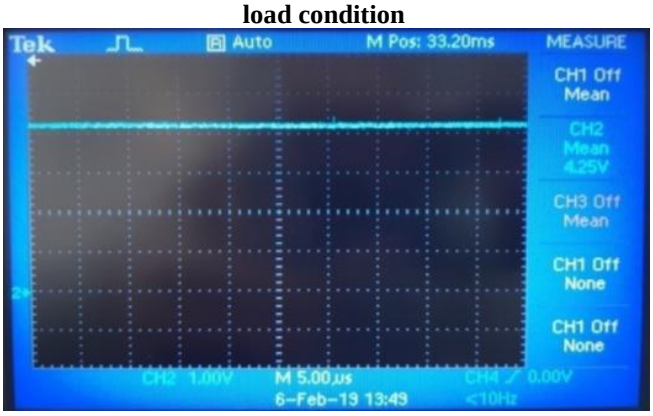


Fig. 14: PFC_Ok Pin waveform in loaded condition

The circuit contains two important parts, AC-DC converter with Power factor correction circuit and Flyback converter..The power factor correction implements the L4984D IC to accomplish Fixed OFF time technique. The PFC IC generates the pulse for Mosfet. The output of flyback converter is controlled by changing the duty cycle of the MOSFET. The output can be used for number of application such as battery charging, LED lighting, BLDC motor etc.

V. CONCLUSION

The power factor of the circuit is improved by using the power factor correction circuit based on the Fixed Off Time (FOT).Detailed mathematical modeling of fixed offtime approach is presented. IC L4984d based on Fixed Off Time (FOT) is used in the hardware. Simulation results are presented to show the improvement in input power factor. To verify the working of L4984D, different necessary operating voltages are presented in tabular form. Hardware results at different pins at loaded and unloaded conditions are presented.

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