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Memristor: A Unique Discovery for Reducing Power

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Abstract: ***A Process parameter variation has increasing, which results unpredictable device behaviour, due to occurrence of deep submicron CMOS technology. As the time passage this issue is exasperated by low power requirements which are approaching transistor operation into sub threshold regime. Principally for portable devices efficient, capable and process variation amiable memory is the most demandable in the market. In designing of low power memories, leakage power is observant parameter to design low power devices, because leakage power plays a dominant role in the total power utilization of the devices. In this paper, simple 6T SRAM formed with memristor has compared with the technique based 6T SRAM for the various parameters like total power and leakage power.***

Keywords: Vtcmos, Memristor, Forced Stack, Dtcmos.

I. INTRODUCTION

In Static Random Access Memory (SRAM) at discrete levels of extraction, cache memories occupy nearly 70 - 90 % area of the chip in modern processor. Due to this quality SRAM behaves as very important digital circuit part along with multi-core processors. As technology is proceed towards in the territory of nanoscale era, the "Process, Voltage and Temperature" (PVT) variations have become appreciable curtailment in the increasing anticipation of failure of SRAM and loss of bear in put together. CMOS process technology is uninterrupted scaling down in nanometer sovereignty, to satisfy Moores law for upcoming design desideratum. Therefore, leakage current and process variations of device become critical; which get larger due to shift in the "operating conditions". Fluctuation in the pre-established design parameters such as width, threshold voltage, length, etc at the time of manufacturing can lead to trouble like timing mismatch etc. Due to fluctuations, it shows significant increase in device malfunctioning. Threshold voltage is most credulous to discrepancy among the entire device framework. PVT variation creates a contemporaneous consequence on device, which to an certain extent can be attenuated at circuit level using some techniques. SRAM (Static Random Access Memory) is a very special type of memory that provides a link with CPU. Plotting of SRAM is difficult because its belongings to take large area and power. Because of that to overcome this problem we have designed Memristor based SRAM.

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Memristor is a forth missing non-linear resistor which acts as memory and it revamp the power and speed.In 1971 Leon Chua [1] was first accounted the postulation of memristors. He has presented it as a two-terminal device, and because of this a foundational connection between magnetic flux ϕ and charge q developed. $d\phi = M(q)\, dq$ is the relation for a memristor with memristance (M). A memristor behaves more like a resistor at a time, with the property that the resistance be fully dependent on the past history of the amount of current passing through it. In 2008, HP has first comprehended memristors as a nanoscale titanium dioxide cross point switches [2]. From that time to till now lots of research has been done and proves that the use of memristors as a unique non volatile memory element [3], its also called as resistive RAM .In past different type of logic circuit has been made using memristors [4, 5, 8, 9, 10, 11].

II. MEMRISTOR

Memristor's (memory-resistor) postulation was given by Leon Chua in 1971 and formalized by Kang [6,7] as a new primordial circuit element. Memristor consists of two layers ,a thin nano layer (6 nm–8 nm) of insulating TiO_2 and a second one ,Oxygen deficient nano layer of TiO_{2-x} sandwiched between two Pt nanowires [12,13]. Its electrical behaviour as a memory is determined by the boundary between these two sections. It is based upon the assumption where one part of the TiO_2nano layer loses oxygen ions while other part of TiO_2 receives oxygen ions (O2-). A change in distribution of oxygen ions within TiO_2 nano layer changes the resistance [14]. The voltage /current relationship of the memristor defined as *M(q),* can be modelled as:

Fig 1: Memristor

$$v(t) = \left[R_{on}\frac{w(t)}{D} + R_{off}\left(1 - \frac{w(t)}{D}\right)\right] i(t) \text{ .....(1)}$$

Where D is $Ti_{o2/Ti_{o2-x}}$, film thickness $R_{ON}$is the resistance for completely doped memristor while R_{0ff} is the resistance for the undopped region. The width of the doped region w(t) is given by:

$$w(t) = \mu_D \; R_{\frac{ON}{D}} \; q(t) \text{..... (2)}$$

for R_{ON}<<R_{off} that is the case of digital circuit,

Eq 1 is modified to;

$$M(q) = R_{OFF}\left(1 - \frac{\mu_D R_{ON}}{D^2} q(t)\right) \ldots\ldots\ldots(3)$$

where μD is the average dopant mobility (m2S-1V-1).

III. BASIC OPERATION OF MEMRISTORS

We can understand the basic operation of memrestior from fig 2. M1 (memrestior) connected t with a resistance R(L) in series and a voltage source V(s) .V (SET) behaves as a voltage source through which the memristor switches to a low resistance state where as V(RESET) also a voltage at which memrestior switches to a high resistance state. Memristor switches goes to a low resistance state, when V(S) = V(SET). R(L) is a resistor to limit the current , known as current limiting resistor. When the memristor is set the current which flows is known as the compliance current. [15]. If R(L) is too large the amount of compliance current will reduce. This obviates the memristor from entirely switching to a low resistance state in a given time. Let's, in this circuit the memristor used has an ON state resistance of 1k ohm and 300k ohm off state resistance [16]. The memristor will take a very long time to completely change its resistance to 1k ohm if R(L) is too large. The memristor can switch its state completely in 0.2ns. V (cond) is a voltage less than V(set), that cannot change the state of the memristor. It is the voltage that is applied to understand the state of the memristor.

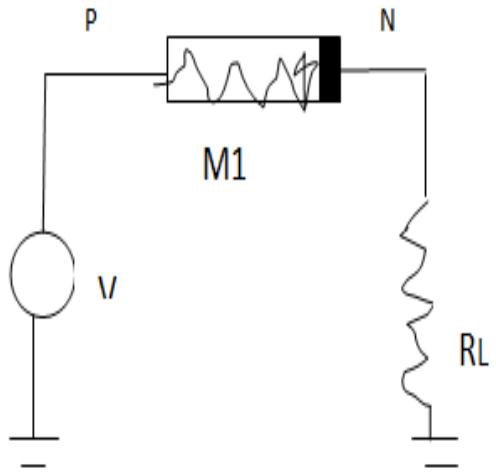


Fig 2: Memristor operation

A. 6T-SRAM

Figure 3 shows the conventional 6T-SRAM cell. In this two CMOS inverter, are cross coupled with each other. In write and read operation, both the transistors are connected to word line for activation of read and write operation. In active mode first word line gets actuated and turned on for access transistors for read data from memory cell or we can say to write data on memory cell through bit line. Power dissipation takes place during all read/write process. There are three types of operation takes place in SRAM

1) Stand by operation
2) Read operation
3) Write operation

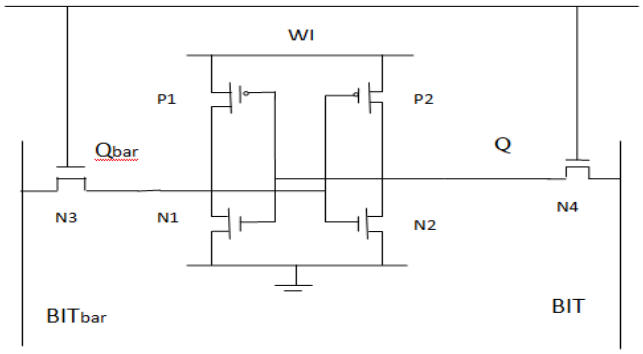
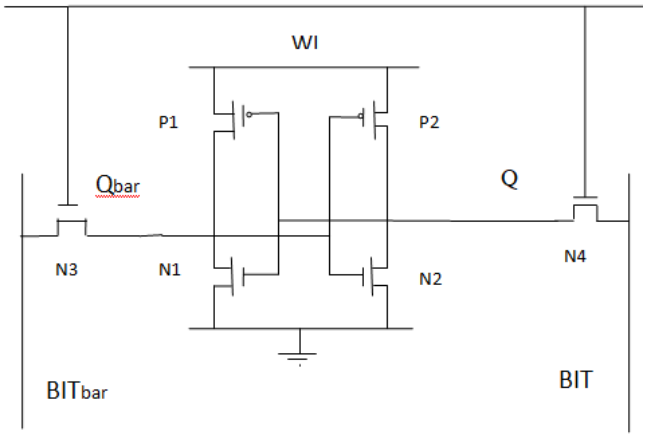


Fig 3: 6T SRAM



B. SRAM OPERATION

A standard one bit 6T SRAM structure is presented in Fig 3. A one bit SRAM cell operated in Standby, Read and Write mode. In each mode of operation SRAM cell suffers with strong power dissipation. A standard 6T-SRAM cell consists of two cross coupled inverter (P1, N1, P3, N3) and two pass transistor (N2, N4) to access the data in both the operations. The Write data enable line WL is pulled to HIGH to turning ON pass transistor N2 and N4 to access the values from the Read access line BL and BL'.Q and Q' are the stored node in Write/Read operation.

Standby mode: In this mode SRAM will store value "1"and "0" in Q and Qbar respectively, so that precharge cycle in SRAM circuitry pull capacitors HIGH for Bit and Bit bar'. When write line WL will be "1", the access pass transistors turned ON with a Standby of Read "1" mode for SRAM cell.

Read mode: In this mode memory should hold some value such that Q=1and Qbar=0 and WL should be one, Bit and Bit bar line should be output line, capacitor should be precharge means voltage should be Vdd near the capacitor point. There is voltage difference between th Q_{bar} and the node pt so the capacitor near the Qbar discharges so bit bar voltage decreases and the output value should be one.

Write mode: In write operation, memory block hold Q=0 and Q_{bar}=1, and WL should be one, bit and bit_{bar} equal to I/P because we have to write into the memory, we have to make bit_{bar} grounded.

IV. 6T SRAM WITH MEMRISTOR

Memristors are passive elements that are also known as a memristance, with resistance varying according to our requirements [14]. These devices with varying resistance are basically resistors, which be based on the history of the device. Memristors is the device where the data is stored as a resistance and these data can be used as a memory . For memristive devices its main application is as a memory, the other applications of these memristive devices are as functional blocks, analog circuits, neuromorphic systems, and logic circuits. Memristive devices definition is broader than the definition of memristors. We can use memristor term for all memristive devices [15,16].

If its further changes than future change in memresistance is depend upon its prior history, means total change that takes place through it or we can say the total flux through it. In this figure 4 memristors are connected with two NMOS. N1 is cross connected with the M2 memristor and N2 is connected with M1 memristor.

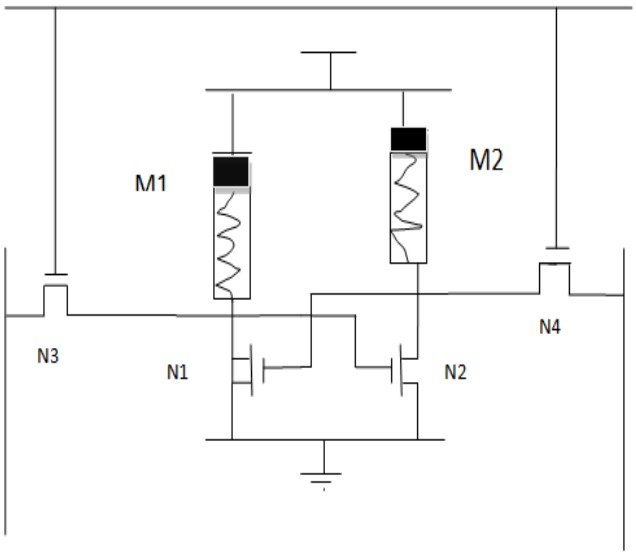


Fig 4: 6T SRAM with memristor

V. DIFFERENT TECHNOLOGY ON 6 T SRAM

A. SRAM WITH SLEEP TRANSISTOR TECHNIQUE

In figure 5 the circuit of SRAM with two sleep transistors that are enforced on the up side as well as on the down side of the circuit. Virtual power supply toward PMOS side and virtual ground NMOS side is formed with one PMOS transistor and one NMOS transistor. These two transistors are connected in series with the transistors of cell [17]. The working of the circuit is such that when the circuit is on; sleep transistor gets activated so that the circuit remains retained. Whereas in off state the sleep transistor gets off so that source node of the gate gets float because of this leakage path gets cut off. There are two main reasons for power reduction first is low sub-threshold leakage current of high Vth and second is stacking of transistors

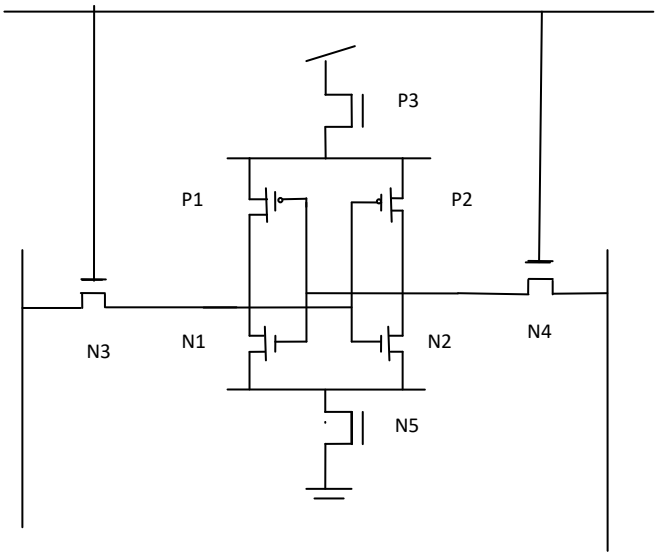


Fig 5: SRAM with sleep transistor technique

B. 6T SRAM WITH DTMOS TECHNIQUE

Figure 6 shows SRAM circuit using dynamic threshold voltage MOSFET known as DTMOS technique. In DTMOS; dynamic body biasing is used as substrate and gate terminals are connected together due to which there is body effect developed and which changes the threshold voltages dynamically of both PMOS and NMOS. In the fig consider the one part of the SRAM using DTMOS technique i.e. an inverter , that is in the active mode; the logic changes from low to high with a higher speed as threshold voltage is low for PMOS; whereas in the standby mode; the static leakage current is determined by the sub-threshold current of the NMOS which has high threshold voltage. The static leakage current decreases considerably because of the high threshold voltage of the NMOS [18]. The main advantage of using DTMOS technique is that it increases the cell stability while body biasing improves tolerance variation in logic.

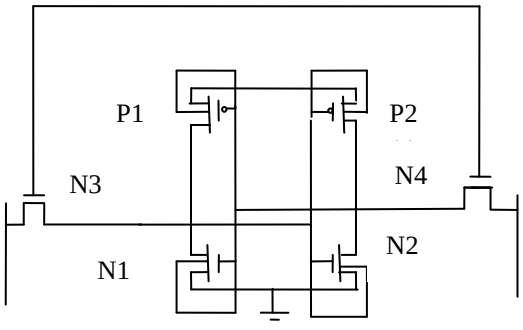


Fig 6: basic 6T SRAM with DTMOS technique

C. FORCED STACK TECHNIQUE

The figure shows 6T SRAM with force stack technique. The basic concept of forced stack technique is the mirror image of every transistor in the circuit. It has been observed from its working ,during off mode the stacked transistors are turned off so that reverse bias is induced between transistors , because of this reason sub-threshold leakage current reduces .Fig 7 shows forced stack technique on 6T SRAM

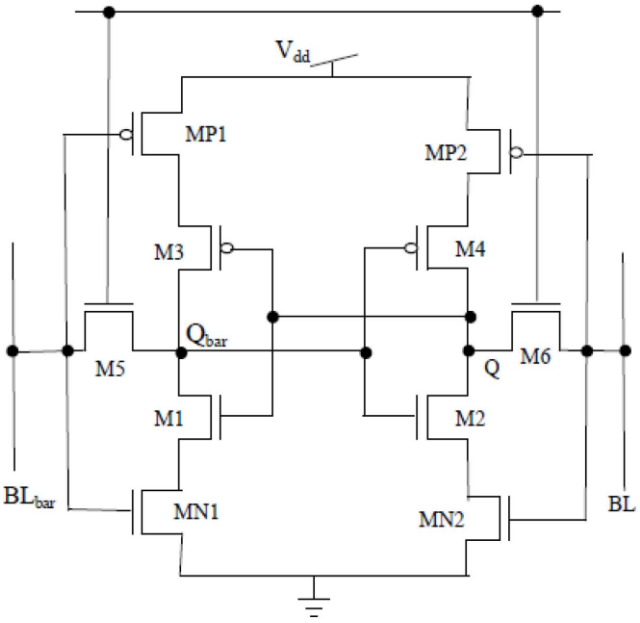


Fig 7: Forced stack technique on 6 T SRAM

D. SRAM DESIGN TECHNIQUES USING VTMOS

For low power applications as today's requirement, leakage current of the circuit with DTMOS technique is high. Further reduction of the leakage current in standby mode could be possible using Variable Threshold MOSFET (VTMOS) technique. Fig8 shows the circuit using VTMOS technique implemented on 6T SRAM. This VTMOS technique is based on working of MOS devices in which bias provided between gate and substrate. In case of PMOS; negative bias is produced between gate and substrate whereas in NMOS; positive bias is provided between gate and substrate. Although VTMOS is realized from DTMOS, however there is considerable reduction in power dissipation as well as operating current. Using VTMOS approach after simulation all other properties remain almost same.

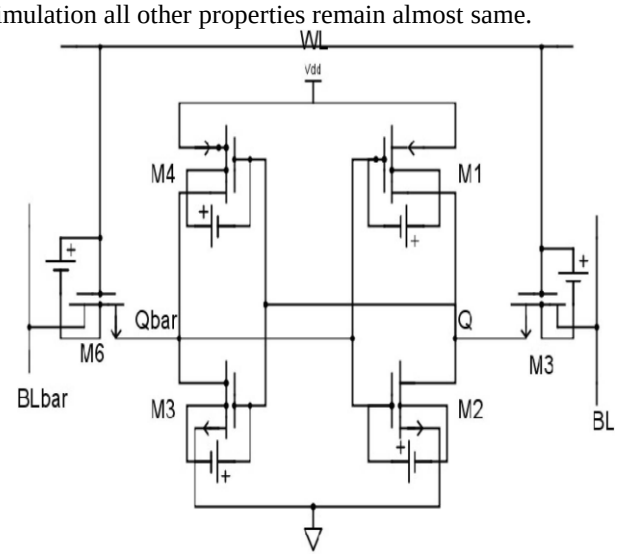


Fig:8 VTMOS technique on 6T SRAM

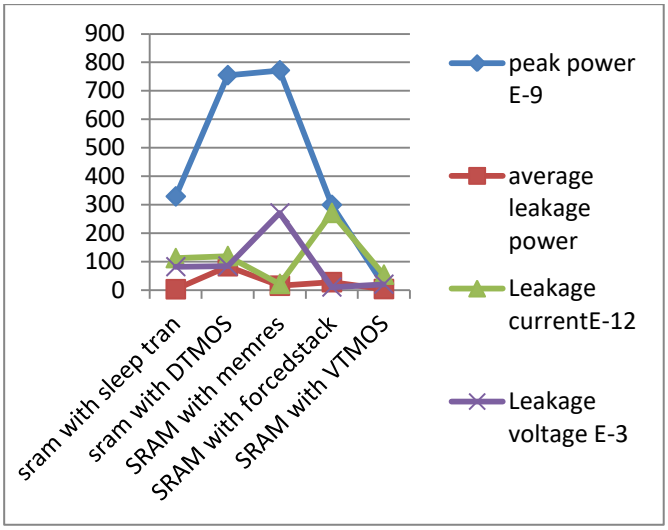
VI. RESULTS AND DISCUSSION

Simulation of the circuit mentioned in the paper has been done using cadence virtuso tool for 90nm as well as on 45 nm technology parameters.

Simulation results on 90 nm cadence virtuso tool

TECHNOLOGY	Peak Power dissipation	Average Leakage power dissipation	Leakage current	Leakage voltage
SRAM with sleep transistor	329.0E-9	3.084E-9	112.5E-12	82.29E-3
SRAM with DTMOS technique	754.7E-9	83.85E-9	119.79E-12	84.61E-3
SRAM with MEMRESTIOR	771.7E-9	15.44E-9	22.06E-12	271.1E-3
SRAM with VTMOS	17.96E-9	3.85E-9	54.39E-12	20.74E-3
SRAM with Forcedstack tech	299.3E-9	27.85E-9	271.2E-12	10.63E-3

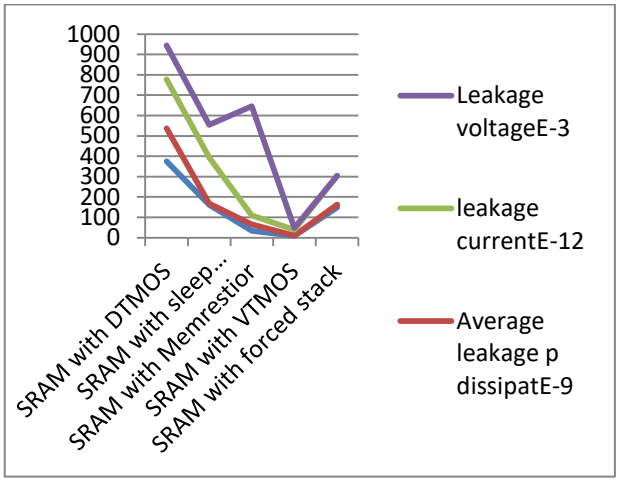
Results in graph for 90 nm cadence vituso tool



Simulation results on 45nm cadence virtuoso tool

Technology	Peak Power dissipation	Average Leakage power dissipation	Leakage current	Leakage voltage
SRAM with sleep transistor	162.0E-9	6.084E-9	225.5E-12	161.29E-3
SRAM with DTMOS technique	375.7E-9	160.85E-9	241.79E-12	166.61E-3
SRAM with MEMRESTIOR	33.7E-9	31.44E-9	45.06E-12	535.1E-3
SRAM with VTMOS	8.96E-9	1.476E-9	26.79E-12	9.78E-3
SRAM with Forcedstack tech	148.89E-9	14.79E-9	140.44E-12	6.334E-3

RESULT in graph for 45nm cadence virtusotool



V: CONCLUSION

By studying the result that we get from both the 90nm and 45 nm we saw that variation in results is same in both the technology. Result that we get with memrestior is very satisfying. so if we use memrestior with 6T SRAM , PVT shows satisfying result.

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Current Research Interests

- Low Power/Low Voltage Electronics
- Energy Aware Reliable SoC Architectures
- Nanoscale CMOS Device/Circuits/System Co-Design
- Characterization and Design of Low Power Logic and Memory
- Leakage Power Reduction and Ground Bounce Noise Reduction Techniques
- Power-Gated Arithmetic Circuits for Energy-Precision
- Process Variation Aware Power Gating Techniques
- Distributed Data-Retention Power Gating Techniques for Embedded SRAM
- CAD For VLSI
- Low Power Embedded Multimedia Communication System
- HDL Design Methods for Low Power/Energy Efficient FPGA Implementation

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