Noise-Tolerant Circuits in Deep-Submicron using Limiting Pass Transistors

Hanan A, Hosni Mahmoud

Abstract : In this paper, we propose a technique to increase the noise tolerance significantly over that of the existing circuit components and design styles. The paper proposes noise tolerance in the discrete, yet interrelated, areas of computational components design, powerless/groundless design style, dynamic circuit style, and memory design. Our results indicate a huge gain in noise-tolerance over the existing circuits and styles. The circuit components and design styles, developed by the technique, are integrated into architectures to study and demonstrate the combined effects of the techniques. This will be in addition to observing and analyzing the individual noise-tolerances of each components and circuit styles developed.

We are proposing the limiter pass transistor technique, which is a new method to immune dynamic circuits from noise. Our proposed technique demonstrates 5.9X times gain in noise tolerance over the convectional dynamic circuit and 3.0 X gains over the best known method in the literature. Based on the preliminary proposed technique, we expect to come with dynamic circuit styles that can provide an order of magnitude more noise-immunity.

Keywords : Noise-immunity, Efficient NAND, VLSI design, CMOS

I. INTRODUCTION

The continued scaling of the device and interconnect in the deep submicron realm of the complementary metal oxide semiconductor (CMOS) very large scale design (VLSI) has brought many new design challenges and exposed the limitations of the traditional VLSI design. One of the most severe problems in the deep submicron is that the circuits tend to malfunction by producing incorrect outputs in the event of inputs that have glitch [1]-[3]. Such noise problem has emerged as the critical reliability problem in the deep submicron, in addition to the power dissipation problem [4]-[6]. In this proposal, new technique is proposed to counter the

noise problem through novel circuit design techniques and methodologies.

Despite the recent technique advances in designing noise-tolerant circuits, there is a vast gap between the noise-tolerance provided by such technique and the noise-tolerance that will be actually needed in the very deep submicron

(VDSM) in order for the designs to function correctly [7]-[8]. For example, circuit components and design styles have been proposed that provide about 1.5 times to 2 times more noise immunity than the traditional VLSI design techniques.

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Although such level of noise-immunity may provide impressive results above the deep submicron level and also just at the edge of the deep submicron, they will almost certainly be insufficient to avoid functional failures in the VDSM [9]. The continued voltage scaling and the increased operating frequency requires increased noise-tolerance for correct operation [10]-[11].

The proposed technique aims to increase the noise tolerance significantly over that of the existing circuit components and design styles. In order to achieve excellence in a gamut of design problems, the paper proposes to target noise tolerance in the discrete, yet interrelated, areas of computational components design, powerless/groundless design style, dynamic circuit style, and memory design. Our preliminary results indicate a huge gain in noise-tolerance over the existing circuits and styles. The circuit components and design styles, developed by the technique, will be integrated into architectures to study and demonstrate the combined effects of the techniques. This will be in addition to observing and analyzing the individual noise-tolerances of each components and circuit styles developed.

The proposed technique is expected to deepen the understanding of noise-tolerance in the VDSM in several ways. In addition, it is expected to impact the human resource development in many dimensions.

II. OBJECTIVE

Noise in the deep sub-micron CMOS VLSI circuits is emerging as one of the prime challenges. Much remains to be done for building noise immune circuits and methodologies as the technique in this area is in infancy as compared to the technique that has been done in other areas such as the issues of area, delay, and power [11]-[14]. This technique paper is proposed to address some of these issues for noise immunity.

Various noise sources are prominent at the deep-submicron level of integration, such as power supply noise [15]-[17], cross-talk noise and noise originated due to device characteristics and technology. Power supply noise is mainly due to switching of I/O buffers and also due to switching of internal gates, which can be significant in deep sub-micron technologies. Cross-talk noise is due to the effect of coupling capacitances as the device feature size and interconnects have shrunk. This technique tackles the problem of noise in the context of CMOS digital design for deep-submicron. The term noise refers to any deviation from nominal supply or ground voltages at nodes that should otherwise represent stable logic 1 or 0. This may result in an incorrect state of operation and cause functional failures.

Before the advent of the deep-submicron era, the digital CMOS circuits were considered immune-enough-from-noise, which has changed now because of factors introduced in the deep-submicron technologies.

Through this technique, we propose to devise novel circuit components and design styles to combat the problem of noise in the deep-submicron. In order to achieve excellence in a gamut of design problems, the paper proposes to target noise-tolerance in the discrete, yet tightly interrelated, areas of computational components design, dynamic circuit style, memory element design, and development of noise-aware algorithms at the circuit and architectural levels.

Objectives/Features

To devise and develop novel dynamic circuit techniques for achieving high noise immunity in VDSM

To devise and develop novel methodologies for designing combinational critical-path circuit components for high noise-immunity in VDSM

To devise and develop novel memory elements and level converters for high-speed, low-power, and glitch-free operation in VDSM

To develop algorithms and computer-aided-design (CAD) tools capturing devised low noise circuits and architecture-building mechanisms

The proposed technique is expected to enhance the technique-understanding by contributing in the following core areas:

How to design gates that yield glitch-free but high-speed and low power operation in VDSM

How to design memory elements that eliminate glitch propagation and yield low power while maintaining high speed in VDSM.

Background of Related Technique

Since early days, noise tolerance has been an issue with digital circuit designers [2]-[3]. Many studies were conducted to find the sources of noise and several new logic techniques as well as analysis were proposed to provide reliable computation in the presence of noise [18]. In spite of all this, noise was never considered a major issue and was just considered as a precaution. Beginning from the early 90's, noise in digital circuits gained a new perspective and by the end of the decade, researchers realized its importance [18]. In the last few years, technique in this area has gained momentum but there is lot to be done. We propose mechanisms for encountering the circuit noise in separate sections and cover the directly related technique therein, as applicable.

III. PROPOSED TECHNIQUE FOR NOISE TOLERANCE IN DYNAMIC CIRCUITS

We propose a technique for boosting the noise-tolerance in the dynamic CMOS circuit in the VDSM. The aim is to devise techniques that yield significant noise immunity to ensure high reliability for the designs in 90 nm or below technologies. This paper is divided as follows. We give a brief introduction to the noise problem in the dynamic CMOS circuits followed by coverage of the related technique. Our proposed technique demonstrates 6.0x times gain in noise tolerance over the convectional dynamic circuit and 2.8 x gains over the best known method in the literature. Based on the preliminary proposed technique, we expect to come with dynamic circuit styles that can provide an order of magnitude more noise-immunity.

Noise in Dynamic Circuits

Dynamic circuits work in alternate precharge-evaluate cycles. Due to the inherent nature of this technique, it is affected by noise due to various factors. Once the charge accumulated at the precharge node is lost, it cannot be recovered until the next precharge cycle. The working of the CMOS transistor is dependent on (Vt) the switching voltage, the threshold voltage. In static circuits, the switching threshold is equal to Vdd/2 In dynamic circuits, this switching threshold is equal to the threshold of the transistor (Vth for NMOS PDN) is depicted in fig. 1, for an inverter. Whenever the amplitude exceeds Vth, an accidental charge loss can occur leading to functional failure in dynamic circuits. The dynamic circuits are plagued by charge sharing. Charge sharing occurs when the charge at the precharge node is redistributed between the dynamic nodes in the pull-up or pull-down stack as shown in Fig. 1(b). This occurs when the path is switched ON due to the inputs. The draining of the precharge node can lead to incorrect evaluation of logic in the next stage i.e. the evaluation stage.

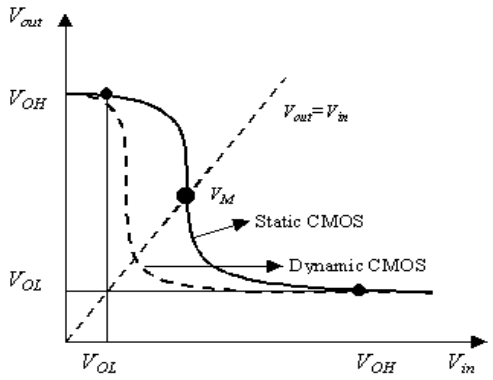


Fig. 1. Inverter voltage-transfer characteristic

The charge sharing problem can be tackled by introducing a bleeder transistor, which is connected in parallel to the pre-charge transistor. This reduces the impedance of the output node, but introduces static power consumption. This can be handled by making bleeder long and narrow. Another solution is to precharge internal nodes using a clock-driven transistor called keeper. Charge sharing can be also handled by rearranging the inputs in order in which they appear. This will negate the charge sharing path hence reducing the problem. The operation of dynamic gate relies on the dynamic storage of output value on a capacitor. Two sources of leakage can be identified, as illustrated in Fig. 2. Firstly, the output capacitance C_L partly consists of the drainage capacitance of the pull-down NMOS transistor.

The stored charge will slowly leak away through the reverse-biased diode of the diffusion area. Secondly, although the input transistor is OFF, some sub-threshold current can still flow from drain to source. This effect become more prominent when V_A is not completely 0, but approaches V_{tn} in the presence of noise.

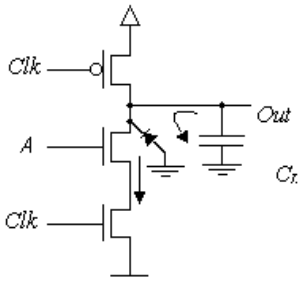


Fig. 2. Sources of leakage

The boosted source technique [10] deals with this problem by rearranging the dynamic circuits such that there are two dynamic nodes. It then uses a sense amplifier to determine the correct voltage level. A keeper transistor can also help to a certain extent. In VLSI, Capacitive cross-talk is the more prominent one.

Related Technique - Existing Noise Tolerant Techniques

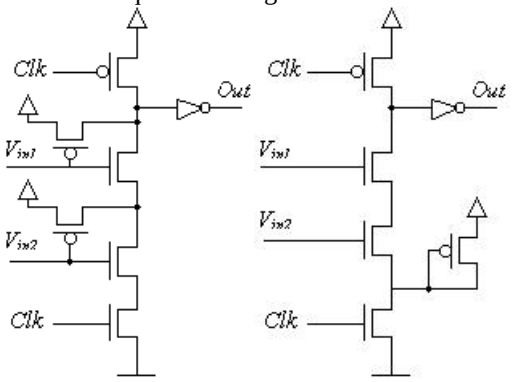
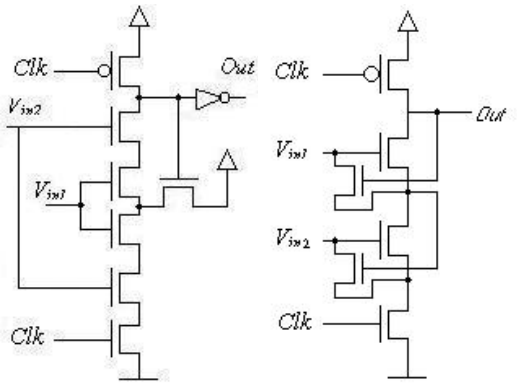


Fig. 3. (a) CMOS inverter technique (b) The PMOS pull-up



(c) The Mirror technique (d) The Twin-Transistor technique

One disadvantage of the CMOS inverter technique is that it is not suitable for NOR logic circuits since for some combination, the Vdd will short to ground leading to large power dissipation. The PMOS pull-up technique, shown in Fig. 3(b), reduces the charge leakage current in the evaluate net. Using a pull up transistor. This increases the switching threshold of the circuit to provide noise immunity.. The third technique referred as mirror technique, shown in Fig. 3(c), uses two identical NMOS evaluation nets and an additional transistor to achieve noise immunity. The output voltage controls the gate voltage of the additional transistor and it provides a path between Vdd and the common node. This technique avoids loss of static power but suffers from stacking net leading to higher delays. This can be avoided if the transistors are resized. The fourth technique is the twin transistor technique, shown in Fig. 3(d), resizing the twin transistor can increase the switching threshold. The twin transistor technique achieves this at the expense of energy.

IV. PROPOSED NOISE PASS TRANSISTOR LIMITER TECHNIQUE FOR DYNAMIC CIRCUITS

In the following, we are proposing the limiter pass transistor technique, which is a new method to immune dynamic circuits from noise. Fig. 4 shows a dynamic CMOS inverter implemented with the limiter pass transistor technique. The proposed technique utilizes a pass transistor for every transistor in the evaluation net. We call this transistor as the limiter pass transistor.

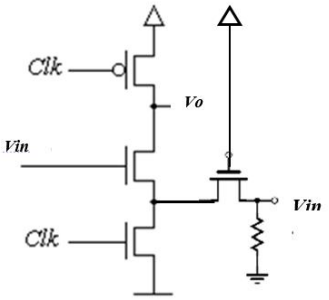


Fig. 4. A dynamic-CMOS inverter implemented with the proposed pass transistor limiter transistor

The gate voltage of this limiter pass is controlled by the corresponding transistor's input. The limiter pass transistor acts like a voltage source and delivers VX - Vth at the common source node or dynamic node where VX is the drain voltage of the limiter pass transistor. The drain voltage can typically be the supply voltage i.e Vdd. (VX can be smaller than Vdd resulting in less power consumption). This consequently increases the switching threshold for the dynamic CMOS inverter. The limiter pass transistor technique can be applied on both NAND and NOR logic circuits. Fig. 5 shows the circuit configuration for the NAND logic circuit type. We show the design of the NAND circuit in Fig. 5 with two inputs Vin1 and Vin2. The input Vin2 is "1" and Vin1 is "0". When the circuit is evaluating, the limiter pass transistor corresponding to Vin1 turns ON. This increases the gate to drain voltage to Vdd-Vtn , thereby raising the noise threshold of that transistor.

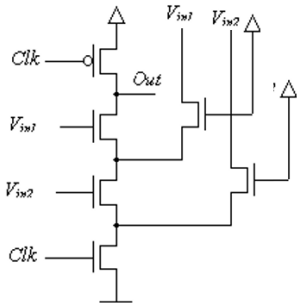


Fig. 5. Proposed technique applied on dynamic-CMOS NAND gate

The increase in the noise threshold comes into play only when the gate input is high. When the amplitude of the noise pulse becomes greater than the threshold of the limiter pass transistor, the internal node is charged thereby increasing the noise threshold. The increase in the noise immunity comes at the expense of power consumption. There is some power loss during evaluation period for certain input combinations and depends upon the logic implemented. But this increase in power consumption is a tradeoff for reliability achieved by the noise immunity in our preliminary technique. The limiter pass transistor technique reduces the charge sharing problem also thereby mitigating the need for any special preventive measure.

We utilized metrics in [23] to measure the noise-tolerance of the dynamic circuits. The metric used is a plot between the amplitude of the noise pulse (Vn) and the pulse duration or pulse width (Tn). Each measure indicates that if the noise lies above that point then the circuit will erroneously produce an output. All points below this fall in safe zone. Therefore the region below this curve is error free region of operation under noisy conditions. For quantitative value of noise immunity in dynamic circuits, a metric called average noise threshold energy (ANTE) [23] is calculated by the noise immunity equations. It is given by: ANTE=E(V2noiseTnoise), E is the average.

V. TECHNIQUE RESULTS AND COMPARISONS

In this section, experimental results are depicted from simulation. The limiter pass transistor technique is applied on dynamic CMOS NAND gate and a 1-bit dynamic CMOS full-adder. The circuits are simulated before and after the limiter pass transistor technique is applied on them. All the circuits are tested. Simulations utilizing HSPICE are performed with 1.2v Vdd.

SUM section of the 1-bit dynamic CMOS full-adder implemented with and without implementing the limiter pass transistor technique are tested. The noise immunity curves of NAND gate for conventional dynamic circuit, twin transistor technique and proposed technique are shown in Fig. 6. Table I shows the simulation results for different implementations of the NAND gate and the full adder. From the noise immunity measurement results, it can be seen that the use of limiter pass transistor technique for NAND gate provides an improvement in ANTE that is 7.5X higher than that provide by conventional dynamic circuit and 3.5X than that provide by the twin transistor technique. For 1-bit full adder, the improvement in ANTE is 4.6X over conventional dynamic circuit and 2.3X over twin transistor technique. The overall improvement as compared to conventional dynamic circuits is 5.9X, the improvement is 3.0X.

One disadvantage of the CMOS inverter technique is that it is not suitable for NOR logic circuits since for some combination, the Vdd will short to ground leading to large power dissipation. The PMOS pull-up technique reduces the charge leakage current in the evaluate net. Using a pull up transistor. This increases the switching threshold of the circuit to provide noise immunity. The third technique referred as mirror technique uses two identical NMOS evaluation nets and an additional transistor to achieve noise immunity. The output voltage controls the gate voltage of the additional transistor and it provides a path between Vdd and the common node. This technique avoids loss of static power but suffers from stacking net leading to higher delays. This can be avoided if the transistors are resized. The fourth technique is the twin transistor technique resizing the twin transistor can increase the switching threshold. The twin transistor technique achieves this at the expense of energy.

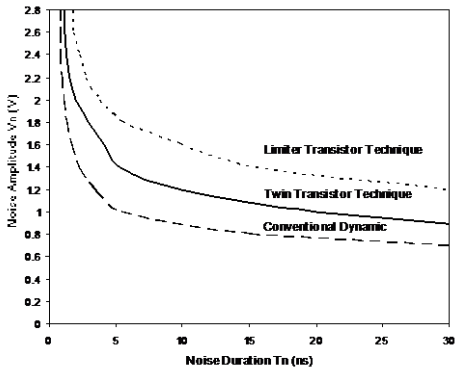


Fig. 6. Noise immunity curves of dynamic-CMOS NAND gate.

Table- I: Noise immunity results

	Conventional Dynamic	Twin Transistor	Proposed *Limiter pass transistor*
NAND gate	1.303	3.143	10.044
Full adder	4.512	8.882	18.978

VI. CONCLUSIONS

In this paper, we proposed the limiter pass transistor technique, which is a new method to immune dynamic circuits from noise Our proposed technique demonstrates 6.0x times gain in noise tolerance over the convectional dynamic circuit and 3.0 x gains over the best known method in the literature. Based on the preliminary proposed technique, we expect to come with dynamic circuit styles that can provide an order of magnitude more noise-immunity.

We also addressed the following problems:

- Starting with our current level of noise-immunity achievement (i.e. 5.9x times), perform technique to continue devise techniques that aggressively gain more noise immunity.
- Develop new dynamic circuit styles for noise-tolerance.
- Devise techniques that provide trade off among the level of noise-immunity, power consumption, and area.

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REFERENCES

1. Lei Wang and N. R. Shanbhag, "Noise-tolerant dynamic circuit design," *1999 IEEE International Symposium on Circuits and Systems (ISCAS)*, Orlando, FL, 1999, pp. 549-552 vol.1.
2. M. Kule, H. Rahaman and B. B. Bhattacharya, "Reliable logic design with defective nano-crossbar architecture," *2016 IEEE Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER)*, Mangalore, 2016, pp. 47-52.
3. Wei Su, Song Jia, Xiayu Li, Limin Liu and Y. Wang, "New noise-tolerant dynamic circuit design," *2009 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)*, Xi'an, 2009, pp. 254-257.
4. U. M. Bokare and Y. A. Gaidhani, "Design of CMOS dynamic logic circuits to improve noise immunity," *2017 International Conference on Communication and Signal Processing (ICCSP)*, Chennai, 2017, pp. 1948-1952.
5. Sarthak Bhuva, Praneeta Kalsait, "Keeper designs for wide fan in dynamic logic", *International Journal Of Microelectronics Engineering (IJME)*, vol. 2, no. 1, January 2016.
6. Pal and A. Islam, "Circuit-Level Technique to Design Variation- and Noise-Aware Reliable Dynamic Logic Gates," in *IEEE Transactions on Device and Materials Reliability*, vol. 18, no. 2, pp. 224-239, June 2018.
7. V. Dokania, A. Islam, "Circuit-level design technique to mitigate impact of process voltage and temperature variations in complementary metal-oxide semiconductor full adder cells", IET Circuits Syst., vol. 9, no. 3, pp. 204-212, May 2015.
8. V. Dokania, A. Islam, "Design of variation-resilient CNFET-based Schmitt trigger circuits with optimum hysteresis at 16-nm technology node", Proc. IEEE Annu. India Conf., pp. 1-6, 2013.
9. S. Hasan, A. K. Palit and W. Anheier, "Fault diagnosis of crosstalk induced glitches and delay faults," *13th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems*, Vienna, 2010, pp. 358-363.
10. S. Hasan, A. K. Palit, W. Anheier, "Test Pattern Generation and Compaction for Crosstalk Induced Glitches and Delay Faults", Proc. VLSI Design 2010, Jan 3–7, 2010.
11. W. Y. Chen, S. K. Gupta, M. A. Breuer, "Test Generation in VLSI Circuits for Crosstalk Noise", Proc. ITC 1998, pp. 641-650.
12. N. Nedovic and V. G. Oklobdzija, "Hybrid latch flip-flop with improvedpower efficiency," in Proc. Symp. Integrated Circuits Systems Design,SBCCI2000, Manaus, Brazil, Sept. 18, *22, 2000, pp. 211–215*.
13. N. Nedovic, M. Aleksic, and V. G. Oklobdzija "Conditional prechargetechniques for power-efficient dual-edge clocking," in Proc. Int. Symp. Low-Power Electronics. Design, Monterey, CA, Aug. 12, 2002, pp.56–59.
14. Y. Zhang, H. Yang, and H. Wang, "Low clock-swing condi-tional-precharge flip-flop for more than 30% power reduction," Electron. Lett., vol. 36, no. 9, pp. 785–786, Apr. 2000
15. J. Lin, "Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 1, pp. 181-185, Jan. 2014.
16. Y. He, C. H. Chang, J. Gu, "An area-efficient 64-bit square root carry select adder for low power application", *Proc. IEEE Int. Symp. CircuitSyst.*, vol. 4, pp. 4082-4085, 2005.
17. M. Tehranipoor and K. M. Butler, "Power Supply Noise: A Survey on Effects and Technique," in *IEEE Design & Test of Computers*, vol. 27, no. 2, pp. 51-67, March-April 2010.
18. P. I. Chuang *et al*., "26.2 Power supply noise in a 22nm z13™ microprocessor," *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2017, pp. 438-439.
19. T. Webel et al., "Robust Power Management in the IBM z13", */BM J. of Researchand Develnnment*, vol. 59, pp. 1-16, 2016.
20. R. Hegde and N. R. Shanbhag, "Energy-efficiency in presence of deep submicron noise," *1998 IEEE/ACM International Conference on Computer-Aided Design. Digest of Technical Papers (IEEE Cat. No.98CB36287)*, San Jose, CA, USA, 1998, pp. 228-234.
21. J.J. Covino, "Dynamic CMOS circuits with noise immunity", US Patent 5650733, 1997.
22. G.P. D'Souza, "Dynamic logic circuit with reduced charge leakage", US Patent 5483181, 1996.
23. S. R. Sahoo and K. K. Mahapatra, "Noise tolerant circuit techniques for high performance feedthrough logic," *2012 International Conference on Emerging Trends in Science, Engineering and Technology (INCOSET)*, Tiruchirappalli, 2012, pp. 354-358.