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Coefficient Combined and Shift and ADD Implementation (CSSI) Based Tunable Multiplierless Rotator Design

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Abstract: ***Signal processing algorithms like Discrete Fourier Transform, Discrete Cosine Transform, and Fast Fourier Transform Transforms find various applications in the field of Image processing, Wireless communication, Robotics, and many others. It covers basically three operations viz. Multiply, Shift and Accumulate. Hence if the input data goes on rising as in cases where high resolution is required the amount of multiply operations also rises significantly. For example the number of complex multiply operations in case of Discrete Fourier Transform is N^2, where N is the number of points. Latency becomes an important issue which needs to be addressed in today's era as we, humans, thrive for the fastest systems with maximum resolution. To reduce latency we need to either emphasize on reduction in amount of data to be processed or change the processing structure which can affect the overall time to output. Multiplierless techniques for this purpose has been always a research area as it helps in reduction of the later part. Coordinate rotation of digital computer (CORDIC) based techniques are well known for the Multiplierless implementation of the sinusoids. However it carries certain drawbacks viz. large number of iterations and accuracy. This paper provides Coefficient combined & shift and add implementation (CCSSI) based approach for the design of Multiplierless rotators for various transforms for multiple constant rotators as well. The approach improves the range of coefficients with respect to number of adders (the range taken is from 4 to 10 adders) and number of point (the range taken is from 1 to 64 points) compared to the existing approaches and is shown in the results. It also presents a novel tunable Multiplierless architecture.***

Keywords**: *CORDIC, CCSSI, DCT, DFT, Multiplierless rotators..***

I. INTRODUCTION

Digital signal processing, scientific computing, and other communication applications, signal transforms are a major part of signal analysis.

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There are various signal processing transform algorithms such as the discrete Fourier Transform [1], discrete cosine transform [2] and many more which are used in many of the digital signal processing applications. These algorithms are designed in a highly structured form and exhibit a large amount of parallelism. Thus these algorithms are well suited for the hardware implementation as a sequential data-path on a field-programmable gate array (FPGA) and DSP processors. These algorithms require many arithmetic steps to perform such as addition, subtraction and multiplication. There are many processors which handle the complex and huge multiplications which are necessary for the signal transform. Performing multiplication on hardware is much computationally costly as well as it also requires complex hardware which eventually requires a huge space for the development of the hardware.

With the increase in technological advancement, the requirement for the smaller, portable, cost-effective and efficient performance of any system is necessary. For adaptive signal processing systems, these are the important factors and more importantly the computational cost on the hardware point. Thus such computationally costly and power-consuming operation on the hardware is multiplication. Real-time hardware multipliers are required for adaptive signal processing which consume too much power and require memory which is scare system resources. Portable devices such as mobile phones and other communication devices require such multipliers for the signal analysis at the software level but on contrary the power consumption increases which leads to shorter battery life. Thus to reduce the power consumption one has to reduce the use of hardware multipliers at the software level which can be obtained by designing algorithms for signal processing in such a way that it uses fewer hardware multipliers.

Signal processing algorithms for the signal transforms such as discrete Fourier transform or fast Fourier transform [1] use complex numbers (Twiddle Factor) which are multiplied with signal and their corresponding frequency analysis is obtained. Here these complex numbers used in the algorithms are fixed which can be obtained by rotation by the fixed angle on the complex plane. Implementation of getting such a complex number on hardware is done using different Rotators. This rotator takes an angle as an input to it and performs rotation based on the input angle. There are various algorithms such as Coordinate rotation digital computer (CORDIC) [8] which uses these rotators.

Thus we need to select a complex number that increases the efficiency of the use of rotators and improves the performance.

Section II. gives an overview on the basics of CORDIC[8] algorithm, section III talks about CCSSI[18], section IV discuss on the proposed design, Section-V focuses on Results and Conclusions followed by conclusion and references.

II. CORDIC ALGORITHM[8]

CORDIC[8] stands for the Co-ordinate Rotation In Digital Computer. It aims at bringing down the number of multipliers used in the rotators by shift and add approach. The equations (1) shows the normal rotation for points *xi* and *yi* by and angle θ& equation (2) below show the normal operation of CORDIC[8] algorithm. To reduce the number of multiplications, there are some assumptions taken into consideration in equation (1) to convert it into shift and add approach. It has an advantage of having only a single multiplication of scaling factor if the number of iterations are comparatively higher.

$$\begin{bmatrix} Xi+1 \\ Yi+1 \end{bmatrix} = \begin{bmatrix} xi \\ yi \end{bmatrix} \begin{bmatrix} \cos\theta i & -\sin\theta i \\ \sin\theta i & \cos\theta i \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} Xi+1 \\ Yi+1 \end{bmatrix} = \begin{bmatrix} xi \\ yi \end{bmatrix} \cos\theta i \begin{bmatrix} 1 & -\tan\theta i \\ \tan\theta i & 1 \end{bmatrix} \quad (2)$$

Where $\tan\theta i = 2^{-i}$

But CORDIC[8] has a drawback of very large number of iterations for considerable accuracy which increases the latency. Various versions of CORDIC[8]-[14] are in in place in the literature for the multiplierless approaches for their implementation.

III. COEEFICIENT COMBINED SELECTION AND SHIFT AND ADD IMPLEMENTATION (CCSSI)[18]

This approach uses the combined coefficient selection and shit-and-add implementation (CCSI) method [18] and calculates the total number of coefficients obtained for the different cases. It does not set any restriction to C+jS selection, it selects the best and efficient coefficient which is then used for multiplication with x and y using shift-and-add implementation. The CCSSI[18] approach can solve two types of rotation problems SCR (single constant rotation) and MCR (multiple constant rotation). The goal here is to find the optimal coefficient and the total number of coefficients with the given input angles based on N point DFT or FFT, word length i.e. b bits, maximum allowed error e_{max} and number of allowed adders that can be used, which is represented in the block diagram in the Fig.1. below.

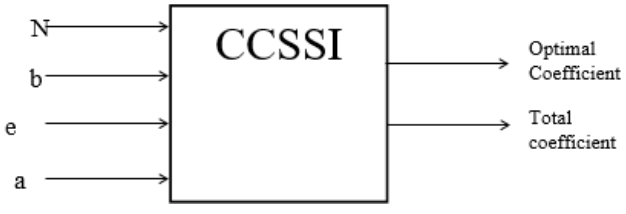

Fig. 1: Block Diagram of the proposed approach

To explain the proposed approach an example where word length and other parameters are considered as follows, b = 5, e_{max} = 0.05, angle = 14 & 38 and the number of allowed adders is 4. The following steps are used for the design.

Step-1: Complete the space of which consists of all possible finite word length values as shown in Fig.2 (a) for our example. It leaves 2^{2b-2} different coefficient values for every angle in the provided set of angles.

Step-2: Narrow down the set of coefficient based on the angle $\delta = \sin^{-1} e_{max}$ from the angles taken into consideration. This is shown in the Fig.2(b). Considering the coefficient between $angles\ \alpha + \delta\ and\ \alpha - \delta$ find out the coefficient which has the rotation error less than the e_{max}.

Step-3: Under this step, the coefficients are further reduced based on the scaling. In the example, fixed scaling is taken into consideration. Here the bound for reducing search space based on scaling is taken as $2 * R_{fixed} * e_{max}$, figure-2(c) illustrate the same.

Step-4: The number of adders that are required to design each rotation is found using the canonic signed digit (CSD)[15]-[16] method. Before that kernels are formed based on the remaining coefficient till Step-3. A kernel is the set of the coefficient for M angles. In the next step, the number of adders are calculated for the kernel and then reduced set of kernel based on the maximum adder bound is found.

Step-5: Calculate the number of efficient coefficients obtained at the end.

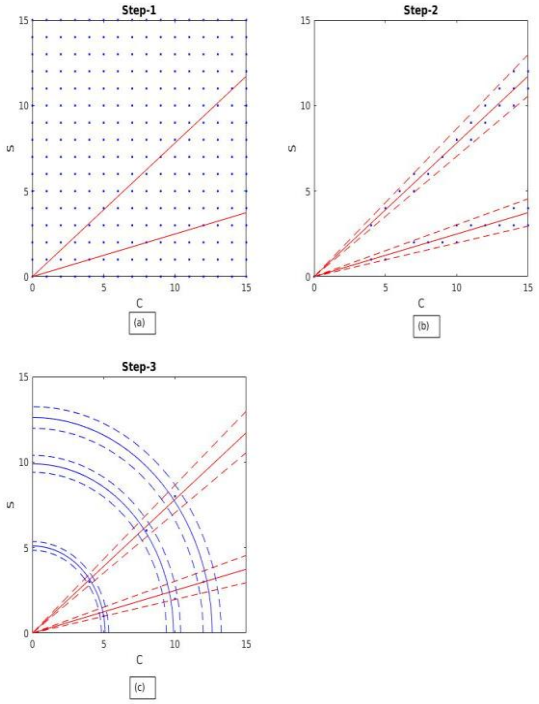

Figure 2: Steps for the proposed approach. (a) Initial design space with the required angles. (b) Reduced coefficient based on the delta angle. (c) Further reduction of coefficient based on the fixed scaling factor.

Table 1: MCR Remaining Kernel based on the proposed approach

$\alpha_1 = 0^o$	$\alpha_2 = 22.5^o$	$\alpha_3 = 45^o$	R	Err	Adder
7	7+3i	5+5i	7.31	$4.301x10^{-2}$	6
10	10+4i	7+7i	10.344	$4.301x10^{-2}$	4
11	10+4i	8+8i	10.8474	$4.299x10^{-2}$	4
13	12+5i	9+9i	12.8653	$1.068x10^{-2}$	6

IV. PROPOSED DESIGN

This section provides the design of the rotators based on the steps given in the above section. Also, this section provides an overview on how number of adders are calculated. First part focuses on the calculation of number of adders for the kernel based on given method discussed in section III [18].
The number of adders for single constant rotation are initially calculated which is described below,
If the Rotation coefficient is give as $P = C + jS$ the total number of adders for P is given as

$$AR(P) = 2 \cdot AM(C,S) + 2 \quad (3)$$

Where *AM(C, S)* is number of adders used for multiplying C and S with constant and it is calculated based on CSD approach. Similarly if *P* is just real number or imaginary number then the total number of adders for P is given as

$$AR(P) = 2 \cdot AM(C) \quad (4)$$

Or

$$AR(P) = 2 \cdot AM(S) \quad (5)$$

Using Canonic Signed Digit (CSD)[15]-[16],one can compute *AM(C)* and *AM(S)*. These cases are considered to optimum use of adders for designing rotators. Now using this SCR method, calculate number of adders for every coefficient in the kernel for each angle and then consider maximum out of it. Number of adders for kernel can be represented as

$$AK = \max\{AR(P_i)\} \quad (6)$$

Now considering an example of MCR[27] with three angles obtain the optimized coefficient for fixed scaling. Here the following angles are considered for designing the proposed approach. $\alpha_1 = 0^\circ\ \alpha_2 = 22.5^\circ\ and\ \alpha_3 = 45^\circ$. Reduction is carried out based on adders and scaling factors to get optimized coefficient. The maximum allowed error and number of adders considered here are as 0.05 and 6 respectively. After performing the steps provided in the section III the remaining coefficient are shown in the Table-1. The coefficient can be selected based on the requirement. Here it is observed that kernel with the minimum rotation error i.e. $1.068x10^{-2}$ is at approximate radius 13 and also satisfies the requirements of number of adders. However other Coefficients with lesser number of adders than 6 can also be used but one has to compromise with the rotation error.

V. RESULTS AND DISCUSSIONS

This section provides the results of the proposed approach which is obtained based on several parameters. The experiments carried out are for the N point FFT where the values of N are considered from 8 to 64.Also, word length (bits) for the design space starting from 4 to 12 bits for better accuracy is taken. In N-point FFT twiddle factor need to be calculated to transform signal from one form to another. For instance angles for 8 point are found by dividing $[0\ 2\pi]$ into 8 equal parts as a result we get a point at angles $[0, \frac{\pi}{4}, \frac{\pi}{2}, \frac{3\pi}{4}, \pi, \frac{5\pi}{4}, \frac{3\pi}{2}, \frac{7\pi}{4}]$.

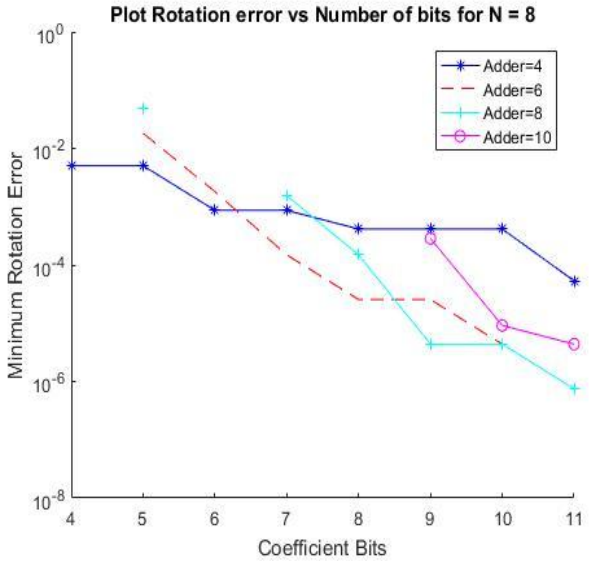

Fig. 3. Trade-off for minimum Rotation Error vs. number of bits b.

It is better to consider only angle which belongs to $[0\frac{\pi}{4}]$, since the points which belongs at an angle greater than $\frac{\pi}{4}$ can be generated by interchanging the values and changing signs of the points.
For calculation of number of adders required for the coefficient, CSD[15]-[16] approach is considered. The number of adders are calculated using CSD for each coefficient in the kernel of m angles, then checked for the maximum number of adders required in that kernel which is used as the minimum required adders for the multiplication for that kernel of m-angles.
Figures 3-6 presents the proposed results for the W_8, W_{16}, W_{32}, and W_{64}. The results shows the trade-off between minimum rotation error and word length (b-bits).

Different number of minimum required adders and max allowed rotation error are considered to obtain the coefficients for the set of kernels. Then, the optimum coefficient values based on the minimum rotation error and required number of adders is chosen.

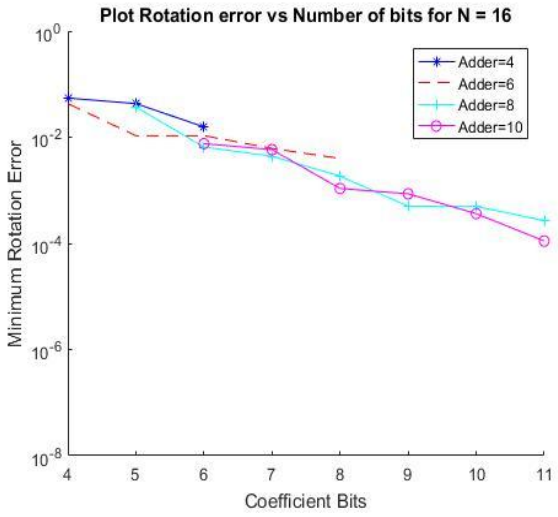

Fig.4. Trade-off for minimum Rotation Error vs. number of bits b.

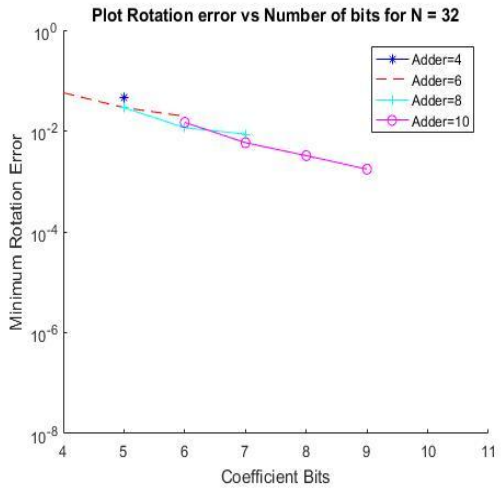

Fig. 5. Trade-off for minimum Rotation Error vs. number of bits b.

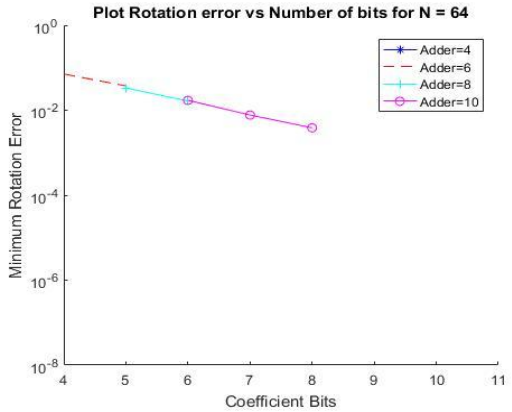

Fig. 6. Trade-off for minimum Rotation Error vs. number of bits b.

Now realization of these coefficients in the form of shifters and adders can be given as shown in the Fig.7 and combined realization of the kernel is showed Fig.8. For combined realization multiplexer is used.

In Fig.7. Realization of the rotator for $\alpha = 22.5^{\circ}$ using 7+3i is shown and then combined realization for the first kernel of table-1 is shown in figure-8.

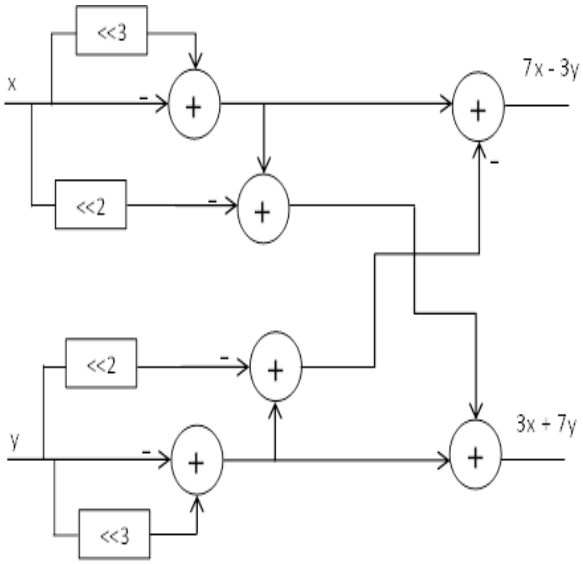

Fig. 7. Realization of rotator for alpha = 22.5 using 7 + 3i

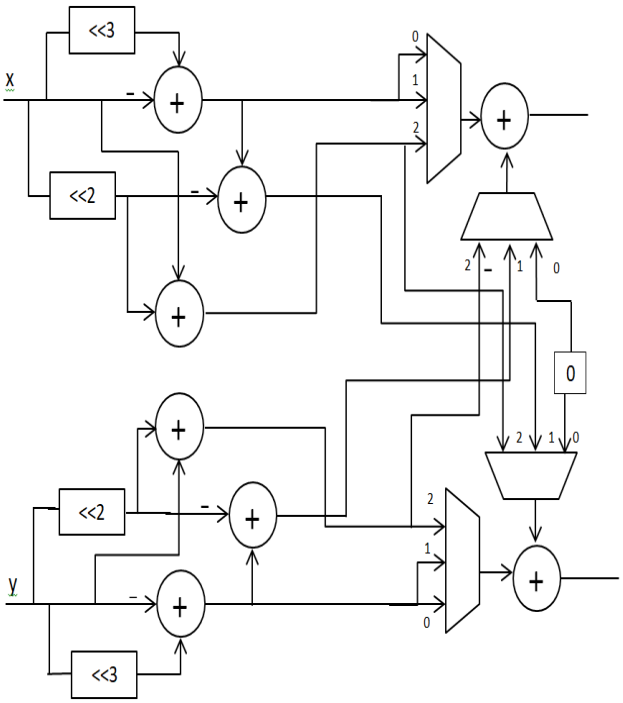

Fig. 8. Realization of combined rotator design for kernel. This figure is drawn for kernel-1 from Table-1

VI. CONCLUSIONS

This paper determines the technique which uses the CCSSI for the design of low complexity multiplierless constant rotators. This approach is further extended in finding total number of unique coefficients which are obtained with the help of CCSSI algorithm for different number of bits and N points.

Experimental results based on this approach indicates that the CCSSI based approach provides a multiplierless tunable architecture based on the parameters like number of bits, maximum allowable error and the number of adders. Multiple constant rotators for three different angles can be designed with the help of only eight adders which significantly improves the latency for determining the optimized coefficient for a transform.

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