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Double Gate MOSFETs: Assessment with Single Gate MOSFETs with Channel Material Configuration, its Structure Orientation and Future Applications

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Abstract*: In last 3 decades or so as we have scale down the MOSFETs with single-gate to nanometer region in order to maintain the performance level high but single gate MOSFETs still continue to suffers from the interface coupling, channel orientation, channel mobility, leakage current, switching delay and latch up. Further, the additional parameters such as short channel effects (DIBL, GIDL), body effect, hot electron effect, punch through effect, surface scattering, impact ionization, subthreshold swing and volume inversion has shown result inform of increase in leakage current, decrease of inversion charge and decrease in the drive current since double-gate MOSFET came into existence, which relies on the exploration of novel higher mobility channel materials which might perform even better than current existing single gate MOSFETs. This paper compares double-gate MOSFET configuration and single-gate MOSFET configuration using different performance parameters and channel material configuration and additionally assessed different channel materials along with its structure orientation and the future applications.

***Keywords* : Scaling, Double-Gate, MOSFET, Short Channel Effects, Volume Inversion.**

I. INTRODUCTION

In early 1930s there was requirement of finding a device which can potentially replace large sized, costlier, slow, high power consuming and high power dissipating Vacuum Tubes and following such a need gives rise to concept of FETs (Field Effect Transistor) but it does not demonstrate structure effectively because surface states were present at interface of semiconductor and oxide which does not permit electric field to enter in semiconductor material [1].

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This inefficiency was overcome by combining three layers of Metals (M), Oxide (O) and Semiconductor (S) over grown layer of Silicon Dioxide (SiO_2) on semiconductor surface results in permitting of electric field to enter in semiconductor material and gives rise to the new invention concept named Silicon (Si) based MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) with the single-gate configuration (SG-MOSFET) shown in Fig.1. In early 1960s, MOSFET have become most worth and precious building blocks of the Integrated Circuit (ICs) and now a days, they are even utilized as basic switching elements in field of ICs by keeping its basic structure similar to one fabricated in early 1960s [2].

When Moore's Law was first introduced, which states that during time period of nearly 18 months, number of transistors

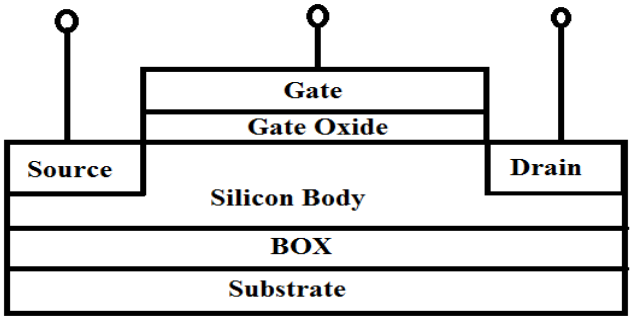

Fig. 1. Single-Gate Configuration of MOSFET

in particular area doubles shown in Fig. 2, thus in order to accommodate more and more transistors in the particular area

dimensions of MOSFETs are decreased continuously (scaling) with more focus has been spend on finding out the highly efficient chips with higher speed performance and lowering cost of transistors per chip with utilization of non-Si materials which have capabilities like higher carrier mobility, high speed device applications and low power consumption so that it can be future alternative for replacing the current single-gate MOSFETs [3-8].

Over the past few decades concept of device scaling has gained popularity in the ULSI and VLSI circuits for the requirements of performance in terms of minimizing power dissipation and power consumption. All dimensional parameters which are directly or indirectly affecting the device are scaled down under device scaling, which are summarized in Table- I.

The main advantages provided by scaling includes

1. Packing Density increases.
2. Chip Functionality increases.
3. Cost Effectiveness increases.
4. Gate Delays decreases.
5. Working range of Frequency increases.

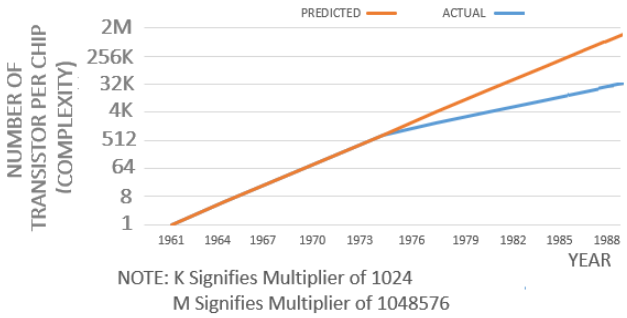

Fig. 2. Moore's Law

Table- I: Scaling Parameters

Device Specifications	Notation	Scaling done at Constant Electric Field	Scaling done at Constant Voltage
Length of Channel	L	μ^{-1}	μ^{-1}
Width of Channel	W	μ^{-1}	μ^{-1}
Capacitance of Gate	C_G	μ^{-1}	μ^{-1}
Capacitance of Oxide	C_{OX}	μ	μ
Electric Field	E	Constant	μ
Transit Frequency	F_T	μ	μ^2
Current	I	μ^{-1}	μ
Substrate Doping	N_A	μ^2	μ^2
Power	P	μ^{-2}	μ
Oxide Thickness	T_{OX}	μ	μ^{-1}
Transit Time	T_T	μ^{-2}	μ^{-2}
Voltage	V	μ^{-1}	Constant
Note: μ is scaling factor			

In addition to above advantages, device scaling also possesses certain limitations in form of Short Channel Effects (SCE) which are most popular in Short Channel Devices. The devices in which channel length has same order of magnitude similar one to source and drain depletion junction layer width are Short Channel Devices. The major SCE which effects the performance are summarized in Table- II. The SCE are prominent after down scaling because of presence of high electric field within a small short channel gap which proves to be steppingstone in desired functioning of device [9-15]. The two major phenomena responsible for these effects includes

1. Modifications done for threshold voltage.
2. Restrictions imposed by electron drift characteristics.

So in order to not only minimize the restrictions imposed by single-gate Si-based MOSFETs but also required for finding out the alternative device configuration along with exploring alternative channel materials and device structure, it gives rise to the concept of multi-gate of which one such configuration is double-gate MOSFET (DG-MOSFET). The device which makes the use of two gates simultaneously is DG-MOSFET. These two gates are situated present on opposite sides of device and are separated by gate oxide of constant or variable thickness as per need so as to utilize maximum gate control over channel and higher gate coupling which can also cancel the effect of fringing electric field lines moving from drain terminal to source terminal gives better current in drain shown in Fig. 3. This device remains in off state and movement of electrons will not be possible till we provide a voltage between gate terminal and source terminal (V_{GS}) greater than or equal to threshold voltage (V_{TH}) i.e. $V_{GS} \leq V_{TH}$. After providing $V_{GS} \geq V_{TH}$, surface potential starts increasing resulting in increase in injection electron exponentially (movement of electron is from source to body in case of N-type channel and movement of electron from body to source in case of P-type channel) is seen because of increase in energy level of electrons [16-22].

The major aim of this paper is to theoretically study and review the different double-gate MOSFETs in terms of channel material configuration, structure orientation and its future applications. The remaining portion of paper has four more sections. In second section we will reviews the conventional work done in field of double-gate MOSFETs simulated by making use of different channel materials by different researchers so far and in addition applications of these simulated configurations. In third section we will conclude the work. In fourth section we will discuss about future scope. In fifth and last section we end the list of papers used as references in this paper.

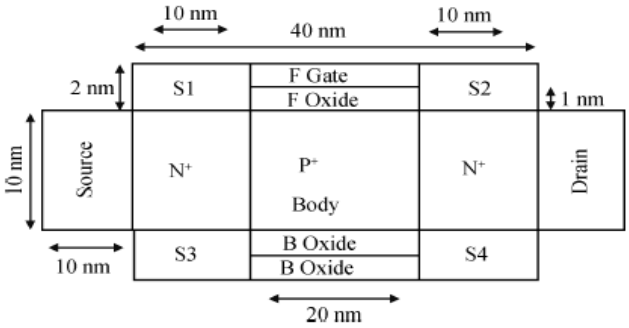

Fig. 3. Double-Gate Configuration of MOSFET

Table- II: Short Channel Effects

Short Channel Effect	Reason
Gate Induced Drain Lowering (GIDL)	When biasing of gate is done either by zero voltage or negative voltage, depletion region beneath gate and drain overlaps and the presence of high electric field in depletion region leads to flow of off state leakage current over drain to substrate junction.
Drain Induced Barrier Lowering (DIBL)	When drain voltage is increased, channel's potential barrier decreases, and electrons moves between source and drain without any opposition even if gate voltage is lower than threshold voltage.
Surface Scattering	The presence of high electric field in depletion region leads to the collision of electrons which are accelerated towards the depletion region and as surface is rough, these electrons will scatter more leading to the surface scattering.
Saturation Velocity	When short channel devices are operating in saturation mode and bias voltage is not lowered, saturation current flows because of carrier velocity in place of pinch off point which leads to transconductance reduction whenever operation mode of MOSFET is saturation mode.
Hot Electron Effect	The presence of high electric field in depletion region leads to the accumulation of charge because of electrons trapped in oxide layer and leads to the increase in threshold voltage.

Threshold Voltage Roll Off	The pattern of electric field generated by gate for short channel devices is 2D, because of same order of magnitude of channel length similar one to source and drain depletion junction layer width so less voltage is required for MOSFET operation thereby reducing threshold voltage.
Punch Through	When the source and drain depletion region merges in case of short channel devices and extends into channel leading to flow of uncontrollable current flow in this region which cannot be even controlled by gate bias.
Oxide Tunneling Effect	The presence of high electric field in depletion region for short channel devices leads to the reduction in oxide layer thickness which in turn is responsible for increase in flow of current in gate.
Carrier Mobility Degradation	The presence of high electric field in depletion region depletion region for short channel devices leads to the collision of electrons which are accelerated towards the depletion region and leading to the reduction in surface mobility.
Parasitic Resistance	The presence of parasitic resistance for short channel devices effects device performance more as channel length decreases as directly effects on-current and it must be kept low.
Parasitic Capacitance	The presence of parasitic capacitance for short channel devices effects device performance more as channel length decreases as directly effects on-current and it must be kept low.
Sub Threshold Leakage Current	The presence of weak inversion conduction region created by Hot Electron Effect in case of short channel devices leads to flow of diffusion current between drain and source whenever gate voltage is less than threshold voltage.
Reverse Bias Leakage Current	The flow of reverse bias current between drain-source and substrate for short channel devices has been seen whenever MOSFET is reversed bias or off state because of junction area.

II. LITERATURE REVIEW

This section reviews the conventional work done in field of double-gate MOSFETs simulated by making use of different channel materials by different researchers so far and in addition applications of these simulated configurations.

The different channel materials and gate configuration used so far, and applications of these simulated configurations are summarized in Table- III.

Table- III: Different channel materials, Gate configuration and Applications

References	Channel Materials and Gate Configuration	Application
[22]	$Si_{0.2}Ge_{0.8}$	Thermoelectric Applications
[23]	$Si_{1-x}Ge_x$	Source Step-FinFET and Inverter Applications
[24-25]	SiGe	Ballistic Carrier Velocity Improvement, High-Speed and High-Volume Optical Interconnect Applications
[26]	$Si_{0.75}Ge_{0.25}$	Better Channel Controllability and On-State Current Applications
[27]	Graphene Nanoribbon	DNA and Gas Sensing Applications
[28]	Si Nanowire	Low Noise Amplifier Applications
[29]	Ge Nanowire	High Mobility Channel Applications
[30]	Nanoscale Ge	High Speed and High Mobility Junctionless Configuration Applications
[31]	Nanoscale Si	Low Power and Tunnel FET Applications
[32]	Analytical Model	Subthreshold Region Applications
[33]	Fully Depleted SOI	Radio Frequency Applications
[34]	Vertical Slit	3-DM Integration Applications
[35]	Gate All Around	6-Transistor SRAM Cell Applications
[36]	β-Ga_2O_3, HfO_2 Gate Dielectric	High Power and High Temperature Electronic Devices
[37]	Heterogeneous Dielectric-Gate All Around-Tunnel	Improving Device Reliability Applications
[38]	Gaussian Like Doping	Optimization Peak Doping Concentration Applications
[39]	Doping Dependent Stack Channel	Multiple Threshold Voltage FinFET Configuration Applications
[40]	Negative Capacitance	Energy Delay Tradeoffs in Low Power Region Switching Applications
[41]	Heterojunction Tunnel Compact Model	Optimize Tunnel Logic Inverter Applications
[42]	2D Short Channel Semiconductor Material IV Model	Sub Threshold and Velocity Saturation Improvement Applications
[43]	III-V Compound Semiconductors	High Speed and Electrostatic Scaling Behavior Applications
[43]	InGaSb	P-Channel MOSFETs Applications
[43-44]	InGaAs	Current Amplification, N-Channel Configuration and Wide Channel Interactions Applications
[44]	Novel Dual Gate ($In_{0.75}Ga_{0.25}As$)	Current Amplification and Wide Channel Interactions Applications
[45]	Optimum High K-Oxide Ultra Scaling	Improving Gate Leakage Ultra-Scaled Applications
[46]	Dual Material	High Performance Circuit Applications
[46]	Dual Material Graded Channel	Threshold Voltage Applications
[47]	SiGe/SiC Asymmetric Dual-K Spacer	High Performance and Robust 6-Transistor (FinFET) SRAM Cell Applications
[48]	Sub 100 nm Tunnel FET	DRAM Applications
[49]	GaN	Commercial Power Devices and Converter Design Applications
[50]	Arsenic (As) and Antimony (Sb)	High Performance Digital Applications
[51]	SiGe Shell	Ultrathin P-FinFET Applications
[52]	Ge Ferroelectric	Current Drivability Applications
[53]	Schottky Barrier	Leakage Current Improvement Applications
[54]	Cylindrical Surrounding Gate	Improved Hot Carrier Reliability and Radio Frequency Applications
[55]	Gate Engineering	Stack Arrangement and Lateral Placed Gate Applications
[55]	Channel Engineering	Pocket Engineering and Graded Doping Applications
[55]	Work Engineering	Diminishing Threshold Voltage Applications

On analyzing above table, the research work carried out by researchers in channel material $Si_{0.2}Ge_{0.8}$, $Si_{1-x}Ge_x$, SiGe and $Si_{0.75}Ge_{0.25}$, can be turning point in future as Ge in future can be better alternative for Si based ICs as Ge not only possesses both balanced and high electron mobility and hole mobility, but also has higher density of states in comparison to the other III–V compounds at conduction band level which will have great impact in replacing pure Si in integrated circuits on chip and communication industry.

III. RESULT ANALYSIS

In this paper, we have analyzed and compared the double gate MOSFET with the single gate MOSFET in terms of different performance parameters for the different channel materials are summarized in Table- IV and the comparison results are summarized in Table- V. The results show that not only double-gate MOSFET are better in comparison with single-gate MOSFETand also shows lot of advantages, thus further utilize of these devices should be carried on. From above discussion, it can be concluded that DG MOSFETs possesses the phenomenally small structure, which has encouraging future in the field of VLSI design. It possesses very large degree of reliability, economical cost, dissipates less power, utilizes very small size (nanoscale), leads better gate electrostatic control of conducting channel and dynamic control of voltage, thus serves better performance. which will be surely be beneficial for designing CMOS circuit which are in very large requirements for electronics and communication industry, which satisfies all the conditions needed for maintaining the design of ICs. Thus, it can be concluded that future of these gates will be very much encouraging in coming generation.

Table- IV: Different Channel materials used for making comparison between Single Gate MOSFET and Double Gate MOSFET

Channel Materials	Used in Single Gate Configuration of MOSFET	Used in Double Gate Configuration of MOSFET
Si	Yes	Yes
SiGe	Yes	Yes
InGaSb	Yes	Yes
InGaAs	Yes	Yes
$Si_{0.75}Ge_{0.25}$	Yes	Yes
$Si_{0.2}Ge_{0.8}$	Yes	Yes

Table- V: Comparison between Single Gate Configuration of MOSFET and Double Gate Configuration of MOSFET for different channel materials

Performance Parameters	Single Gate Configuration of MOSFET	Double Gate Configuration of MOSFET
Electron Mobility of Channel	In Order of 1500 cm^2/Vs	In Order of 3420 cm^2/Vs
Hole Mobility of Channel	In Order of 450 cm^2/Vs	In Order of 1610 cm^2/Vs
Bandgap of Channel Material	Multiple of 1.12 eV	Multiple of 0.66 eV
Electric Field	Requires Break Below field of ~ 10^7 V/cm	Requires Break Below field of ~ 10^5 V/cm
Saturation Velocity	Multiple of 10^7 cm/s	Multiple of $6*10^6$ cm/s
Off State Leakage Current	Greater than 1nA/um	Less than 1nA/um
Drive Current Delay	Higher Order Range of 0.1 ns	Lower Order Range of 0.05 ns
Power Dissipated	Between 0.5 J/s to 0.7 J/s	Between 0.1 J/s to 0.3 J/s
Threshold Voltage	Between 0.35 V to 0.45 V	Between 0.1 V to 0.3 V

IV. CONCLUSION

After analyzing all the conventional work done by different researchers theoretically and comparing the double gate MOSFET configuration with single gate MOSFET configuration in terms of different performance parameters for different channel materials, one can conclude that the future of double gate MOSFET configuration is very prosperous and this device configuration has very bright potential to replace single gate MOSFET configuration in future in terms of speed, complexity, cost effectiveness, low power consumption and low power dissipation and this configuration can be future alternative to replace Si- based channel with non-Si materials which have capabilities like higher carrier mobility applications, high speed device applications and low power consumption applications.

REFERENCES

1. P. Khushwa, "Modelling of Substrate Depletion, Self-heating, Noise and High Frequency Effects in Fully Depleted SOI MOSFETs", Department of Electrical Engineering, Indian Institute of Technology, Kanpur, October 2016.
2. J. P. Raskin, "SOI technology pushes the limits of CMOS for RF applications", IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), pp. 17-20, January 2016.
3. C. Huyghebaert, Schram, Q. Smets, T. K. Agarwal, D. Verreck, S. Brems, A. Phommahaxay, D. Chiappe, S. El. Kazzi, C. L. DE LA Rosa, G. Arutchelvan, D. Cott, J. Ludwig, A. Gaur, S. Sutar, A. Leonhardt, D. Marinov, D. Lin, M. Caymax, I. Asselberghs, G. Pourtois and I.P. Radu, "2D materials: roadmap to CMOS integration", 2018 IEEE International Electron Devices Meeting (IEDM), pp. 1-4, December 2018.
4. M. Shakeri, R. Teymourzadeh and P. Maroofee, "Scaling Trend of CMOS based RF circuits", IEEE Conference of Semiconductor, pp. 1-5, July 2019.
5. H. H. Radamson, X. He, Q. Zhang, J. Liu, H. Cui, J. Xiang, Z. Kong, W. Xiong, J. Li, J. Gao, H. Yang, S. Gu, X. Zhao, Y. Du, J. Yu and G. Wang, "Miniaturization of CMOS", Micromachines (Basel), vol. 10, no. 5, pp. 1-52, April 2019.
6. G. V. Angelov, D. N. Nikolov and M. H. Hristov, "Technology and Modelling of Nonclassical Transistor Devices", Hindawi International Journal of Electrical and Computer Engineering, pp. 1-18, November 2019.
7. H. Agarwal, H. L. Chang, Y. S. Chauhan., J. P. Duarte, P. Kushwaha, Y. K. Lin, A. Sachid S. Salahuddin and C. Hu, "Unified Compact Model for Gate All Around FETs- Nanosheets, Nanowires, Multi Bridge Channel MOSFETs", Informatics, Electronics and Microsystems: TechConnect Briefs 2018, vol. 4, no. 1, pp. 249-252, May 2018.
8. V. A. Tiwari, and R Divakaruni, "Analysis of Systematic and Random Variation of Gate-Induced Drain Leakage in Silicon-Germanium channel PFET", 2016 3rd International Conference on Emerging Electronics (ICEE), pp. 1-, December 2016.
9. S. Cristoloveanu, J. Wan, and A. Zaslavsky, "A Review of Sharp-Switching Devices for Ultra-Low Power Applications", IEEE Journal of the Electron Devices Society, vol. 4, no. 5, pp. 216-227, September 2016.
10. A. S. Medury, K.N. Bhat and N. Bhat, "Impact of carrier quantum confinement on the short channel effects of double-gate silicon-on-insulator FINFETs", Microelectronics Journal, Elsevier, vol. 55, no. 1, pp. 143-151, September 2016.

11. B. Talukdar, P.C. Pradhan and A. Agarwal, "Review Paper on New Technology Based Nanoscale Transistor", Advances in Materials Science and Engineering: An International Journal (MSEJ), vol. 3, no. 1, pp. 39-58, March 2016.
12. U. A. Maduagwa and V. M. Srivastava, "Performance of Potential Distribution of CSDG MOSFET Using Evanescent-Mode Analysis", International Journal of Emerging Technologies in Learning (IJET), vol. 7, no. 4, pp. 5649-5653, 2018.
13. V.M. Srivastava, "Scaling Effect of Cylindrical Surrounding Double-Gate MOSFET: A Device Beyond 22 nm Technology", 2017 International Conference on Advanced Computing and Communication Systems (ICACCS -2017), pp. 1-5, January 2017.
14. T. D. Das, R. Pradhan, D. Singh, A. Rath, S. Pattnaik, "Performance Analysis of Devices in Double Gate MOSFET", International Journal of Engineering and Advanced Technology (IJEAT), ISSN: 2249 – 8958, vol. 7, no. 1, pp. 131-136, October 2017.
15. S. P. Narwade, A. U. Bhurke, S. Makdey, "Study on Performance of 22nm Single Gate and Multi-Gate MOSFET" International Journal of Scientific Engineering and Research (IJSER), ISSN: 2347-3878, vol. 4, no. 10, pp. 42-45, October 2016.
16. A. Singh, D. Kapoor and R. Sharma, "Performance analysis of SiGe double-gate N-MOSFET" Journal of Semiconductors, vol. 38, no. 4, pp. 1-7, April 2017.
17. B. Sharma and V Ramola, "A Review on Double Gate MOSFET", World Journal of Engineering Research and Technology (WJERT), vol. 3, no. 4, pp. 105-111, June 2017.
18. L. Witters , H. Arimura, F. Sebaai, A. Hikavyy, A. P. Milenin, R. Loo, A. De Keersgieter, G. Eneman, T. Schram, K. Wostyn, K. Devriendt, A. Schulze, R. Lieten, S. Bilodeau, E. Cooper, P. Storck, E. Chiu, C. Vrancken, P. Favia, E. Vancoille, J. Mitard, R. Langer, A. Opdebeeck, F. Holsteyns, N. Waldron, K. Barla, V. De Heyn, D. Mocuta, and N. Collaert, "Strained Germanium Gate-All-Around PMOS Device Demonstration Using Selective Wire Release Etch Prior to Replacement Metal Gate Deposition", IEEE Transactions on Electron Devices, vol. 64, no. 11, pp. 4587-4593, November 2017.
19. H. Sood, V. M. Srivastava, and G. Singh, "Advanced MOSFET Technologies for Next Generation Communication Systems-Perspective and Challenges: A Review", Journal of Engineering Science and Technology Review, vol. 11, no. 3, pp. 180-195, July 2018.
20. A. Z. M. Taiyer, S. M. J. Nobi and Md. R. Islam, "Performance of SMGAA and DMGAA SiGe MOSFETs: A Comparative Study", Proceedings of the 2017 4th International Conference on Advances in Electrical Engineering, pp. 719-724, September 2017.
21. S. K. Saha, "Modelling Statistical Dopant Fluctuations Effect on Threshold Voltage of Scaled JFET Devices", IEEE Open Access Journal, vol. 4, no. 1, pp. 507-513, March 2016
22. A. Singh, D. Kapoor and R. Sharma, "Review of SiGe Double Gate N-MOSFET", International Journal of Information Technology & Systems, vol. 4, no. 1, pp. 19-24, March 2015.
23. R. Saha, B. Bhowmick and S. Baishya, "Effect of Ge Mole Fraction on Electrical Parameters of Si1−xGex Source Step-FinFET and its Application as an Inverter", Springer Science, vol. 11, no. 1, pp. 209-219, April 2018.
24. L. Nguyen, A. Izadi and G. Denoyer, "SiGe BiCMOS Technologies for High-Speed and High-Volume Optical Interconnect Applications", Proceedings of IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), pp. 1-8, September 2016.
25. J.T. Teherani, "A Comprehensive Theoretical Analysis of Hole Ballistic Velocity in Si, SiGe, and Ge: Effect of Uniaxial Strain, Crystallographic Orientation, Body Thickness, and Gate Architecture", IEEE Transactions on Electron Devices, vol. 64, no. 8, pp. 3316-3323, August 2017.
26. B. Vandana, J.K. Das, S.K. Mohapatra and S. L. Tripathi, "Impact of Channel Engineering (Si0.75Ge0.25) Technique on Gm (Transconductance) And Its Higher Order Derivatives Of 3D Conventional and Wavy Junctionless FinFETs (JLT)", FACTA UNIVERSITATIS, Electronics and Energetics, vol. 31, no. 2, pp. 257-265, June 2018.
27. K. Tamersit and F. Djeffal, "Double-Gate Graphene Nanoribbon Field-Effect Transistor for DNA and Gas Sensing Applications: Simulation Study and Sensitivity Analysis", IEEE Sensors Journal, vol. 16, no. 11, pp. 4180-4191, June 2016.
28. N. Gupta and R. Chaujar, "Influence of Gate Metal Engineering on Small Signal and Noise Behavior of Silicon Nanowire MOSFET for Low Noise Amplifiers", Applied Physics A, Springer, vol. 122, no. 8, pp. 717-725, 2016.
29. H. Wu, W. Wu, M. Si, and P. D. Ye, "Demonstration of Ge Nanowire CMOS Devices and Circuits for Ultimate Scaling", IEEE Transactions on Electron Devices, vol. 63, no. 8, pp. 3049-3056, August 2016.
30. C. Jiang, R. Liang, J. Wang, and J. Xu, "Subthreshold Behaviours of Nanoscale Silicon and Germanium Junctionless Cylindrical Surrounding-Gate MOSFETs", Physical Sciences Review, vol. 3, no. 3, pp. 1-27, April 2016.
31. R. Ranjan, M. A. Rao, K. P. Pradhan and P. K. Sahu, "A comprehensive investigation of silicon film thickness (TSI) of nanoscale DG TFET for low power applications", Advances in Natural Sciences: Nanoscience and Nanotechnology", vol. 7, no. 3, pp. 1-7, August 2016.
32. D. Duggal and R. Sharma, "Review article on Analytical Models for Single Gate and Double Gate MOSFETs in Subthreshold Regime", International Conference on Microelectronics, Computing and Communications (MicroCom), pp.1-4, January 2016.
33. J. P. Raskin, "Analogue and RF performances of Fully Depleted SOI MOSFET", ISTE Open Science, FDSOI, vol. 19, no. 2, pp. 1-18, April 2019.
34. P. L. Yang, T. B. Hook, P. J. Oldiges, and Bruce B. Doris, "Vertical Slit FET at 7-nm Node and Beyond", IEEE Transactions on Electron Devices, vol. 63, no. 8, pp.3327-3334, August 2016.
35. P. Zheng, "Advanced MOSFET Structures and Processes for Sub-7 nm CMOS Technologies", Electrical Engineering and Computer Sciences University of California, Berkeley, December 2016.
36. M. J. Tadjerz, N. A. Mahadik, V. D. Wheeler, E. R. Glaser, L. Ruppalt, A. D. Koehler, K. D. Hobart, C. R. E. Junior and F. J. Kub, "Communication—A (001) β-Ga2O3 MOSFET with +2.9 V Threshold Voltage and HfO2 Gate Dielectric", ECS J. Solid State Science Technology, vol. 5, no. 9, pp. 468-470, July 2016.
37. J. Madan and R. Chaujar, "Interfacial Charge Analysis of Heterogeneous Gate Dielectric-Gate All Around-Tunnel FET for Improved Device Reliability", IEEE Transactions on Device and Materials Reliability, vol. 16, no. 2, pp. 227-234, June 2016.
38. B. Singh, D. Gola, K. Singh, E. Goel, S. Kumar and S. Jit, "Analytical Modelling of Channel Potential and Threshold Voltage of Double-Gate Junctionless FETs With a Vertical Gaussian-Like Doping Profile", IEEE Transactions on Electron Devices, vol. 63, no. 6, pp. 2299-2305, June 2016.
39. S. Dubey and P. Kondekar, "Doping dependent stacked channel FinFET for multiple threshold voltage applications", 3rd International Conference on Emerging Electronics (ICEE), pp. 1-4, December 2016.
40. G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Energy-Delay Tradeoffs in Negative Capacitance FinFET based CMOS Circuits", 3rd International Conference on Emerging Electronics (ICEE), pp. 1-4, December 2016.
41. Y. Dong, L. Zhang, X. Li, X. Lin and M. Chan, "A Compact Model for Double-Gate Heterojunction Tunnel FETs", IEEE Transactions on Electron Devices, vol. 63, no. 11, pp. 4506-4513, November 2016.
42. L. Nguyen, A. Izadi and G Denoyer, "A Short-Channel I –V Model for 2-D MOSFETs", IEEE Transactions on Electron Devices, vol. 63, no. 6, pp. 2550-2555, June 2016.
43. J. A. D. Alamo, D.A. Antoniadis, J. Lin, W. Lu, A. Vardi and X. Zhao, "Nanometer-Scale III-V MOSFETs", IEEE Journal of the Electron Devices Society, vol. 4, no. 5, pp. 205-214, September 2016.
44. B. S. Sharma and M. S. Bhat, "A Novel Dual-Gate Nano-Scale InGaAs Transistor with modified Substrate Geometry", 2017 International Conference on Innovations in Electronics, Signal Processing and Communication (IESC), pp. 1-4, April 2017.
45. M. S. Jelodar, H. Ilatikhameneh, S. Kim, K. Ng, P. Sarangapani, and G. Klimeck, "Optimum High-k Oxide for the Best Performance of Ultra-Scaled Double-Gate MOSFETs", IEEE Transactions on Nanotechnology, vol. 15, no. 6, pp. 904-910, November 2016.
46. B. Singh, D. Gola, K. Singh, E. Goel, S. Kumar and S. Jit "2-D Analytical Modelling of Threshold Voltage for Graded-Channel Dual-Material Double-Gate MOSFETs", IEEE Transactions on Electron Devices, vol. 63, no. 3, pp. 966-973, March 2016.
47. M. Gopal, V. Sharma, S. K. Vishvakarma, "Evaluation of static noise margin of 6T SRAM cell using SiGe/SiC asymmetric dual-k spacer FinFETs", Micro & Nano Letters, Institution of Engineering and Technology, vol. 12, no. 12, pp. 1028-1032, July 2017.
48. N. Navlakha, J. T. Lin, and A. Kranti, "Retention and Scalability Perspective of Sub-100-nm Double Gate Tunnel FET DRAM", IEEE Transactions on Electron Devices, vol. 64, no. 4, pp. 1561-1567, April 2017.
49. E. A. Jones, F. F. Wang and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges", IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 19-24, September 2016.

50. G. Pizzi, M. Gibertini, E. Dib, N. Marzari, G. Iannaccone and G. Fiori, "Performance of Arsenene and Antimonene double-gate MOSFETs from first principles", Nature Communication, vol. 7, pp. 1-9, August 2016.
51. E. Yu, W. J. Lee, J. Jung, and S. Cho, "Ultrathin SiGe Shell Channel p-Type FinFET on Bulk Si for Sub-10-nm Technology Nodes", IEEE Transactions on Electron Devices, vol. 65, no. 74 pp. 1290-1297, April 2018.
52. M. Bansal and H. Kaur, "Analytical drain current model to study the impact of interface trap charges on device performance of Double Gate Ge Ferroelectric FET (DGGeFeFET)", Proc. IEEE Conference on Emerging Devices and Smart Systems (ICEDSS 2018), pp. 1-4, March 2018.
53. M. Schwarz and A. Kloes, "Analysis and Performance Study of III–V Schottky Barrier Double-Gate MOSFETs Using a 2-D Analytical Model", IEEE Transactions on Electron Devices, vol. 63, no. 7, pp. 2757-2763, July 2016.
54. J.H.K. Verma, S. Haldar, R. S. Gupta and M. Gupta, "Modeling and simulation of cylindrical surrounding double-gate (CSDG) MOSFET with vacuum gate dielectric for improved hot-carrier reliability and RF performance", Springer, Journal of Computational Electronics, vol. 15 no. 2, pp. 657-665, June 2016.
55. N. Goyal and N. Sah, "Review Article on Impact of Various Engineering on Double Gate MOSFET", International Journal of Information Technology & Systems ISSN: 2277-9825, vol. 45 no. 2, pp. 38-43, April 2018.

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