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Design of PMOS and NMOS Input Folded Cascode Amplifier using 180nm SCL Technology Node for Low Power Application

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Abstract*: This paper presents the details design and simulation of the Folded Cascode amplifier using Source-Coupled-Logic (SCL) technology node for both the P-Type Metal Oxide Semiconductor (PMOS) and N-Type Metal Oxide Semiconductor (NMOS) input. The different way to implement the circuit design for a given specification has clearly described including all the design equation has been presented. All the parameter like open loop gain, Unity Gain Bandwidth (UGB) and Phase Margin (PM) are compared for both the NMOS and PMOS input fully differential folded cascode op-amp circuit are discussed and finally we have got after performance analysis that NMOS input fully differential folded cascode op-amp is the best choice for low power high speed application like in pipeline Analog to Digital (ADC). The circuit has been simulated using cadence virtuoso tool in 0.18µm SCL technology node.

Keywords*: Folded Cascode Opamp, Phase Margin, Open loop gain, Source-Coupled-Logic (SCL) technology, Unity Gain Bandwidth, Phase Margin.

I. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) technology is continuously scaled down to achieve low-power, high-speed, low-cost and high-density digital systems. Due to the rapid development in digital CMOS technology, single chip solutions becoming an attractive approach for systems with increase in complexity [1]. In the past three decades the world has been faced a rapid growth and evolution of integrated circuit (IC) technologies to cope up with the ever growing complexities of signal processing systems [3]. These ICs are widely used in the field of application like communications, medical imagining technique, speech processing, instrumentation, sonar, radar, satellite communication etc. Operational amplifier (Op-amps) are one of the most core parts of the many mixed signal and analog circuit design system [4]. Generally op-amps are divided into several types of topologies such as telescopic op-amp, folded cascode op-amp, two stage op-amp [5]-[7] etc. For our work in this paper we have designed a f
ully differential folded cascode op-amps circuit. Folded cascode can be formed by two types of transistor signal paths- NMOS and PMOS types [1].

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This types of signal paths produce a different op-amp circuit performance. However the folded cascode op-amps easily controls the input and output of common mode, and it can operate at a low-power voltage supply.

II. METHODOLOGY

The designed op-amps is basically consist of two parts [1]. First one is the differential input part and the second part is the common source stage. First stage is the fully differential input stage which converts the input voltage to current and provides a high gain [8]-[10]. The second stage is configured with a simple common mode source stage which converts the current to the voltage output and provides high output swing [11]-[12]. In the NMOS type fully differential folded cascode op-amps all the first three transistor M1, M2, M3 are the NMOS type and in PMOS type folded cascode op-amps all the first three transistor are PMOS type.

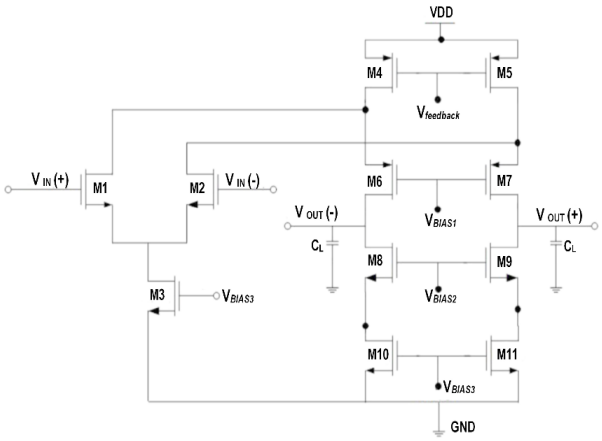

Fig. 1.Fully Differential Folded Cascode Opamp with NMOS Input

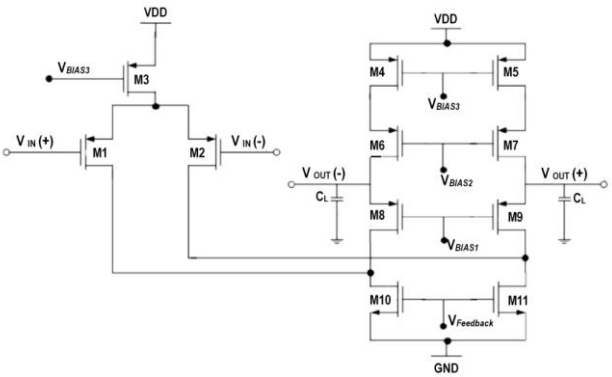

Fig. 2.Fully Differential Folded Cascode Opamp with NMOS Input

A. Design Specification

DC Gain: The DC gain of the fully differential folded cascode op-amps is the simply transconductance of the amplifier with infinite input resistance.

We have design the op-amp which DC gain is more than 50 dB [7].

Phase Margin (PM): It is the measure of the stability of the system [1].

Unity Gain Bandwidth (UGB): The unity gain bandwidth of an op-amp is the entire range of frequency in which an op-amp can produce high gain. So we should kept the UGB high as much as possible [6].

B. Design Steps

Step 1

First we have to find out the slew rate from the circuit [2]

$$Slew\ Rate = \frac{I_{B3}}{C_L} \tag{1}$$

Step 2

Then Find out the power dissipation of the circuit [2]

$$Power\ Dissipation\ (P_{diss}) = (V_{DD} - V_{SS})(I_3 + I_{10} + I_{11}) \tag{2}$$

Step 3

The Gain Equation of the circuit is [2]

$$Gain\ Equation = g_{m1} r_o \tag{3}$$

In place of r_o we can write that from the circuit is

$$Gain = g_{m1}[\{g_{m6} r_{06}(r_{o1} \parallel r_{o4})\} \parallel \{g_{m8} r_{o8} r_{o10}\}] \tag{4}$$

Step 4

Then we have to calculate the output resistance of M1, M4, M6, M8, M10 transistor in the circuit using [2]

$$r_o = \frac{1}{\lambda I_{ID}} \tag{5}$$

Step 5

Then we have to calculate the transconductance and the total output resistance [2]

$$g_m = \sqrt{2\mu C_{OX} \frac{W}{L} I_D} = \frac{2I_{ID}}{V_{DSAT}} \tag{6}$$

$$r_o = [\{g_{m6} r_{06}(r_{o1} \parallel r_{o4})\} \parallel \{g_{m8} r_{o8} r_{o10}\}] \tag{7}$$

Step 6

The dominant pole has a frequency of [2]

$$f_p = f_{-3db}$$

$$f_{-3db} = \frac{1}{2\pi C_L R_o} \tag{8}$$

Unity Gain Bandwidth

$$UGB = A_V(S) \times f_P \tag{9}$$

Step 7

To find out saturation Voltage [2]

$$V_{DSAT5} = V_{DSAT7} = \frac{1}{2}(V_{DD} - V_{OUTMAX}) \tag{10}$$

$$V_{DSAT9} = V_{DSAT11} = \frac{1}{2}(V_{OUTMIN} - V_{ss}) \tag{11}$$

Step 8

Now we have to find the W/L Ration of the Transistor [2]

$$\frac{W}{L} = \frac{2I_{ID}}{\mu C_{OX} V_{DSAT}} \tag{12}$$

Or,

$$\frac{W}{L} = \frac{I_{ID}}{\frac{1}{2}\mu C_{OX} V_{DSAT}} \tag{13}$$

For PMOS

$$\frac{W}{L} = \frac{I_{ID}}{K_P V_{DSAT}} \tag{14}$$

For NMOS

$$\frac{W}{L} = \frac{I_{ID}}{K_n V_{DSAT}} \tag{15}$$

After getting all the aspect ratio of the all transistors we have designed the circuit completely and run the simulation in various conditions. All the results are analyzed in the next part of this paper.

III. RESULTS AND ANALYSIS

All the simulation are done in the Cadence Software tool using SCL Technology taking minimum channel length of the transistors are taking as 0.18 µm. We have run the simulation using various supply voltage for constant room temperature and TT process state for the fully differential folded cascode op-amps in both NMOS and PMOS input type structure and compared all the results. The output plot of the nominal voltage (1.8 V) has been shown here and in the results table all the conditions are discussed.

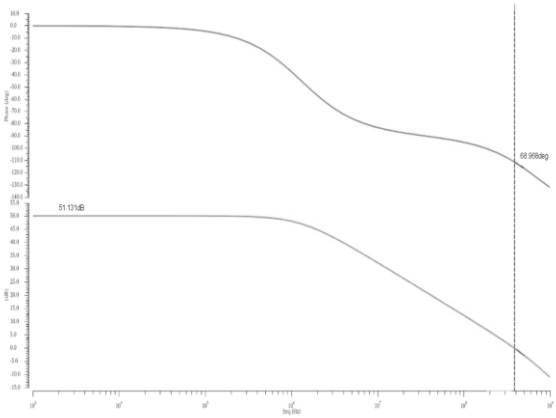

Fig. 3.Gain and Phase Margin (PM) plot when Vdd = 1:8V and Temperature is 27°C and process step is NN and Load Capacitance is 500f F for PMOS input

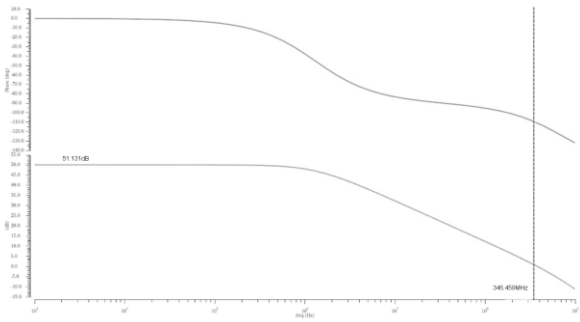

Fig. 4.Gain and Unity Gain Bandwidth (UGB) plot when Vdd = 1:8V and Temperature is 27°C and process step is NN and Load Capacitance is 500f F for PMOS input

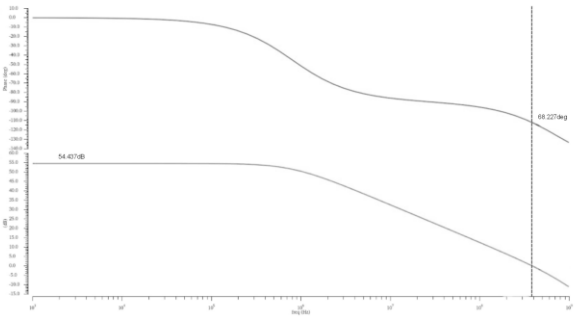

Fig. 5.Gain and Phase Margin (PM) plot when Vdd = 1:8V and Temperature is 27°C and process step is NN and Load Capacitance is 500f F for NMOS input

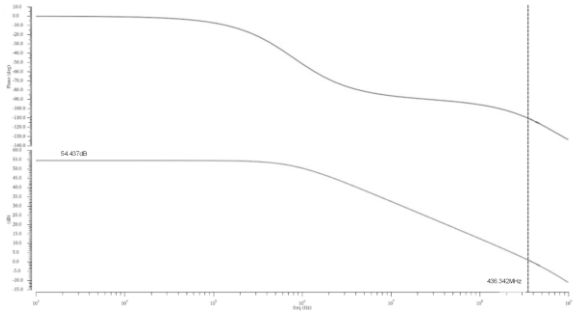

Fig. 6.Gain and Unity Gain Bandwidth (UGB) plot when Vdd = 1:8V and Temperature is 27°C and process step is NN and Load Capacitance is 500f F for NMOS input

From the graph we have seen that the gain of the NMOS input fully differential op-amp is more than the PMOS input circuit due to slew rate, flicker noise, elimination of body effect and less area for NMOS. Also the power dissipation is very less.

All the results are analysed which has found in the simulation in cadence tools in various conditions

Table- I: Corner Analysis of NMOS and PMOS input Fully Differential Folded Cascode op-amp when Vdd=1.8V, Load Capacitance=500 fF, Temperature=27°C and process state is NN

Parameter	PMOS input	NMOS input
Gain (dB)	51.131	54.437
Unity Gain Bandwidth (MHz)	346.968	436.342
Phase Margin (°)	68.968	68.227

Table- II: Corner Analysis of NMOS and PMOS input Fully Differential Folded Cascode op-amp when Vdd=2V, Load Capacitance=500 fF, Temperature=27°C and process state is NN

Parameter	PMOS input	NMOS input
Gain (dB)	52.923	54.931
Unity Gain Bandwidth (MHz)	353.786	471.398
Phase Margin (°)	67.915	67.431

Table- III: Corner Analysis of NMOS and PMOS input Fully Differential Folded Cascode op-amp when Vdd=1.6V, Load Capacitance=500 fF, Temperature=27°C and process state is NN

Parameter	PMOS input	NMOS input
Gain (dB)	50.591	52.889
Unity Gain Bandwidth (MHz)	333.579	423.671
Phase Margin (°)	69.186	68.973

From all the table we have found that the NMOS input fully differential folded cascode op-amp are the best as comapred to the NMOS input fully differential folded cascode op-amp.

IV. CONCLUSION

This work describe the design of the fully differential folded cascode op-amp and comparative analysis between the NMOS and PMOS input type topology. From the results we have found that at nominal voltage NMOS input fully differential folded cascode op-amp gives almost 54.43 dB which is pretty good as compared to the PMOS input circuit. Also the size of the NMOS input fully differential folded cascode op-amp is less as compared to PMOS input. So low power high performance application NMOS input fully differential folded cascode op-amp performance is best.

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Deepjyoti Kalita received B. Tech in Electronics and Communication Engineering from Assam Central University, Silchar in 2018. Currently he is in the final year of M. Tech from Indian Institute of Information Technology, Guwahati India in Electronics and Communication Engineering Department. His area of interests are Analog IC Design, Mixed signal circuits, Biomedical research, Machine Learning and AI in Healthcare.