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Full Adder for Low Power Applications

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Abstract: ***In an electronic processing system, addition of binary numbers is a fundamental operation. A one bit low power hybrid FA(full adder) is shown in showing performance improvisation by analysis and comparing with other conventional adders. 1 bit low power hybrid full adder is considered as a good way for enhancing the speed of the circuit in comparison with other conventional circuits of full adders. In that analysis paper, one bit low power hybrid FA(full adder) is implemented by EDA tool and the simulation is analysis by using generic 90nm CMOS technology at 5 volts and comparison is done at various voltages with other conventional full adders. For comparing 1 bit low power hybrid full adder with other conventional adders at various parameters such as static and dynamic power usage, delay & pdp (power delay product) are taken into consideration to show that 1 bit low power hybrid full adder is most suitable for various low power applications.***

Keywords: 1 bit low power hybrid full adder is considered as a good way for enhancing the speed of the circuit in comparison with other conventional circuits of full adders.

I. INTRODUCTION

In current years due to hasty growth and development of integration system of manufacturing if ICs from small scale integration (which allow the manufacturing of ICs with 1-10 transistor in a single chip) to ultra large scale integration (which allow manufacturing of ICs which consists of billions of transistor in a single chip) which lead the development in the electronics world[1]. Due to advancement of electronic world development takes place in the electronics devices in smart phones, laptops, computers which demand low power consumption, high speed performance with very less time propagation delay[2]. In those devices arithmetic logic units adders plays a vital role to perform the various logical operation (addition, subtraction, multiplication, division) in a system. Full Adder is the adder which adds three inputs and produces two outputs.

Some reason panaches are uses recently for contrivance full adder prison cell. Respectively reason panache have their peculiar loots & difficulties. Normal stationary complementary metal oxide semiconductor full adder is built on consistent complementary metal oxide semiconductor structure with tug active and tug downcast transistors[3].

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This adder offers bursting production electrical energy blow in contradiction of electrical energy & sizing of transistor.

Therefore the restrictions of that project is its higher series and sluggish swiftness because of the obtainability of positive metal oxide semiconductor devices and bigger contribution capacitance of the stationary complementary metal oxide semiconductor reason gateways. Happening a additional pointer, CPTL(Complementary pass transistor logic) is reckless & offers complete electrical energy blow production. The conventional full adders are considered in this paper for performance exploration of 1 bit low power hybrid FA(full adder)[3-4].

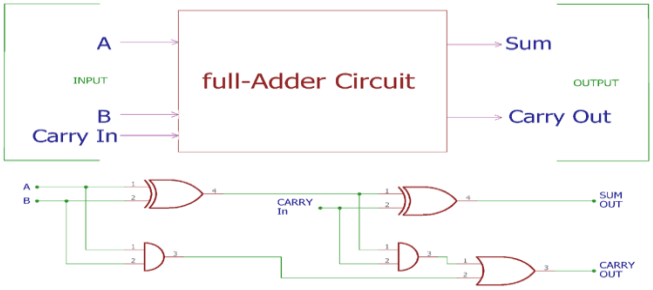

Figure 1:- Basic full adder Circuit

Table 1:- State Table of one bit FA(full adder)

Input			Output	
A_{in}	B_{in}	C_{in}	Sum	C_{out}
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0

Full Adder has an extensive variety of application are as follows:-

1. ALU- Arithmetic Logic Unit (one of the circuit is a full adder) to produce memory addresses inside a computer and to make the Program Counter point to next instruction, the ALU makes use of this adder.
2. For visuals correlated claims, wherever there is a actual considerable requirement of multifaceted calculations, the graphic processing unit uses optimized arithmetic logic unit which is made up of full adders, additional circuits as fine.

Basically, it is used in designing ALU and this ALU is used for wide variety of applications (from designing CPU to GPU).

II. DESIGNED STRUCTURE OF 1-BIT LOW POWER HYBRID FULL ADDER

3 sections are designed separately and by combining all sections low power full adder is implemented is as follows:-

Section 1

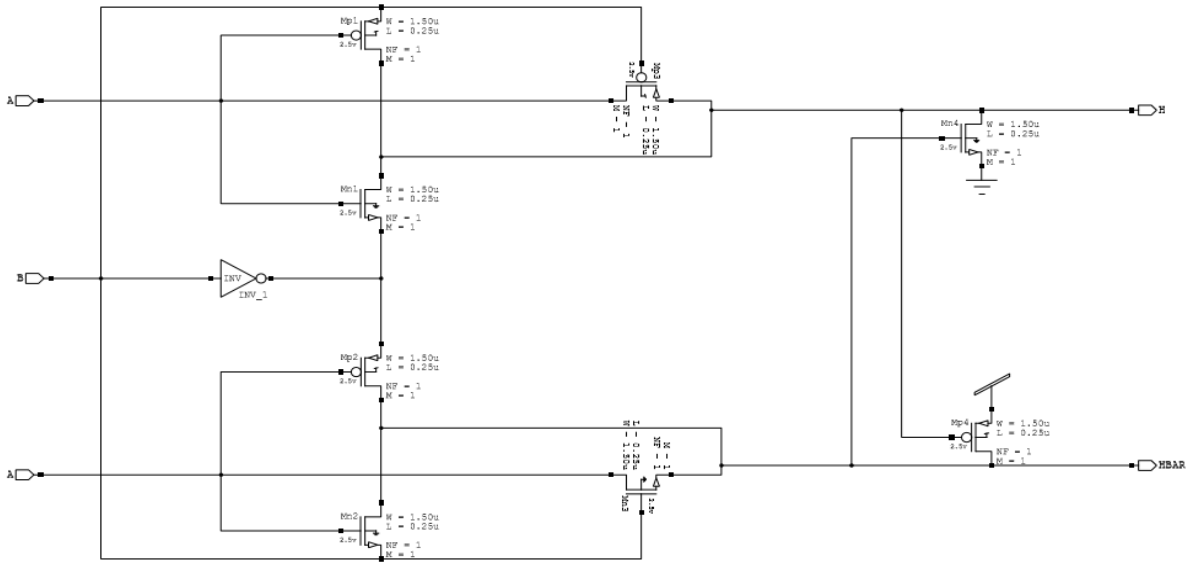

Figure 2:- CMOS logic for Section 1

In this section two subsection is added one is XOR section and other one is XNOR section and by combing those subsection (XOR and XNOR) a new (XOR-XNOR) prison cubicle is formed with one contribution buffer with input B & feedback loop is also inserted so that the error at the output end shall be reduced[1-4]. And when the above circuit is simulate and compare with other conventional full adder design the result of the transmission delay, power usage and pdp (power delay product) improved so much. This section is used to reduce power usage and pdp (power delay product) and production of full swing intermediate signal for other two sections[5].

Section 2

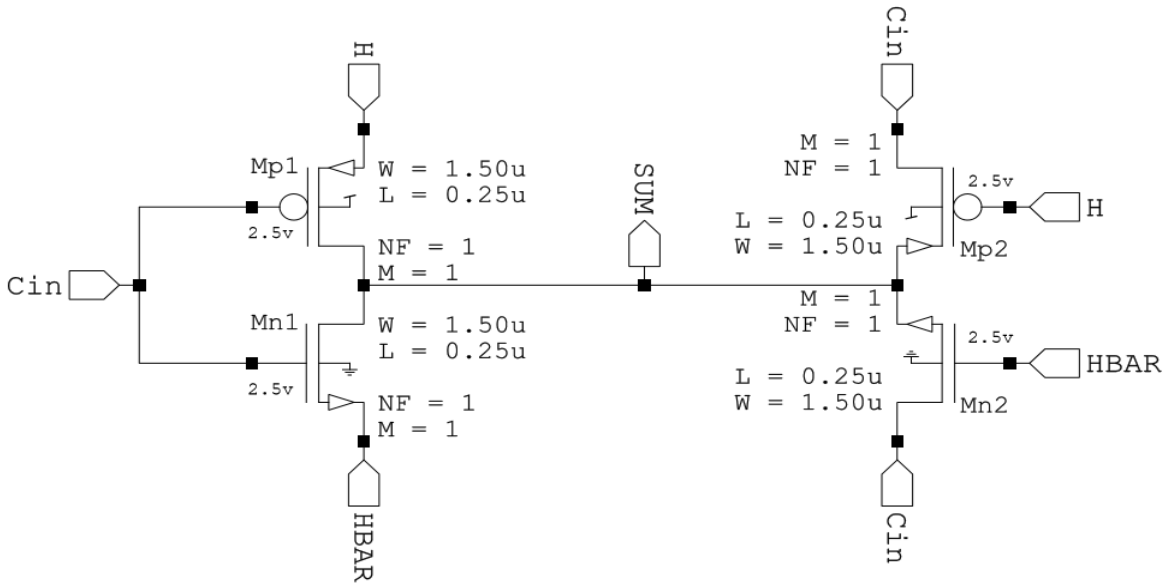

Figure 3:- CMOS design of Section 2

Section 3

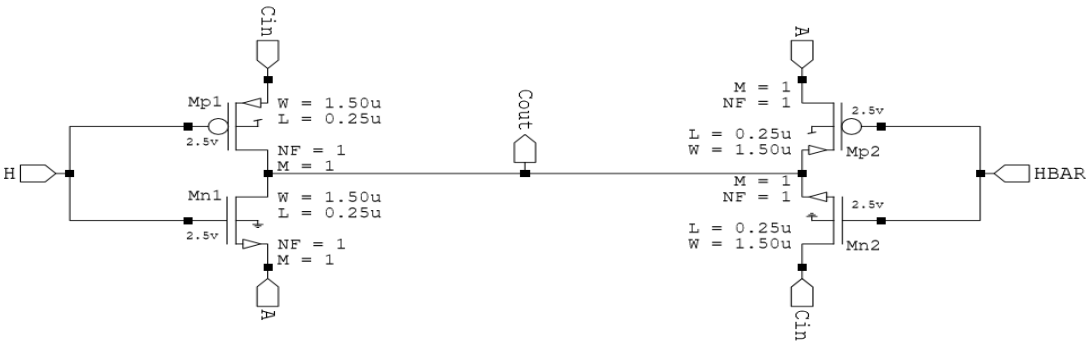

Figure 4:-CMOS design of Section 3

In Section 2 and Section 3, the full swing output signal is give by the Section 1. Section 1 & 2 are used to prevent the drop of threshold voltage below a particular level so that we can achieved the desired and improved output of adder.

III. LOW POWER HYBRID FULL ADDER BY COMBINING ALL SECTIONS

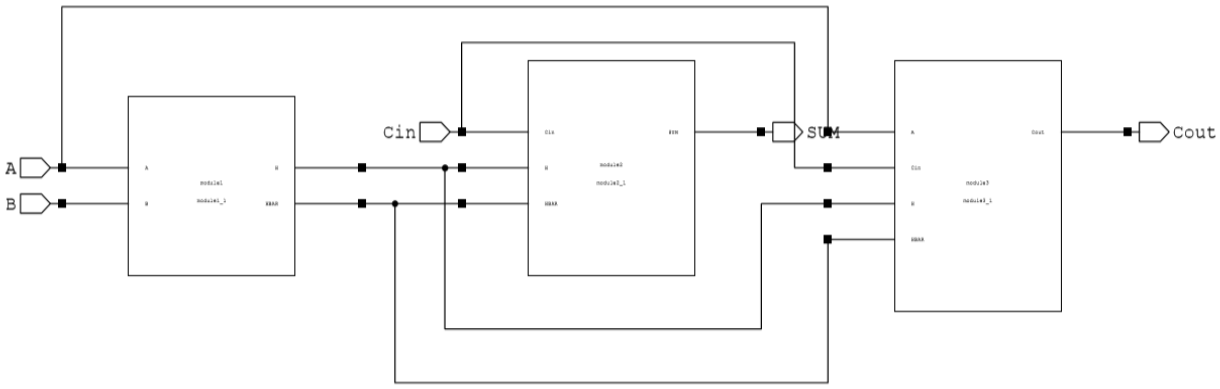

Figure 5:- Low power hybrid full adder by combining all sections

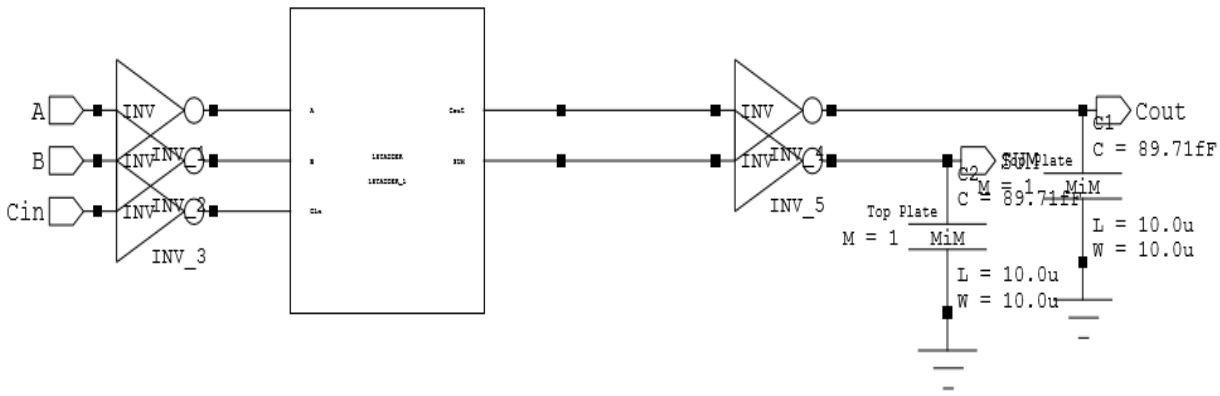

Figure 6:- Symbolic view of 1 bit low power hybrid FA(full adder)

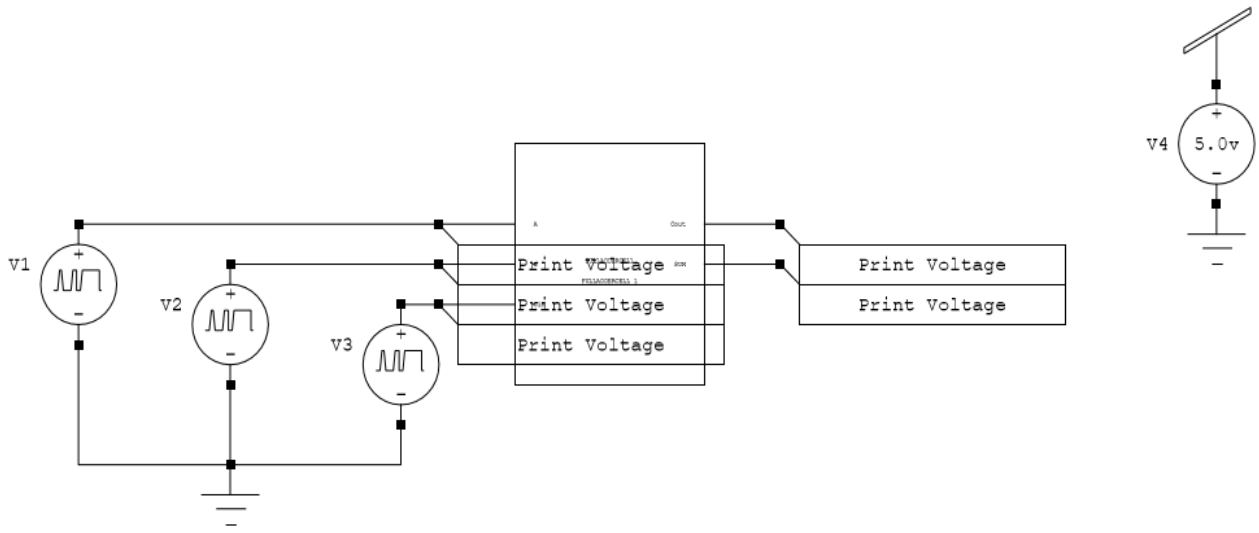

Figure 7:- Simulating design of an one bit low power hybrid FA (full adder)

IV. SIMULATION RESULT OF 1-BIT LOW POWER HYBRID FA(FULL ADDER)

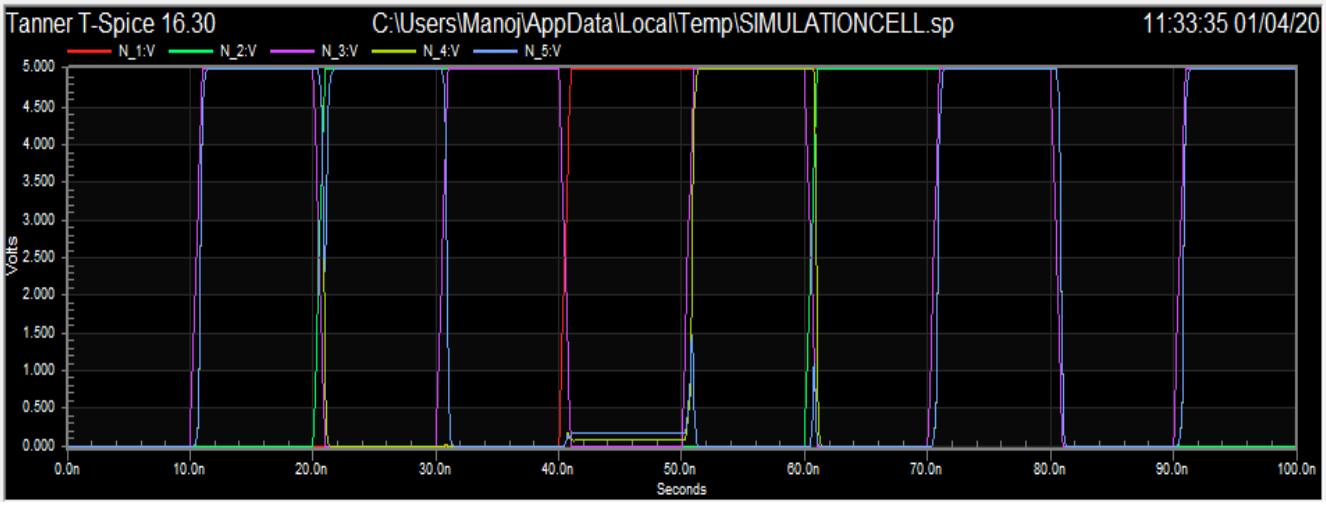

Figure:-8 Confined output of an one bit low power hybrid FA(full adder)

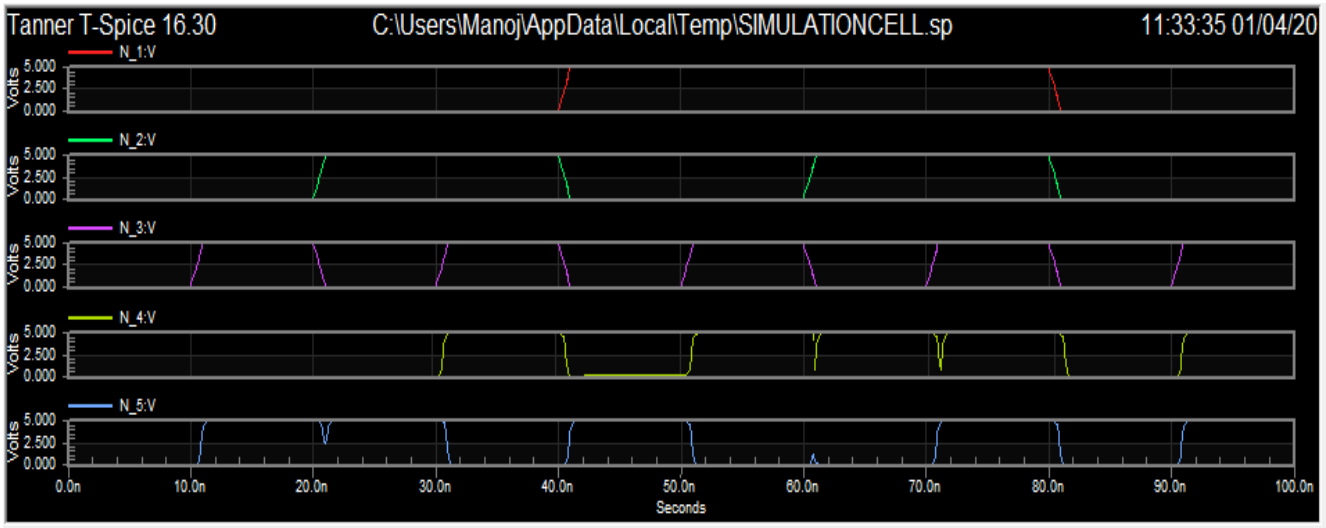

Figure:-9 Output of an one bit low power hybrid FA(full adder)

V. LAYOUT OF ONE BIT HYBRID FA (FULL ADDER) AT 90NM TECHNOLOGY

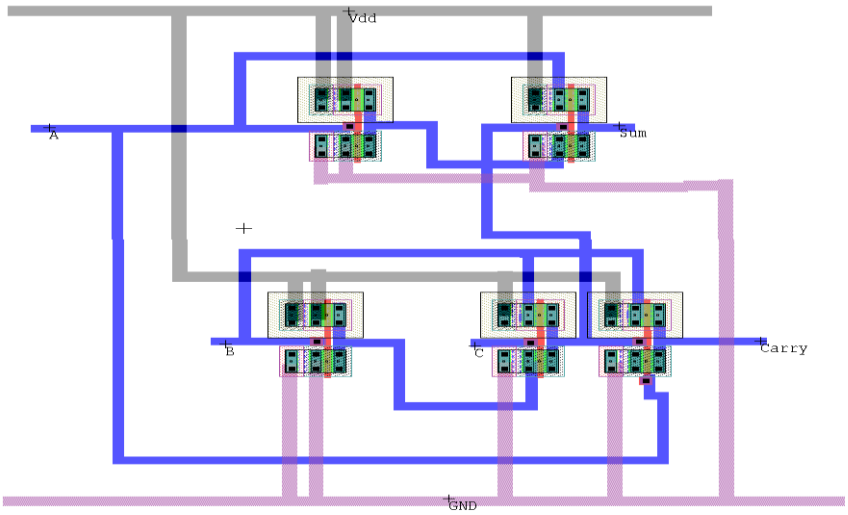

Figure:-10 Layout of one bit hybrid FA (full adder)

VI. RESULT ANALYSIS AND PERFORMANCE ASSESSMENT BETWEEN LOW POWER HYBRID ONE BIT FA(FULL ADDER) AND ONE BIT PRE DESIGNED FA(FULL ADDER)

Table 2:- Comparison of dynamic and static power of various adder circuit

Adder circuit	Static power	Dynamic power
CMOS	372.0 pw	6.1416 µw
CPL	1.379 nw	7.2183 µw
Hybrid	230.1 pw	3.9879 µw

Table 3:- Power usage , pdp(power delay product) and delay assessment of various pre designed FA(full adders) at various voltages in the absence of check bench in 90-nm technology

V_{dd}(volts)	0.5	0.7	0.9	1.1	1.19
Power usage (µW)					
C cmos	0.1956	0.4528	0.8329	1.453	2.447
HPSC	—	0.4143	0.7765	1.258	2.172
Hybrid	0.1543	0.353	0.6795	1.25	2.448
Hybrid cmos	0.2031	0.4377	0.811	1.492	2.664
Delay (Ps)					
C cmos	896.6	234.4	131.8	97.4	81.93
HPSC	—	163	97.97	72.98	60.66
Hybrid	546.6	164.6	99.83	75.82	75.5
Hybrid cmos	1558	256.6	95.89	60.62	46.94
Power-delay-Product (aJ)					
C cmos	175.374	106.136	109.776	141.522	200.482
HPSC	—	67.530	76.073	91.808	131.753
Hybrid	84.340	58.103	67.834	94.775	184.824
Hybrid cmos	316.429	112.313	77.766	90.445	125.048

Table 4:- Power usage ,pdp(power delay product) and delay assessment of various pre designed FA(full adders) at various voltages in accordance to check bench in 90 nano meter technology

V_{dd} (volts)	0.5	0.7	0.9	1.1	1.10
Power usage(μW)					
C cmos	0.371	0.8621	1.580	2.562	3.846
HPSC	—	0.9210	1.649	2.41	3.481
Hybrid	0.3201	0.7661	1.414	2.281	3.389
Hybrid cmos	0.3712	0.8429	1.529	2.447	3.647
Delay (Ps)					
C cmos	1078	270.1	157.6	107.9	89.53
HPSC	—	205.9	118.3	86.56	72.05
Hybrid	764.1	206.2	117.2	87.13	71.16
Hybrid cmos	2321	393.3	139.1	80.9	60.78
Power Delay Product (aJ)					
C cmos	391.020	231.263	234.590	274.910	344.332
HPSC	—	190.545	194.440	210.590	250.806
Hybrid	243.342	158.461	166.497	194.772	241.161
Hybrid cmos	846.139	331.090	213.504	200.1073	221.665

VII. CONCLUSION & FUTURE SCOPE

In that paper, one bit low power hybrid FA(full adder) electronic circuitry path is implemented & simulation had done successfully using EDA tool recording of various parameters is done and their comparison is done in accordance with various parameters with conventional full adders. These days full adders have wide range of applications so the consumption of power and delay have to reduce which can done by low power hybrid FA (full adder) as shown and comparison of low power full hybrid adder is done with various conventional adders circuit which shows that low power hybrid full adder had reduce the power usage, power delay product and delay.

Future work will include the reduction of power dissipation & area by reducing the numbers of transistors used for implementing the low power hybrid full adder.

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