

# New Algorithm for Dht and Its Verilog Implementation



Anamika Jain, Neeta Pandey

**Abstract:** This paper presents a new algorithm for computing Discrete Hartley Transform (DHT) (type-2) of  $N$  with  $N=4^r$ , where  $r>1$ . Paper also suggest VLSI architecture for the implementation of the newly developed algorithm. The computation of DHT using this algorithm is simple and requires less arithmetic operations compared with the general method for finding DHT. Also the suggested VLSI structure for the algorithm is regular and less complicated in terms of hardware requirement. Parallel processing of the algorithm make the processing further fast.

**Keywords:** Discrete Hartley transforms, recursive structure, Parallel processing.

## I. INTRODUCTION

Discrete Hartley transform is an orthogonal transform. Bracewell [1] introduced the DHT for a  $N$  point sequence, efficiently replace the corresponding DFT. In recent time researches in the field of digital signal processing shows keen interest in discrete Hartley transform. DHT find application in audio compression [2], Optical Spatial modulation [3], Watermarking [4], image compression techniques [5] and harmonic analysis [6-8] etc.

The DHT has the property of real number computation which is simpler than complex number operations in DFT. As the vast majority of applications involved only real valued data, significant performance gains are realized without much loss of generality. If one performs the complex DFT on an  $N$  point real valued sequence, the product is a complex sequence of  $2N$  real points of which  $N$  are redundant. The DHT, on the other hand, will yield a real sequence of the same length with no redundant terms, using only half the time and half the memory resources.

Also, all the properties applicable to DFT such as convolution and shifting theorem etc., apply to DHT as well. DHT is a linear and invertible transform. Thus; one can use a single program or a single architecture for both forward and inverse transform computation.

Apart from DFT, DHT outperform another orthogonal transform- discrete cosine transform (DCT),

which is the optimum fast transform for video compression application, for the images obtained using positron Emission Tomography (PET) and Magnetic Resonance Imaging (MRI) [9], and possibly for certain types of digitized radiographs. Also DCT can be derived from DHT through simple manipulations [10]. It is also interesting to note that the type-II, type-III and type-IV, DHT has the same definition as DW transform excepting the scale factor [11].

Computing DHT directly from its definition is too slow; restrict its use where the computational time is of great importance. Many algorithms were found in the literature to reduce the computation complexity, increasing the processing speed and their VLSI Implementation [12-17]. In this paper a new algorithm is presented in which a single structure with two multipliers and four adders used recursively to find DHT. Also, to simplify the computational complexity of DHT  $\text{Cos}(\cdot)$  function is used instead of  $\text{Cas}(\cdot) = \text{Cos}(\cdot) + \text{Sin}(\cdot)$  function. The number of multiplications for computing DHT of  $N$  point sequence using the general equation is  $N^2$ , which is reduced to  $(3/8)N^2$ , computation using new algorithm. This is less than half the no of computations required using general equation. Further HDL simulation and FPGA implementation of the suggested structure is presented. In this paper Verilog HDL simulation has been carried out and the results are discussed.

The content of this paper is structured as follows: the next section shows the mathematical formulation for the DHT. Section-III presents architecture for the proposed algorithm, Verilog simulation of the proposed algorithm is shown in Section IV. Simulation results and final conclusion of the work are summarized in Section-

## II. ALGORITHM FORMULATION FOR DHT

The generalized Discrete Hartley Transform (DHT) is defined for sequence  $x(n)$  of length  $N$  by the following equation.

$$X[k] = \sum_{n=0}^{N-1} x(n) \text{Cas} \left( \frac{2\pi nk}{N} \right) \quad (1)$$

And the inverse transform can be defined as

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X[k] \text{Cas} \left( \frac{2\pi nk}{N} \right) \quad (2)$$

Where  $\text{cas}(\cdot) = \text{cos}(\cdot) + \text{sin}(\cdot)$

The transform is linear and its coefficients are real. It can be observed that both forward and inverse transformations can be computed with the same kernel except the constant multiplication.

**Revised Manuscript Received on February 28, 2020.**

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Equation (1) can be decompose

$$X[k] = \sum_{n=0}^{\frac{N}{4}-1} \left[ x(n) \text{Cas}\left(\frac{2\pi nk}{N}\right) + x\left(n + \frac{N}{4}\right) \text{Cas}\left(\frac{2\pi\left(n + \frac{N}{4}\right)k}{N}\right) + x\left(n + \frac{N}{2}\right) \text{Cas}\left(\frac{2\pi\left(n + \frac{N}{2}\right)k}{N}\right) + x\left(n + \frac{3N}{4}\right) \text{Cas}\left(\frac{2\pi\left(n + \frac{3N}{4}\right)k}{N}\right) \right] \quad (3)$$

Further, CAS (.) can be written as Cos(.)+Sin(.

$$X[k] = \sum_{n=0}^{\frac{N}{4}-1} \left[ x(n) \left( \text{Cos}\left(\frac{2\pi nk}{N}\right) + \text{Sin}\left(\frac{2\pi nk}{N}\right) \right) + x\left(n + \frac{N}{4}\right) \left( \text{Cos}\left(\frac{\pi k}{2}\right) \text{Cos}\left(\frac{2\pi nk}{N}\right) - \text{Sin}\left(\frac{\pi k}{2}\right) \text{Sin}\left(\frac{2\pi nk}{N}\right) \right) + x\left(n + \frac{N}{2}\right) \left( \text{Cos}(\pi k) \text{Cos}\left(\frac{2\pi nk}{N}\right) - \text{Sin}(\pi k) \text{Sin}\left(\frac{2\pi nk}{N}\right) \right) + x\left(n + \frac{3N}{4}\right) \left( \text{Cos}\left(\frac{3\pi k}{2}\right) \text{Cos}\left(\frac{2\pi nk}{N}\right) - \text{Sin}\left(\frac{3\pi k}{2}\right) \text{Sin}\left(\frac{2\pi nk}{N}\right) \right) \right] \quad (4)$$

$$X[k] = \sum_{n=0}^{\frac{N}{4}-1} \left[ x(n) \left( \text{Cos}\left(\frac{2\pi nk}{N}\right) + \text{Sin}\left(\frac{2\pi nk}{N}\right) \right) + x\left(n + \frac{N}{4}\right) \left( \text{Cos}\left(\frac{2\pi nk}{N}\right) (-1)^{\lfloor k/2 \rfloor} + \text{Sin}\left(\frac{2\pi nk}{N}\right) (-1)^{\lceil k/2 \rceil} \right) + x\left(n + \frac{N}{2}\right) \left( (-1)^k \text{Cos}\left(\frac{2\pi nk}{N}\right) + (-1)^k \text{Sin}\left(\frac{2\pi nk}{N}\right) \right) + x\left(n + \frac{3N}{4}\right) \left( \text{Cos}\left(\frac{2\pi nk}{N}\right) (-1)^{\lceil k/2 \rceil} + \text{Sin}\left(\frac{2\pi nk}{N}\right) (-1)^{\lfloor k/2 \rfloor} \right) \right] \quad (5)$$

With  $k = 4p + q$ , and mathematical manipulations above equation (5) can be written (using cas(.) function ) as:

$$X[4p + q] = \sum_{n=0}^{\frac{N}{4}-1} \left[ \left( A + (-1)^q C \right) \text{Cas}(\theta + q\phi) + ((-1)^{\lfloor q/2 \rfloor} B + (-1)^{\lceil q/2 \rceil} D) \text{Cas}((-1)^q (\theta + q\phi)) \right] \quad (6)$$

$$X[4p + q] = \sum_{n=0}^{\frac{N}{4}-1} \left[ \left( A + (-1)^q C \right) \text{Cas}(2\pi nk / N) + ((-1)^{\lfloor q/2 \rfloor} B + (-1)^{\lceil q/2 \rceil} D) \text{Cas}((-1)^q 2\pi nk / N) \right] \quad (7)$$

Where

$$x(n) = A, x\left(n + \frac{N}{4}\right) = B, x\left(n + \frac{N}{2}\right) = C \text{ and } x\left(n + \frac{3N}{4}\right) = D$$

and  $k = 4p + q$ , where  $q=0, 1, 2, 3$  and  $p$  varies from 0 to

$$(N/4)-1 \text{ also taking } \theta = \frac{8\pi nk}{N}, \phi = 2\pi m / N$$

(Using cos (.) function) equation (5) can be written as:

$$X[4p + q] = \sqrt{2} \sum_{n=0}^{\frac{N}{4}-1} \left[ \left( A + (-1)^q C \right) \text{Cos}(\pi / 4(8\pi nk / N - 1)) + ((-1)^{\lfloor q/2 \rfloor} B + (-1)^{\lceil q/2 \rceil} D) \text{Cos}((-1)^q (\pi / 4(8\pi nk / N) + 1)) \right] \quad (8)$$



Separating the above equation for even and odd values of  $q$

Case I: For even  $q$  ( $q=0, 2$ )

The equation becomes

$$X[4p + q] = \sqrt{2} \sum_{n=0}^{N/4-1} \left[ \begin{matrix} (A + (-1)^q C) + (-1)^{q/2} \\ (B + (-1)^q D) \cos(\pi / 4((8nk / N) - 1)) \end{matrix} \right] \quad (9)$$

Case II: For odd  $q$  ( $q=1, 3$ )

$$X[4p + q] = \sqrt{2} \sum_{n=0}^{N/4-1} \left[ \begin{matrix} (A + (-1)^q C) \cos(\pi / 4((8nk / N) - 1)) + \\ (-1)^{q+3} (B + (-1)^q D) \\ \cos(\pi / 4((8nk / N) + 1)) \end{matrix} \right] \quad (10)$$

Equations (9) and (10) represent the final solution for DHT, where any coefficient of DHT can be computed independently through these equations. These equations can be realized in hardware structure which is shown in the next section.

### III Proposed Architecture for DHT Computations

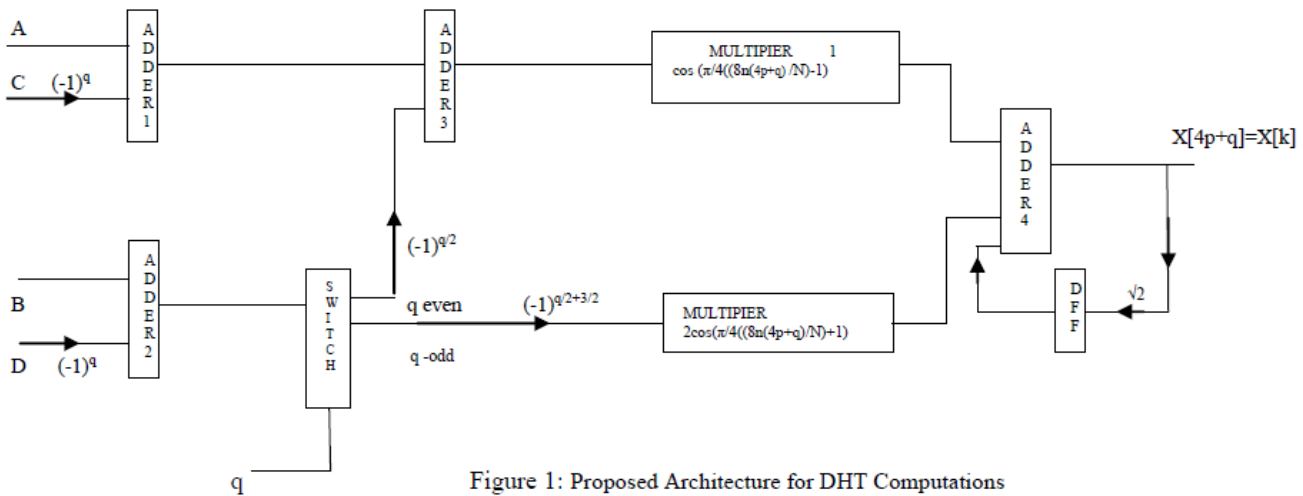


Figure 1: Proposed Architecture for DHT Computations

The Algorithm is realized in hardware through the architecture proposed in the figure 1. In this architecture the inputs are added in a particular order depending upon the value of  $q$ . Here, inputs  $x(n), x(n+N/4), x(n+N/2)$  and  $x(n+3N/4)$  are defined as A,B,C and D respectively and the DHT coefficients  $X[k]$  are defined as  $X[4p+q]$ , where  $p$  varies from  $\{0 \text{ to } (N/4)-1\}$ , and  $q$  have four values  $\{0,1,2,3\}$ . The added output is then multiplied by a factor  $(\cos(\pi/4((8nk/N)\pm 1))$ , depending upon the even  $\{0,2\}$  and odd  $\{1,3\}$  values of  $q$ . For even values of  $q$ , only one multiplier is required to find the value of DHT coefficient and for odd values of  $q$  two multipliers are required to find DHT coefficients. Due to the very regular and modular structure of the algorithm, a 16 point DHT architecture can also be used for any value of input  $N=4^n$ .

For example, when  $q=0$  and  $p=1$ , A and C inputs are added through adder1 and B and D inputs are added in adder2. As  $q$  is even,  $A+C$  and  $B+D$  are added in adder3 then the resultant is multiplied by a multiplier 1. This procedure is repeated for  $n=1,2,\dots,N/4$  times and added through adder4, then final coefficient value  $X[4]$  is obtained. So for computing one coefficient  $N/4$  computation cycles are needed. Similarly, we can compute any coefficient of DHT. Four such structures can be connected in parallel to get four coefficients simultaneously. using parallel processing data throughput is increased to 4 times.

### III. RESULTS

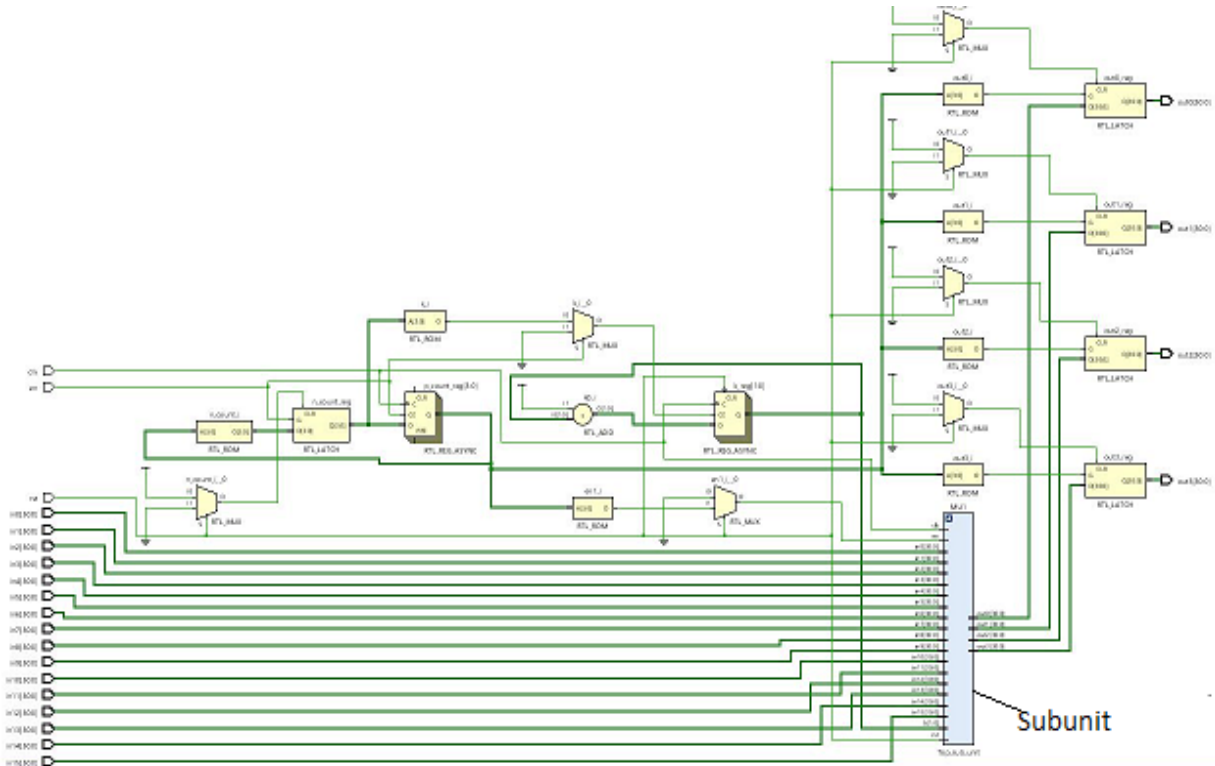
The proposed architecture described above have been implemented in Verilog using Vivado 2018.3. FPGA board used for the same was ZedBoard Zynq Evaluation and Development Kit. Table 1 presents the synthesis results if the proposed architecture. The multiplications are implemented on the dedicated DSP slices (DSP 48E1). Those slices combine high speed with small size, while retaining system design flexibility. The DSP slices enhance the speed and efficiency of many applications in digital signal processing. Some part of the programming is reported in the Appendix. One of the main advantages of the proposed algorithm consists in the possibility to compute it in parallel system. The presented structure is implemented for a sequence of length  $(N = 16)$  as shown in Figure 2. As can be seen in RTL schematic diagram 16 inputs has been taken in the input unit section and 4 outputs have been assigned in output units 1,2,3, and 4 respectively. For parallel processing, subunit block uses four such structures which are shown in figure 1. After parallel processing four coefficients can be obtained simultaneously through the output units. Output unit sections will provide  $X[0], X[4], X[8], X[12]$  coefficients simultaneously.



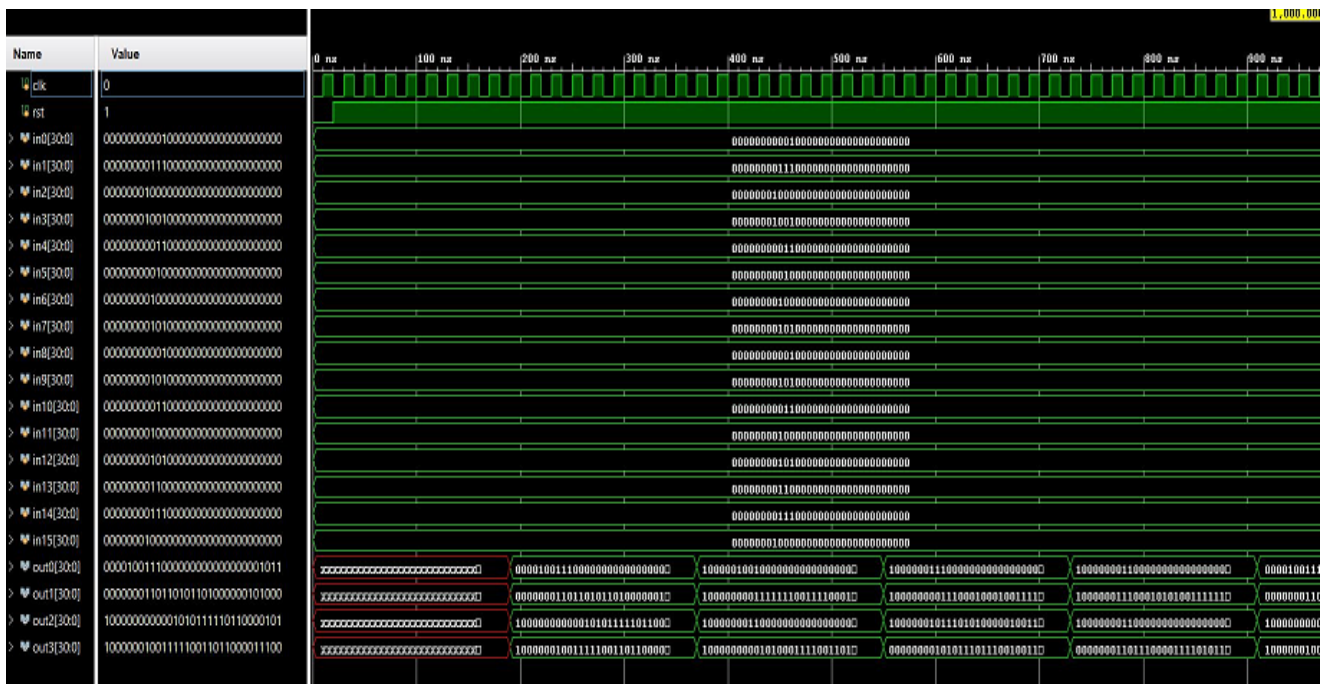
## New algorithm for DHT and Its Verilog Implementation

In the next cycle another set of coefficients are obtained  $X[1]$ ,  $X[5]$ ,  $X[9]$  and  $X[13]$  depending on the value of  $p$  and  $q$ . Similarly, all the coefficients can be obtained in the consecutive clock cycles. Four structures are implemented in parallel such that each unit gives 4 coefficients for  $N=16$ . For input sequence  $X = [1, 7, 8, 9, 3, 2, 4, 5, 1, 5, 3, 4, 5, 6, 7, 8]$ , outputs  $Y = [78, 13.6758, -0.3431, -9.9507, -18, -3.9761, -6, -1.2797, -14, -3.5337, -11.6568, 5.4654, -5.9999, -14.1660, -6, 13.7650]$

were obtained as seen in the simulation diagram in figure 3. Total of 45 clock cycles were required to obtain all 16 coefficients at output. The results obtained were verified using the MATLAB code and it was found that the obtained result was nearly equal to the desired result, that is,  $Y = [78, 13.6758, -0.3431, -9.9507, -18, -3.9761, -5.9999, -1.2797, -14, -3.5337, -11.6568, 5.4654, -5.9999, -14.1660, -6, 13.7650]$ .



**Figure 2: RTL schematic of the proposed architecture for DHT computations for  $N=16$**



**Figure 3: Timing Diagram of the simulated results for  $N=16$**



**Table 1. Summary of slice utilization**

Top_Unit	Utilized	Available	Utilization
Slice LUTs	9166	53200	17%
DSPs (DSP 48E1)	182	220	82.70%
Bonded IOB	6	200	3%
BUFGCTRL	3	32	9.30%
Slice Registers	2285	106400	2.10%
Slice	3156	13300	23.70%
LUT as Logic	9166	53200	17.20%

**IV. CONCLUSION**

In this paper a new algorithm is proposed for the computation of Discrete Hartley Transform with reduced number of computation compared to general method. A corresponding architecture of the algorithm is also presented which requires only 4 adders and 2 multipliers. Main advantage of the algorithm that any desire coefficient can be computer independently and the proposed structure can be connected in parallel for getting more throughput. Simulation of the architecture is done using Verilog HDL and implementation is performed using Vivado 2018.3 Evolution and Development kit. The proposed architecture has been implemented in a parallel using low hardware resources.

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