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Throughput Enhancement of Continuous Time Replication Strategy using Multicast GALS in NoCs

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Abstract: ***The network-on-Chip (NoC) design is the modern development in communication as the integration of the multiple network blocks in a single chip. Before the NoC, system on chip (SoC) was implemented. Development in the day to day the features were added to overcome the SoC like potential of the system on chip, operation frequencies, wiring congestion and size of the chip etc., as the SoC has the long sensitive path which shows the impact on the size of the chip. In wiring congestion: Routing a particular data with SoC requires lot of wirings. Coming to the NoC also developed in packet transferring from source to destination. Serial communication were first used to transfer as it take much time to transfer the data packets from the source to destination to overcome the serial path communication, parallel communication is used. In Parallel communication the packets are transferred from source to destination at a time. To improve the packet transfer in network many techniques are used like mesh topology, tree topology etc. The existing system will supports only the mesh topology and one to many packet transfer. In the proposed system, the new parallel multicast which uses the Globally Asynchronous and locally Synchronous Network on Chip (GALS NoC) that includes both Synchronous and Asynchronous Transmission with a slight change in IPM and OPM Architecture to support both synchronous and asynchronous transmission and reception of data packets. It has several advantages like it supports efficient many-to-one traffic, it is suitable for any topology and has improved Throughput.***

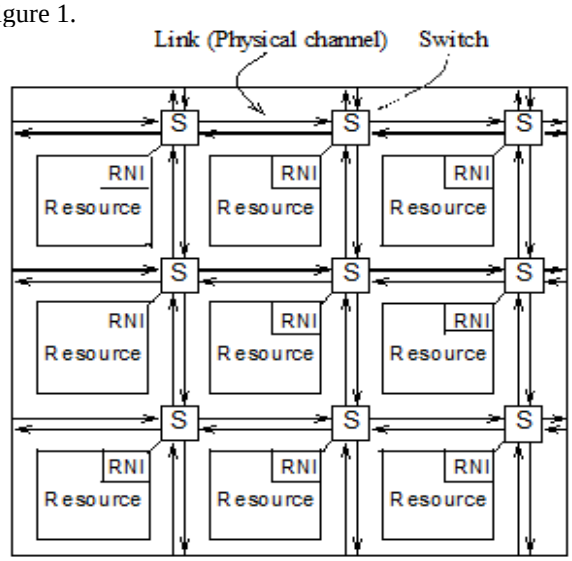
Keywords: **Asynchronous circuits, multicast communication, networks-on-chip (NoCs).**

I. INTRODUCTION

In day to day improvement in the technology leads to improve in the existing system in communication level. To increase the chip capability more circuits are added in a single chip, the SoC is the System-on-Chip which is used earlier then the NoC, were NoC uses the SoC platform but, compare to the SoC the NoC is complex design and high speed chip which can handle more network than the SoC. NoC chip size is reduced and wiring connections are also decreased. SoC will works under the principle of TC protocol that is connection oriented protocol. When the packet is to be transferred transmitter will sends the sync pulse and receiver gives the response of Ack and transmitter will sends the data packets.

Network-on-Chip as a SoC Platform

NoC was introduced in the year 2001 in the SoC community. The mesh structure composed of switches with every resource is connected to exactly one switch, as shown in Figure 1.



(source: Zhonghai Lu, Design and Analysis of On-Chip Communication.)

Figure 1.Mesh NoC with 9 nodes

As shown in Figure 1 all the resources are placed on slots which forms the switch. The resources can be a memory, procesor, IP blocks or any network. The resource will use only the routing technology to transfer the packets without using any wires to perform the task. This NoC uses the parallel communication mechanism and it is designed for the closed system. It has the application like peer-to-peer connection and multicasting, telephony network is also a NoC based design which is used for the communication purpose in voice communication, video and data transfer. Because of the micro network is built on single chip it can have wide parallel wires and allow high rate synchronous clocking by this the area and the power are also reduced. In communication data and timing are the main concern issue were the time is measured in nanoseconds. SoC have the limited space and it is expensive buffering compare to the local area network and wide area network. The power consumption in the NoC uses the less power by this the battery life will increases in the embedded applications.

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Communication-centric [11]: When the packets are transferred from one block to the other, networking IP module is partitioned chip will gives the parallel communication ,were all the modules are integrated separately and clock cycles are used independently by the every module. This gives the packet transfer will be done parallel to all modules at a time. Parallel communication will reduce the power and the architectures permits sequential process. The design space for every module will be sufficient and quality of service (QoS) is performed.

Globally Asynchronous Locally Synchronous

A promising option for dealing with such design challenges is the deployment of globally asynchronous, locally synchronous (GALS) systems. A GALS system consists of complex digital blocks operating synchronously. This model uses asynchronous signaling between different clocked units on a chip. Every clocked signal is surrounded by an asynchronous wrapper that takes care of the signaling between the different clocked parts. Since the design of the asynchronous wrapper is much easier than designing a whole asynchronous system and the problem of clock-skew is much smaller some of the benefits of asynchronous design are gained without having to get rid of the D-flip-flops.

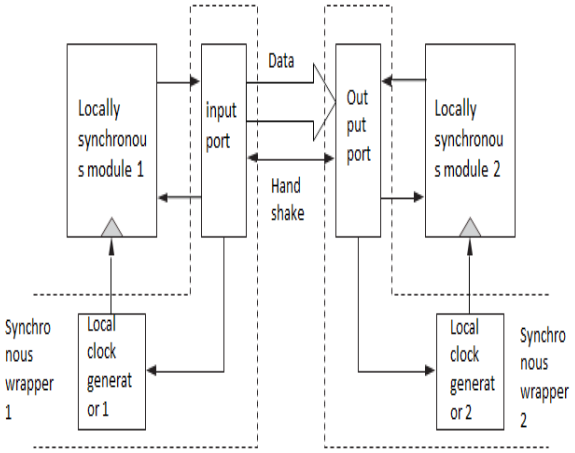
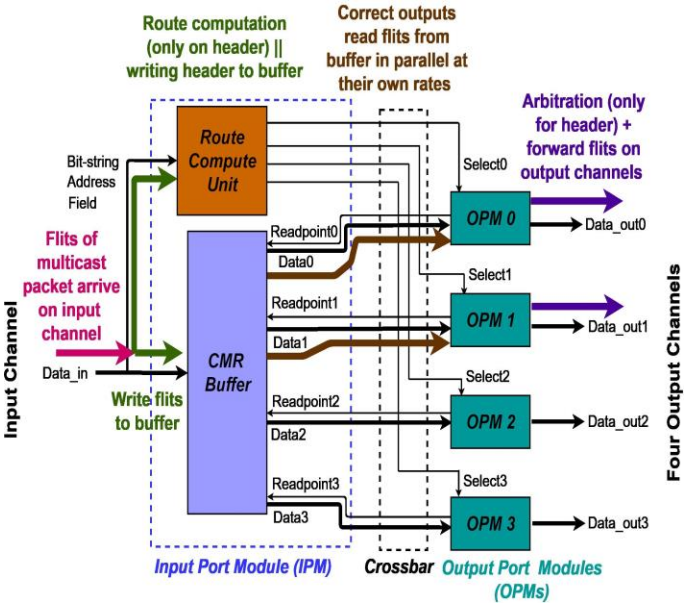


Figure 2: Globally Asynchronous, Locally Synchronous (GALS) System

Different blocks can also use different clock-frequencies. This could also decrease the design time, since the circuits which are not used regularly can use a lower clock frequency.



(Source:KshitijBhardwaj ,M.Nowick,Fellow , IEEE.)

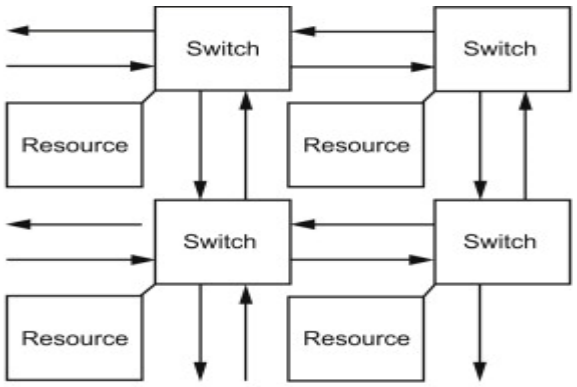
Figure 3: Tree based multi cast continuous time replication strategy

If the clock period is optimized to be as long as possible for every block, power consumption will also be lower, as every block can work at low clock frequency as possible. Figure.2 shows the GALS system and Figure 3 shows the Tree-based multi-casting Continuous-Time Replication Strategy.

II. EXISTING SYSTEM

Serial path based mesh network Multicast NOC

In serial path-based multicast packets are routed serially from source to first destination and to next and so on until the last destination. Packet transformation from source to destination in serial path based multicast is simple but it can gain significant latency overheads for a large number of destinations.



(Source**:** Marilyn wolf, in High-Performance Embedded Computing)

(a) Figure 4: Serial path based mesh network Multicast NOC

(ii) Parallel tree based multipath NoC

In tree-based multicast packets are first routed in a common path from source to all destinations. When this common path ends, the packet is deviated and replicated.as though this method is used widely but it has a disadvantage that is the new packets also follow an algorithmic tree approach, repeating multiple times to achieve the destinations as shown in the fig.5.

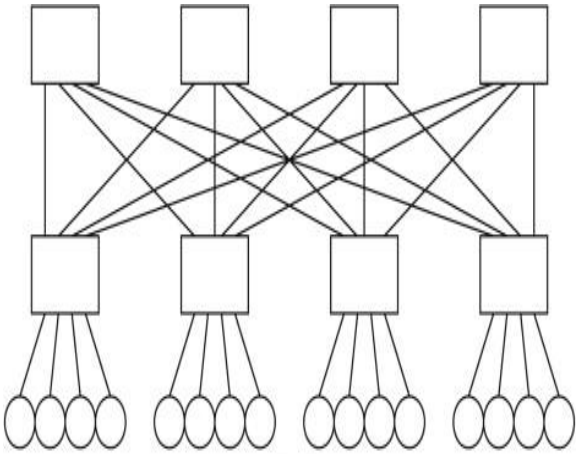
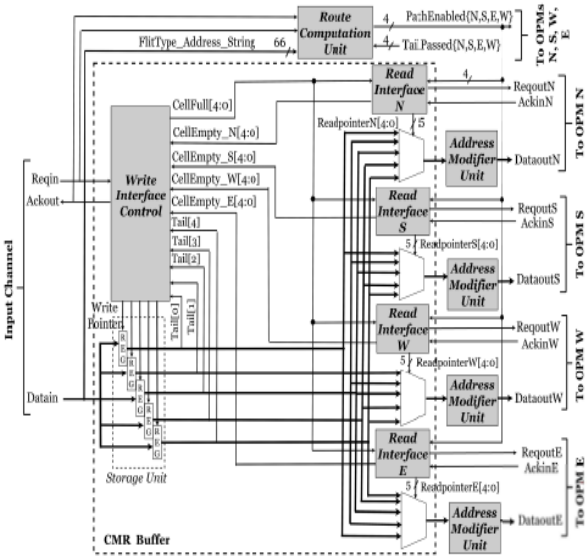


Figure 5: Parallel tree based multipath NOC.

It is typically widely used high-performance or superior design of NOC.

In previously for work set up tree is used in advance using multiple unicasts however recent works don't use unicast-based set up: tree made dynamically.

The new design contains the new Input Port Module (IPM) design that supports the continuous-time replication strategy, along with the details on its Route Computation Unit (RC) and the Continues time Multiway (CMR) Reads buffer as shown in fig. 6.



(Source:KshitijBhardwaj ,M.Nowick,Fellow , IEEE.)

Figure 6. IPM micro architecture with CMR buffer.

The parallel multicast asynchronous NoCs is introduced to exploits asynchronous NoCs which justifies a critical architectural and enabled advanced computing systems. But still it has a disadvantage that is suited only for Mesh Topology and one to many packet transfer.

By adding the GALS system in an input module in CMR buffer to support both synchronous and asynchronous transmission and reception of data packets which uses Continuous time replication methodology, where the flutters of a multicast packets are directed through the unique yields of the switch as indicated by each yield's own rate, in parallel, and in nonstop time. If the clock period is improved to be as long as possible for all block, power consumption will be lower, as all block can work at low clock frequency at the same time the delay is reduced.

III. PROPOSED METHOD

The Multicast Globally Asynchronous and locally Synchronous Network on Chip (GALS NoC) that includes both Synchronous and Asynchronous Transmission with a slight change in IPM and OPM Architecture to support both synchronous and asynchronous transmission and reception of data packets. It has several advantages like it supports efficient many-to-one traffic, it is suitable for any topology. Hence it will improves the throughput of NoC.

The continuous time replication strategy sends the multicast packet over the different output ports in parallel and at each output's own rate and it is used only for the mesh topology and tree topology to overcome this GALS system is used.

To create a GALS system the programmable ring oscillator are required which is inexpensive solution. Whenever the transfer of the packets between the two blocks to an receiver it uses peer- to-peer communication, whereas the data receiver clock will stops the packets this is occur due to the problem of the synchronization of the two clocks. This synchronization problem can be avoided by adding the two techniques they are:

1. Boundary Synchronization and
2. FIFO solution.

If we use the boundary synchronization solution it increases the Latency and throughput well be reduced this is happens because of boundary synchronization uses delayed latches. Figure 7 shows the FIFO based GALS system.

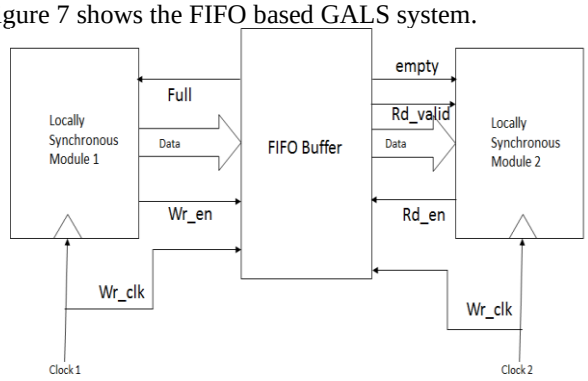


Figure7: FIFO based GALS System

By adding the FIFO buffer block it has the interface of synchronous-synchronous and asynchronous-asynchronous interface this can be improve the throughput. Implementation of FIFO system will not affect the local synchronous operation. The high performing processors will uses more clock cycles it leads the more power consumption so, by sub-dividing the blocks in the local synchronous blocks uses the clock cycles only when the data transfer occurs.

IV. SIMULATION RESULTS

The designs are modelled in Verilog HDL and are functionally verified by using Xilinx ISIM Simulation Tool. The designs are synthesized for Spartan3E FPGA by suing Xilinx ISE 14.5 Tools for the device XC3S500E with a package of FG320 and a speed grade of -5.

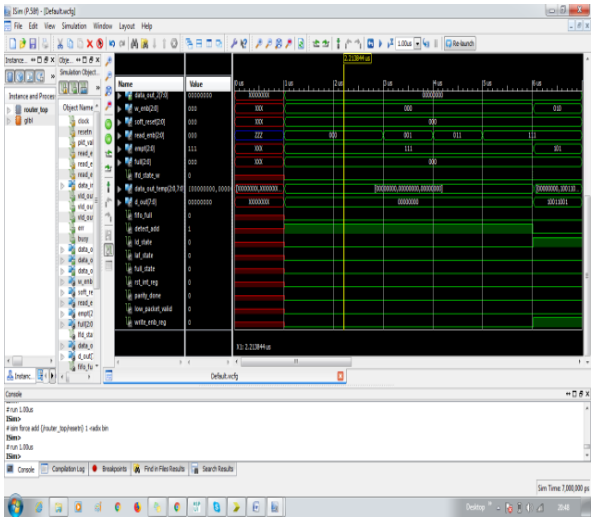


Figure8: Simulation results of proposed system

The simulation waveform of Proposed Router that supports both synchronous and asynchronous routing in NOC is shown in above figure where clearly the packet is routed to every other node. It is observed that many signals considered to show the response of the system, such signals are clock, resetn, pkt_valid, read_enb_0, read_enb_1, read_enb_2, data_in, vld_out_0, vld_out_1, vld_out_2, err, busy, data_out_0, data_out_1, data_out_2.

Here clock is used for synchronous and asynchronous the circuit. Reset signal acts as an input signal to reset the all operations of the design. Packet valid signal is used to validate the operation. Read operation is asserted by the read enable signal. Data input signal having input data these data will be presented in the output signal as per the operation when reset is low and read enable signal is in high. The data out signal carried the output data. Busy signal is asserted when if second data input coming while on processing of first data input. This design is converted to register transfer logic by the Xilinx synthesizer.

Fig 8. Shows that the simulation results prove that the data is stored in temporary file and produced in the next cycle. Here simulation results cleared that during first clock cycle some data stored in data_out_temp (temporary signal) then during next clock cycle same data appeared in the data out signal.

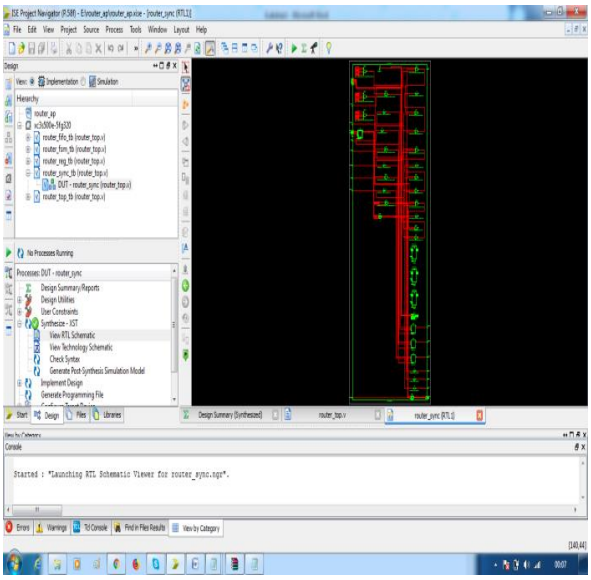


Figure 9: RTL Schematic of Proposed NOC Router

The figure.9 shows that the RTL Schematic of the Proposed NoC Router. It is cleared that the Logic gives the register transfer logic of the devised logic by using primitive logic.

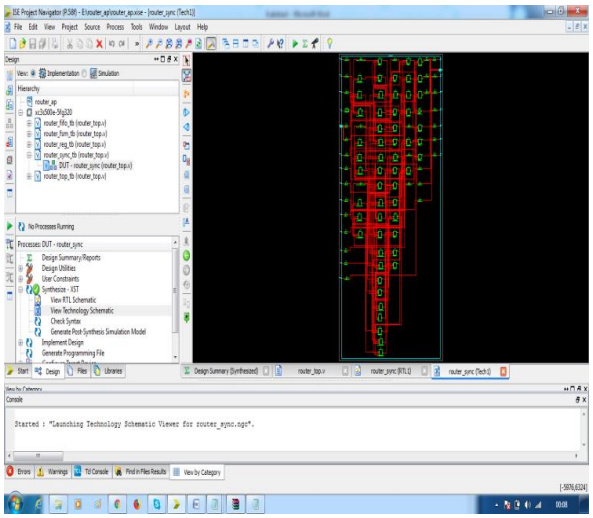


Figure 10: Technology Schematic of Proposed NOC Router

The figure.10 shows that the Technology Schematic of Proposed NOC Router. It is clear that the technology schematic gives the mapped logic to 90nm CMOS technology as look up tables.

The figure.11 shows that the Input and output power analysis of Proposed NOC. It is clearly shows that the power drawn by Input/output's is 3.14 micro watts for an operating frequency of 5 MHz and 12.5% toggle ratio.

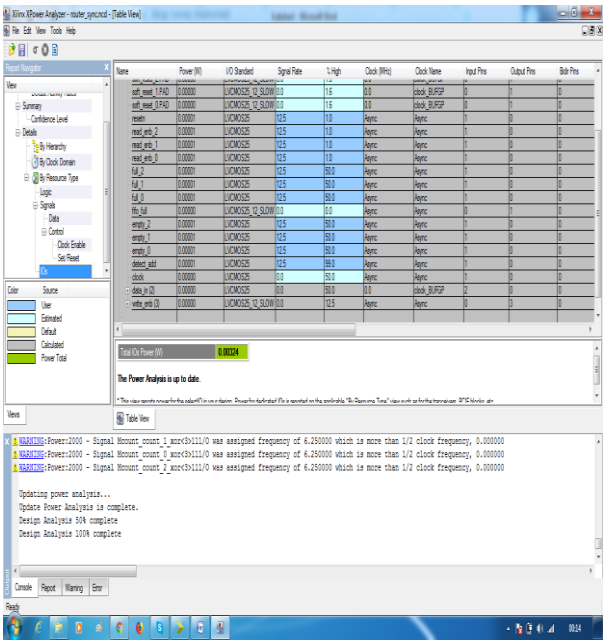


Figure 11: Input and output power analysis of Proposed NOC.

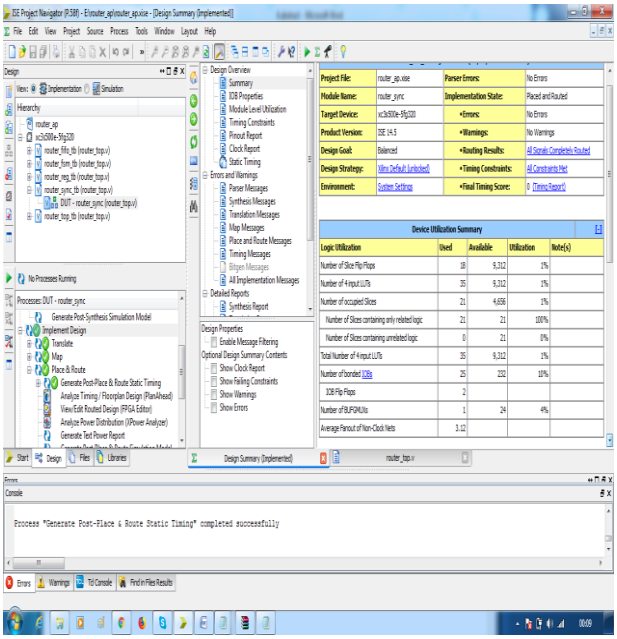


Figure 12: Design summary after implementation of NoC

The figure 12 shows Design summary after implementing of NoC. This shows the number of devices utilization summary , Here the number of slices which is available is 4656 and the used is 21 the total utilization is 1% as well as the number of slice flip-flops used is 18 outoff 9312 that can be represented as 1% and the 4 input LUTs uses 35 devices outoff 9312 it gives 1% utilization and IOB attributes are the true attribute to output flip-flop .That is 25 used and available is 232 flip-flops total utilization is 10% and Global clock(GCLKs) available is 24 and only 1 global clock is used. The average fanout of non-clock is 3.12 and the , this all the above devices are designed that gives the implementation of new NoC design summary.

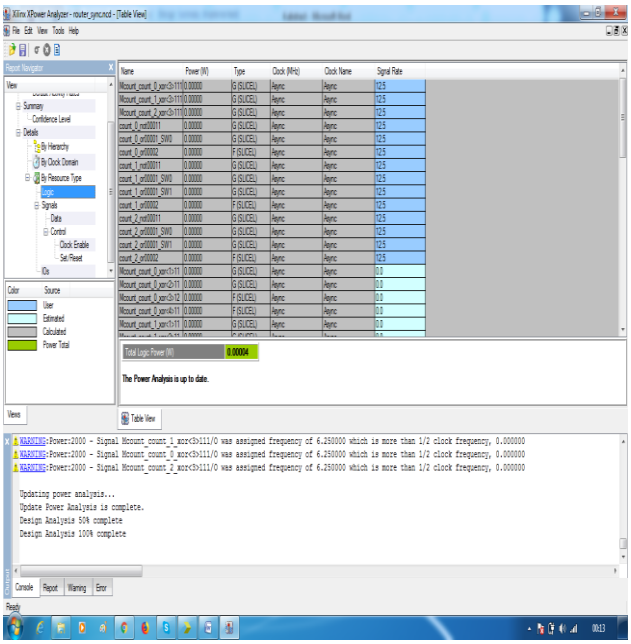


Figure 13: Signal Data power of NoC using GALS system.

The figure 6.9 shows Signal Data power of NoC using GALS system. Here the maximum power used by the devices which are connected internally, to transfer the data is given by total data power of overall system is 0.00002W, by this we can conclude that the signal data power is reduced by 0.00007W to 0.00002W.

Table - I: Comparison Table of NOC Routers

Parameter	Tree Based Multicast NoC Design	IPM and OPM Based Multicast NoC Design	Proposed Multicast NoC Design
No. of slices	485 out of 4656	16 out of 4656	19 out of 4656
No. of 4-input LUTs	481 out of 9312	31 out of 9312	45 out of 9312
Combinational Path Delay	8.153ns	-	6.031ns
Average Fanout	3.87	2.90	3.12
Logic Power	0.00002	0.00004	0.00004
Signal Data Power	0.00008	0.00007	0.00002
I/O Power	0.00315	0.00843	0.00324

Compare to the existing system multicast NOC design the four input lookup table uses 45 lookup tables out of the 9312 lookup tables .The transmission delay of the circuit is reduced to 8.153ns to 6.031ns. The output of a single logic gate can feed the 3.12 number of digital input this called as Fanout of the system it is increased compare to the existing system. Signal data power is reduced from 0.00007 to 0.00002 and the input output power is reduced by 0.00843 to 0.00324 by this results we can conclude that that the average fanout of the data is increased and data power reduced by 71.4%, input output power is reduced by 61.1% and also the delay reduced by 26% so that the throughput is increased.

V. CONCLUSION

The new traffic patterns which uses Parallel multicast asynchronous NoC with a 2-D mesh topology, where the multicast packet are routed through the distinct outputs of the router according to the output's and its own rate in parallel with continuous time. A new Continues time Multiway Read buffer is used to enable this strategy. This paper includes, using the asynchronous NoC show some estimated cost benefits to build a GALS system and performing system-level evaluation and supporting many-to-one traffic and it is also suitable for any topology and has improved Throughput. By adding the GALS system in an input module in CMR buffer to support both synchronous and asynchronous transmission and reception of data packets which uses Continuous time replication methodology, where the flutters of a multicast packets are directed through the unique yields of the switch as indicated by each yield's own rate, in parallel, and in nonstop time. The results prove that the average fanout of data is increased in this design, the signal data power reduces by 71.4% and I/O Power reduces by 61.5%. But it slightly increases the area occupied so as to support both synchronous and asynchronous data transmissions. Also the delay reduced by 26% when compared to existing design.

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